Ultra-low specific on-resistance vertical double-diffused metal–oxide semiconductor with a high-k dielectric-filled extended trench*

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An ultra-low specific on-resistance trench gate vertical double-diffused metal-oxide semiconductor with a high-k dielectric-filled extended trench (HK TG VDMOS) is proposed in this paper. The HK TG VDMOS features a high-k (HK) trench below the trench gate. Firstly, the extended HK trench not only causes an assistant depletion of the n-drift region, but also optimizes the electric field, which therefore reduces $R_{on,sp}$ and increases the breakdown voltage (BV). Secondly, the extended HK trench weakens the sensitivity of BV to the n-drift doping concentration. Thirdly, compared with the super-junction (SJ) vertical double-diffused metal-oxide semiconductor (VDMOS), the new device is simplified in fabrication by etching and filling the extended trench. The HK TG VDMOS with $BV = 172$ V and $R_{on,sp} = 0.85$ mΩ·cm^2 is obtained by simulation; its $R_{on,sp}$ is reduced by 67% and 40% and its BV is increased by about 15% and 5%, in comparison with those of the conventional trench gate VDMOS (TG VDMOS) and conventional superjunction trench gate VDMOS(SJ TG CDMOS).

Keywords: high permittivity, specific on-resistance, breakdown voltage, trench gate

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1. Introduction

The vertical double-diffused metal-oxide semiconductor (VDMOS) field-effect transistor is one of the key devices in power metal-oxide semiconductor field-effect transistor (MOSFET), due to its high switching speed, simple drive circuitry, and easy parallel connection to increasing the output current.[1] In order to minimize conduction loss, a low on-resistance and thus a higher drift doping concentration are required. A low doping concentration is nevertheless necessary to gain a high blocking voltage. There is therefore the silicon limit $R_{on,sp} \propto BV^{2.5}$ for VDMOS.[2,3]

To break the Si-limit, some new devices have been proposed, such as SJ structure and oxide bypassed structure.[4–8] However, the former is sensitive to the charge-imbalance, and the SJ fabrication is complicated and expensive due to epitaxy followed by implantation many times for the high voltage SJ VDMOS.[9,10] The oxide-bypassed fabrication has difficulty in controlling the oxide thickness.[7,8]

Based on HK ($k > 3.9$, k is the relative permittivity) material performances and the trench gate VDMOS,[11–20] an ultra-low specific on-resistance trench gate VDMOS with an HK-filled trench below the trench gate is proposed. Its $R_{on,sp}$ is decreased because the assistant depletion caused by the extended HK trench increases the n-drift region doping concentration. Meanwhile, the extended HK trench optimizes electrical field distribution and thus improves the breakdown voltage.

2. Device structure and mechanism

The schematic cross section of HK TG VDMOS and SJ TG VDMOS are shown in Figs. 1(a) and 1(b), respectively. For HK TG VDMOS, the high-k (HK) dielectric-filled extended trench is placed below the trench gate, which is formed by etching the trench and filling with an HK dielectric material in the n epitaxial Si. In Fig. 1(a), W_n and W_{hk} are the widths of the n-drift region and HK region, respectively, and N_n is the doping concentration of the n-drift region. For SJ TG VDMOS, W_{na} is the width of n-pillar, W_p is the width of p-pillar, N_{na} is the doping concentration of n-pillar, N_p is the doping concentration of p-pillar. The new structure is compared with SJ TG VDMOS, and has the following parameters: the identical thickness $H = 12.5$ μm, width of the device $W = 6$ μm, and length $L_d = 8$ μm of the n-drift region. Other parameters take their own optimum values.

According to the Poisson equation

$$\frac{\partial^2 \phi}{\partial^2 x} = -\frac{\partial E}{\partial x} = -\frac{qN_n}{k\varepsilon_0}, \tag{1}$$

where ε_0 is the dielectric constant of a vacuum. For the narrow n-drift region in the TG VDMOS with the extended trench, the n-drift region and dielectric region are equivalent to a composite material with the effective dielectric constant k_D. If the filling material is an HK dielectric, then $k_S < k_D < k_{hk}$; if it is silicon dioxide (SiO_2), $k_{OX} < k_D < k_S$, where k_S, k_{hk}, and k_{OX} represent the dielectric constants of Si, HK dielectric,

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and SiO_2 in the extended trench, respectively. According to Eq. (1), the high k_D value causes a high N_n, leading to an extremely reduced $R_{on,sp}$ for HK TG VDMOS at the same electric field slope, while a low N_n value results in a high $R_{on,sp}$, due to the lower k_D value for a VDMOS with SiO_2-filled extended trench. For HK TG VDMOS, except for being depleted in the y direction, the n-drift region is also depleted by the metal–insulator–semiconductor (MIS) structure consisting of the gate /HK dielectric/ n-drift region in x direction. The MIS total capacitance C can be considered as a series connection of the depletion-layer capacitance in the n-drift region C_S and the MIS capacitance unit area C_I. The normalized capacitance can be expressed as[21]

$$\frac{C}{C_I} = \frac{1}{\left(1 + \dfrac{2\varepsilon_0 V_{GD} k^2}{d^2 k_S q N_n}\right)^{0.5}}, \tag{2}$$

where d is the distance between the two electrodes in the MIS capacitance and V_{GD} is the voltage between the gate and the drain. The MIS assistant depletion regions are compared with each other for TG VDMOS with the extended trench for the different k values at $V_{DS} = 10$ V in Figs. 2(a)–2(c). The depletion width in the n-drift region increases with the value of k increasing and also with the value of d decreasing as shown in each of Figs. 2(a)–2(c), owing to an increased C_I based on Eq. (2), i.e. $C_{31} > C_{21} > C_{11}$ and $C_{11} > C_{12} > C_{13}$ in Figs. 2(a)–2(c). The relationship between the charge stored in the MIS capacitor and the voltage V_{GD} can be written as $Q = k\varepsilon_0 V_{GD}/d$, where Q is the charge density in the MIS capacitance. A high k value leads to an increase in C_I at the same V_{GD}, Q and the n-drift optimized doping concentration therefore increases as well. The low $R_{on,sp}$ is consequently allowed for HK TG VDMOS. In other words, the HK trench causes an assistant depletion of the n-drift region in the on-state. The higher the k value, the stronger the assistant depletion of the MIS is, which increases the N_n and thus reduces $R_{on,sp}$.

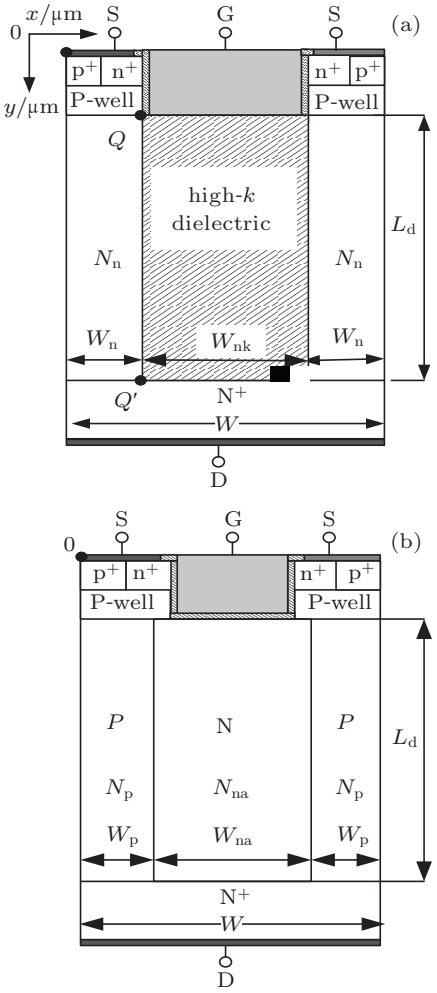


Fig. 1. Schematic cross section of (a) HK TG VDMOS and (b) SJ TG VDMOS.

In the off-state, the gate electrode, the HK dielectric and the drain electrode form a plate capacitor (in Fig. 5(d)). The plate capacitor enhances the vertical field component and weakens the lateral field component, which results in a more uniform vertical electric field distribution and avoids premature breakdown. A high BV is thus obtained. Furthermore, the proposed structure alleviates the sensitivity of BV to the N_n, owing to the HK dielectric and the absence of SJ structure.[15]

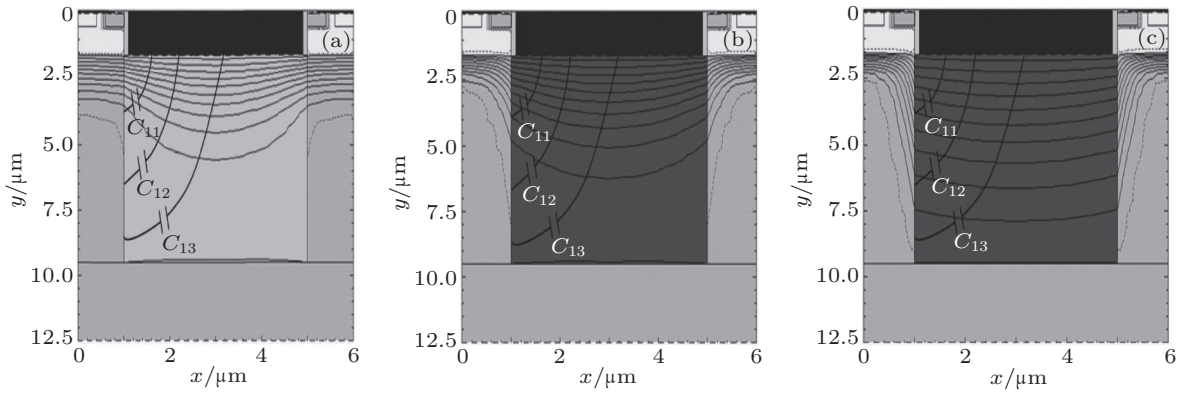


Fig. 2. Depletion regions and equipotential contours for TG VDMOS with the extended trench at $V_{DS} = 10$ V (1 V/contour) and (a) $k = 3.9$ ($N_d = 3 \times 10^{15}$ cm^{-3}); (b) $k = 50$ ($N_d = 1.2 \times 10^{16}$ cm^{-3}); (c) $k = 234$ ($N_d = 1.8 \times 10^{16}$ cm^{-3}).

3. Results and discussion

Figure 3 shows the relationships of BV and $R_{on,sp}$ with N_n for an HK TG VDMOS, a normal TG VDMOS, SJ TG VDMOS, and TG VDMOS with SiO_2-filled trench below the trench gate (OX TG VDMOS). There is a trade-off between BV and $R_{on,sp}$ in order to obtain a high figure-of-merit (FOM) value ($FOM = BV^2/R_{on,sp}$),[22] data in circles represent their own optimal conditions. The $R_{on,sp}$ of HK TG VDMOS is significantly reduced because of the enhanced assistant depleting, and the BV is slightly increased due to the HK trench modulation effect of the n-drift region compared with the SJ TG VDMOS. Furthermore, figure 3 shows that HK TG VDMOS alleviates the sensitivity of BV to the N_n compared with the SJ structure, which contributes to the increase of the BV. For OX TG VDMOS, because of $k_{OX} < k_D < k_S$ based on Eq. (1), the optimal N_n is therefore reduced for the same electric field slope and thus $R_{on,sp}$ is increased. That is to say, the extended SiO_2 trench assistant depletion is weakened and its n-drift doping concentration is lowest, so the values of $R_{on,sp}$ of HK TG VDMOS and TG VDMOS are both less than that of OX TG VDMOS.

Figures 4 and 5 show the electric field distributions along the y direction (at $x = 0.8$ μm) and the equi-potential contours for the HK TG VDMOS, TG VDMOS, SJ TG VDMOS, and OX TG VDMOS, respectively. Compared with TG VDMOS, OX TG VDMOS, and SJ TG VDMOS, the HK TG VDMOS forms the most uniform E-field distribution in the y direction under their own optimal conditions. Figure 4 shows that the E-field peaks at Q for TG VDMOS and OX TG VDMOS as well as the E-field peak at Q' for SJ TG VDMOS to cause premature breakdown, which reduces the BV. Therefore, the BV for HK TG VDMOS increases to 172 V from 164 V of SJ TG VDMOS with the same dimensional parameters as those of SJ TG VDMOS. In Fig. 5, the equi-potential contours for HK TG VDMOS are more uniform than those for OX TG VDMOS and TG VDMOS at the p-body nearby, owing to the plate capacitor effect C_I (consisting of the gate electrode, the HK dielectric and the drain electrode). Figure 5 verifies a more uniform vertical E-field distribution and an improved BV.

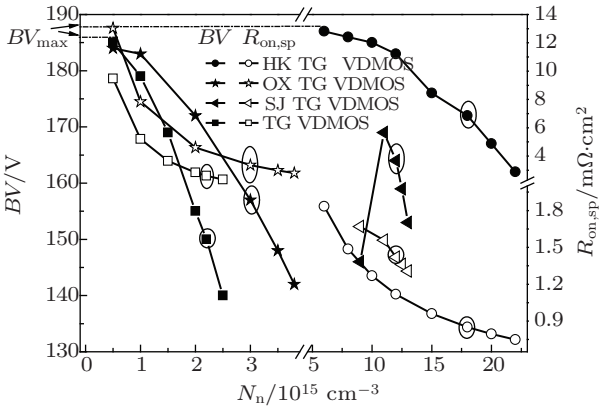


Fig. 3. Dependences of BV and $R_{on,sp}$ on N_n (data in circles represent their own optimal conditions) for TG VDMOS, SJ TG VDMOS, OX TG VDMOS, and HK TG VDMOS (proposed).

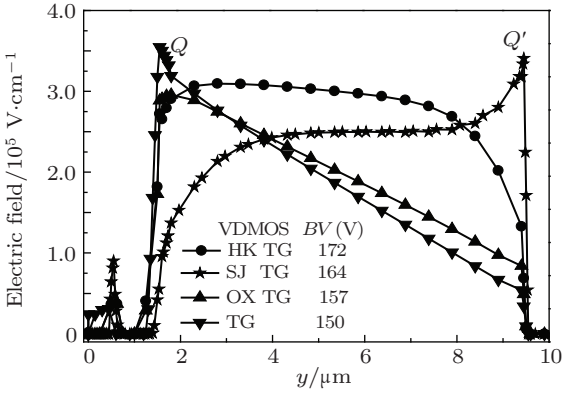


Fig. 4. Electric field distributions along the y direction (at $x = 0.8$ μm, Q and Q' shown in Fig. 1(a), with the optimal conditions in Fig. 2(a)) for TG VDMOS, SJ TG VDMOS, OX TG VDMOS, and HK TG VDMOS (proposed).

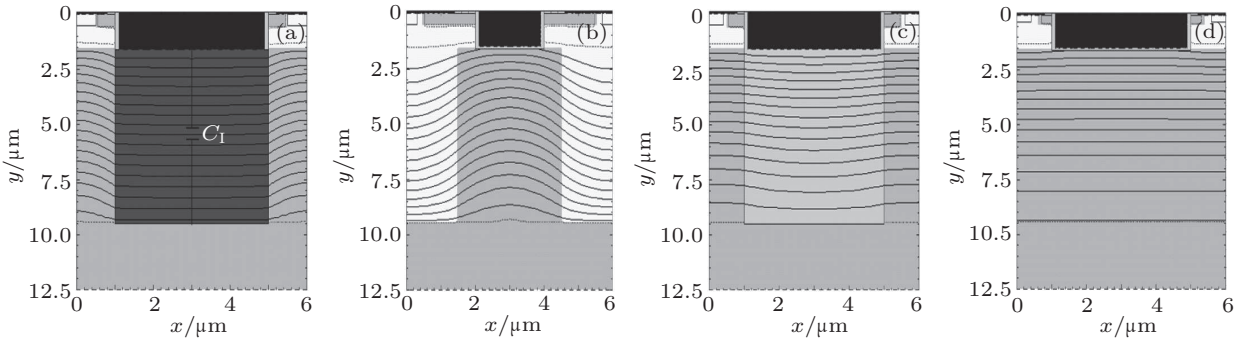


Fig. 5. Equi-potential contours at their breakdown for (a) HK TG VDMOS (172 V), (b) SJ TG VDMOS (164 V), (c) OX TG VDMOS (157 V), and (d) TG VDMOS (150 V) (with the optimal conditions in Fig. 1 10 V/contour).

The values of the BV, $R_{on,sp}$, optimized N_n, and FOM for HK TG VDMOS, TG VDMOS, SJ TG VDMOS, and OX TG VDMOS are given in Table 1. Firstly, $R_{on,sp}$ of the proposed structure is lowest, because the enhanced assistant depletion effect

of the extended HK trench increases the n-drift optimized doping concentration. Secondly, the *BV* of HK TG VDMOS is the highest among these devices, because the HK trench reshapes the electric field and alleviates the sensitivity of *BV* to the N_n. At the same *BV* value of 172 V, the $R_{on,sp}$ value for HK TG VDMOS decreases from 4.61 mΩ·cm^2 of the OX TG VDMOS to 0.85 mΩ·cm^2 with the 6-μm cell pitch by simulation. Thirdly, the *FOM* of HK TG VDMOS is higher than those of other structures as shown in Table 1.

Table 1. Optimized N_n, *BV*, and $R_{on,sp}$ for the four devices (Note: $R_{on,sp}$ is the specific on-resistance at $V_{GS} = 15$ V, $W = 6$ μm).

Device types	$R_{on,sp}$/mΩ·cm^2	Optimized N_n/cm^{-3}	*BV*/V	*FOM* /MW·cm^{-2}
HK TG VDMOS	0.85	1.8×10^{16}	172	35
SJ TG VDMOS	1.42	1.2×10^{16}	164	18.93
OX TG VDMOS	3.36	3.0×10^{15}	157	7.33
	4.61	2.0×10^{15}	172	6.42
TG VDMOS	2.61	2.2×10^{15}	150	8.62

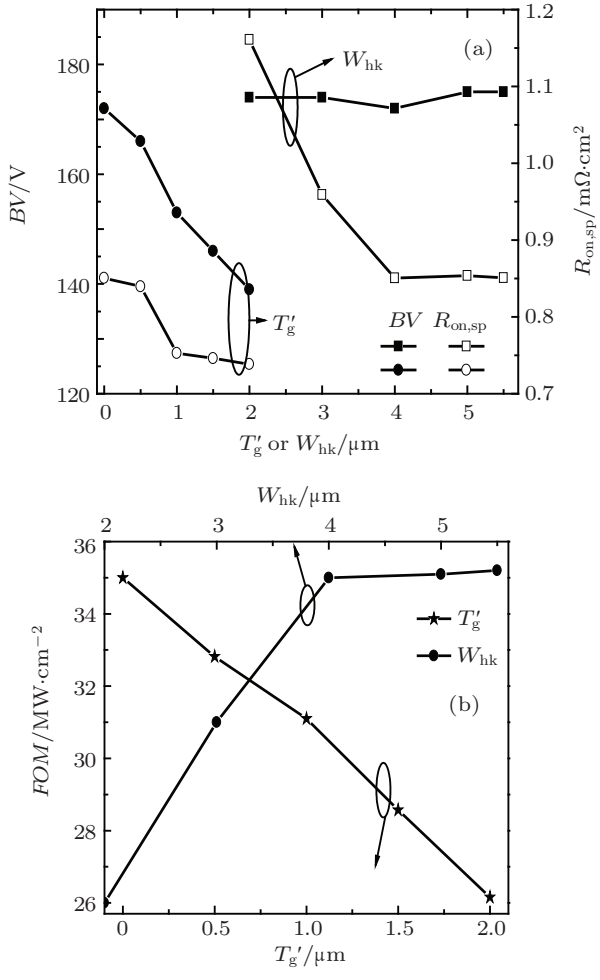


Fig. 6. (a) Dependences of *BV* and $R_{on,sp}$ on W_{hk} or T_g'; (b) Influences of W_n and T_g' on *FOM* for HK TG VDMOS at $W = 6$ μm, $k = 234$.

Figure 6(a) gives the dependences of *BV* and $R_{on,sp}$ on W_{hk} or T_g' for HK TG VDMOS at $W = 6$ μm and $k = 234$. T_g' is the gate bottom lower than the p-body which is introduced for taking the process tolerance into account. The *BV* of HK TG VDMOS stays almost constant and $R_{on,sp}$ reduces significantly with the increase of W_{hk} at $W_{hk} < 4$ μm, because the extended HK trench enhances assistant depletion of the n-drift region. At $W_{hk} > 4$ μm, the $R_{on,sp}$ and *FOM* reach their corresponding saturated value, and the *FOM* value of HK TG VDMOS is the highest in Fig. 6(b).

Because of a lengthened electron accumulation layer beside the trench gate sidewall, with the increase in T_g', $R_{on,sp}$ of HK TG VDMOS gains the reduction. However, the *BV* reduces with the increase of T_g' due to a shortened voltage-sustained region of the HK dielectric below the gate, leading to the premature breakdown near the trench gate sidewall. Furthermore, at $T_g' = 0$ μm, the *FOM* of HK TG VDMOS is the highest in Fig. 6(b).

Figure 7 shows the dependences of BV and $R_{on,sp}$ on *K* for HK TG VDMOS with $W_n = 1$ μm, $W_{hk} = 4$ μm, and $T_g' = 0$ μm. Figure 7 demonstrates that the *BV* of HK TG VDMOS sharply increases and $R_{on,sp}$ decreases with the increase in *k* at $k < 234$, because the extended HK trench modulates the electric field and enhances assistant depletion of the n-drift region. Compared with OX TG VDMOS, the $R_{on,sp}$ reduces 71.5% for an HK TG VDMOS with $k = 234$, due to a high impurity dose (the product of N_nW_n). When $k > 234$, the *BV* and $R_{on,sp}$ stay constant as the value of *k* increases, which reaches the saturation.

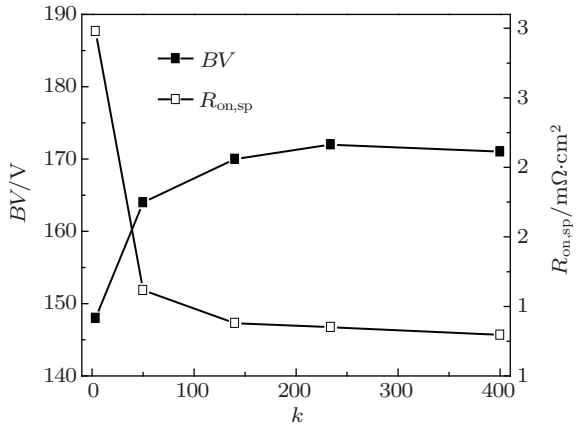


Fig. 7. Dependences of *BV* and $R_{on,sp}$ on *k* for HK TG VDMOS at $W_n = 1$ μm, $W_{hk} = 4$ μm, and $T_g' = 0$ μm.

Figure 8(a) shows the influences of W_n on BV, $R_{on,sp}$, and figure 8(b) displays the influences of W_n on normalized W, $R_{on,sp}$, R_{on}, and BV while the parameters are optimized with the same cell pitch of 6 μm as those in Figs. 6 and 7. As W_n increases, the $R_{on,sp}$ of HK TG VDMOS monotonically increases, while the BV keeps almost constant in Fig. 8(a). According to the expression: $R_{on,sp} = R_{on}W$, showing that $R_{on,sp}$ depends on cell pitch W and R_{on}. At $W_n < 1.0$ μm, although the n-drift doping concentration is very high, the current path is too narrow, R_{on} remains thus almost constant. The $R_{on,sp}$ therefore increases with the increases of W_n and W. At $W_n > 1.0$ μm, both W and R_{on} increase rapidly with the increase in W_n, and $R_{on,sp}$ is therefore sharply increased. Both the above are observed from Fig. 8(b). The optimal value of W_n is 1 μm, taking the difficulty in processing into consideration.

Figure 9 gives the key process steps to fabricate HK TG VDMOS as follows: (i) perform the n-type Si epitaxy (see Fig. 9(a)); (ii) etch Si trench, and thermal growth oxide followed by wet-etch oxide in the trench inner walls to remove damage, then form a pad oxide in the trench inner walls to avoid the degradation of carrier mobility in the near interface between the n-drift region and HK dielectric[16,17] and remove the density of interfacial states (see Fig. 9(b));[19] (iii) fill trench with an HK dielectric, and polish it (see Fig. 9(c)); (iv) Si lateral epitaxial overgrowth to form p-body (see Fig. 9(d)); (v) define the trench gate (see Fig. 9(e)); (vi) form source/drain regions and electrodes (see Fig. 9(f)). Note that TiN material is the trench gate electrode so as to weaken Coulomb scattering;[16] the option of HK dielectrics is SrTiO3 (STO), with a k value up to 300, determined by preparation method and crystallinity. The Si/STO has good interface characteristics due to lattice match.[20]

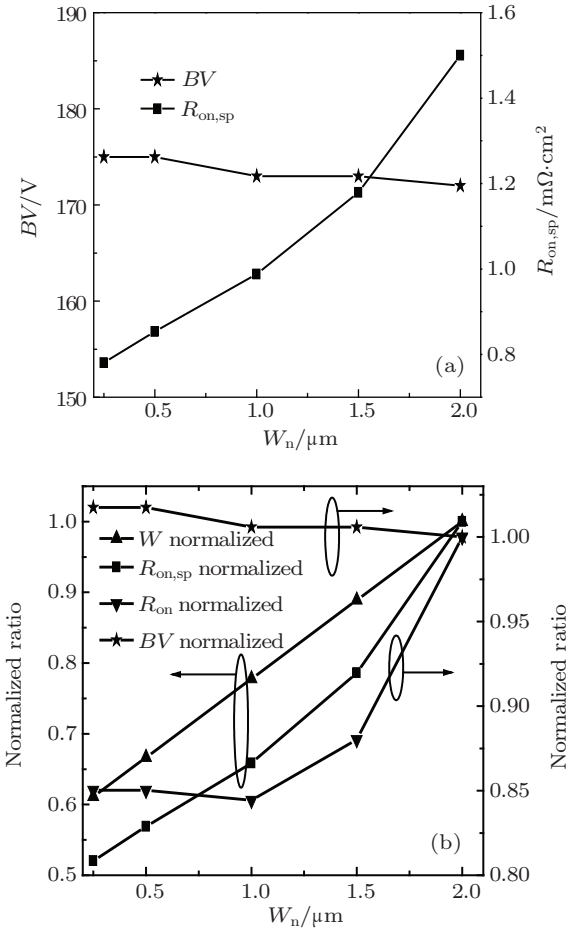


Fig. 8. (a) Influences of W_n on BV and $R_{on,sp}$, and (b) influences of W_n on normalized BV, $R_{on,}$, $R_{on,sp}$, and W for HK TG VDMOS (where BV, R_{on}, and $R_{on,sp}$ are normalized by their corresponding values at $W = 2$ μm, respectively, and W is normalized by 2 μm) $W_{hk} = 5$ μm, $k = 234$, and $T_g' = 0$ μm.

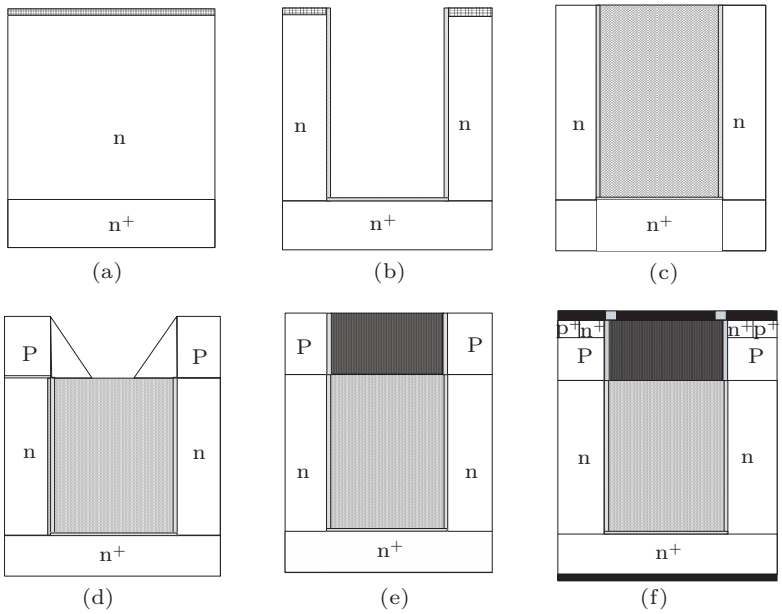


Fig. 9. Key process steps to fabricate an HK TG VDMOS.

4. Conclusion

A new ultra-low specific on-resistance device structure of an HK TG VDMOS is proposed and investigated by simulation. $BV = 172$ V and $R_{on,sp} = 0.85$ mΩ·cm^2 are obtained for $L_d = 8$ μm and the 6-μm cell pitch. The value of $R_{on,sp}$ of the HK TG VDMOS reduces 40% and 67%, and the BV increases 15% and 5% compared with those of SJ TG VDMOS and TG VDMOS, respectively. The novel device not only enhances BV but also significantly reduces $R_{on,sp}$ and overcomes the charge-imbalance issue due to the absence of SJ structure.

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