A low specific on-resistance SOI MOSFET with dual gates and a recessed drain*

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A low specific on-resistance ($R_{on,sp}$) integrable silicon-on-insulator (SOI) metal-oxide semiconductor field-effect transistor (MOSFET) is proposed and investigated by simulation. The MOSFET features a recessed drain as well as dual gates, which consist of a planar gate and a trench gate extended to the buried oxide layer (BOX) (DGRD MOSFET). First, the dual gates form dual conduction channels, and the extended trench gate also acts as a field plate to improve the electric field distribution. Second, the combination of the trench gate and the recessed drain widens the vertical conduction area and shortens the current path. Third, the P-type top layer not only enhances the drift doping concentration but also modulates the surface electric field distributions. All of these sharply reduce $R_{on,sp}$ and maintain a high breakdown voltage (BV). The BV of 233 V and $R_{on,sp}$ of 4.151 mΩ·cm^2 (V_{GS} = 15 V) are obtained for the DGRD MOSFET with 15-μm half-cell pitch. Compared with the trench gate SOI MOSFET and the conventional MOSFET, $R_{on,sp}$ of the DGRD MOSFET decreases by 36% and 33% with the same BV, respectively. The trench gate extended to the BOX synchronously acts as a dielectric isolation trench, simplifying the fabrication processes.

Keywords: MOSFET, silicon-on-insulator, breakdown voltage, specific on-resistance

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1. Introduction

The silicon-on-insulator (SOI) power lateral double-diffused metal-oxide semiconductor (LDMOS) has been widely used in smart power integrated circuits (ICs) owing to its inherent advantages of high reliability, low power loss, and superior isolation.[1–3] Reduced surface field (RESURF) technology has been widely used to improve the trade-off between the $R_{on,sp}$ and breakdown voltage (BV).[4–6] The channel resistance (R_{ch}) plays an important role in the on-resistance of medium- and low-voltage metal-oxide semiconductor field-effect transistors (MOSFETs). A trench gate MOSFET can not only reduce $R_{on,sp}$ by increasing channel density, but also eliminate junction field effect transistor effect (JFET).[6,7] A trench drain shortens the current path and widens the vertical conduction area.[8–10]

Combining the merits of the trench gate, the trench drain, and the RESURF technology, we propose a novel SOI MOSFET which integrates an extended trench gate, a planar gate, and a recessed drain (DGRD). The dual gates reduce $R_{on,sp}$ due to the dual conduction channels; both of the trench gate and the recessed drain widen the vertical conduction area and shorten the extra current path; the P-type top layer not only enhances the drift doping concentration but also modulates the surface electric field distributions. Therefore, a reduced $R_{on,sp}$ and an enhanced BV are obtained.

2. Device structure and mechanism

Figure 1 shows the schematic cross section of a DGRD MOSFET. The DGRD MOSFET has a planar gate and a trench gate extended to the buried oxide layer (BOX). The P-top layer is used to optimize field distribution and increase the N-drift doping. N_d and N_p are the doping concentration of the N-drift region and the P-top layer, respectively. L_{pd} is the space between the P-top layer and the N^+ drain region. A planar gate field plate is employed to improve the surface field distribution. L_{pf} is the space between the P-top layer and the field plate. T_p and T_{dr} are the thicknesses of the P-top layer and the recessed drain in SOI layer, respectively.

In the on-state, the dual gates form dual conduction channels for the DGRD MOSFET. The long electron accumulation layer is formed beside the extended gate in the N-drift to further reduce the $R_{on,sp}$. The multiple-directional depletion regions are caused and strengthened by two MIS-like structures in the dashed rectangle of Fig. 1 (the arrows show the

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depleting direction in the "S" layers of the MIS). It leads to an enhanced RESURF effect. Furthermore, the recessed drain widens the vertical conduction area and shortens the extra current path. Moreover, the P-top layer in the N-drift forms the double RESURF structure to enhance the drift doping concentration. All of these significantly reduce $R_{on,sp}$.

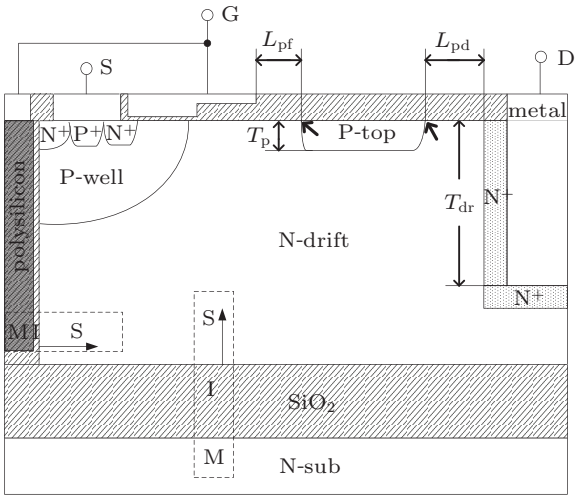


Fig. 1. Schematic cross section of the DGRD MOSFET.

In the off-state, in order to obtain a high BV, the drain does not extend to BOX and an Si-layer below the drain is left to share the BV. The field plate and the P-top layer modulate the surface electric field distributions and the extended trench gate as a vertical field plate improves the bulk field distribution. The blocking voltage capability is thus enhanced.

3. Results and discussion

Figure 2 shows the current flowline contours for the DGRD MOSFET, DGTD (dual gates and a trench drain) MOSFET, TG (trench gate) MOSFET, and Con. (conventional) MOSFET. For the TG MOSFET, although the trench gate spreads the conduction, it lengthens the current path, the $R_{on,sp}$ of 6.46 mΩ·cm^2 is thus the highest. For the Con. MOSFET, the shrunken effective conduction area and the JETF region (in the dashed rectangle) lead to a high $R_{on,sp}$. Two factors cause the substantial reduction in the $R_{on,sp}$ for the DGRD and DGTD MOSFETs: one is the dual conduction channels; the other is the shortened current path caused by the recessed/trench drain and the extended trench gate. The $R_{on,sp}$ values of 4.151 mΩ·cm^2 and 4.012 mΩ·cm^2 are obtained for DGRD and DGTD MOSFET, respectively. In simulation, there are the same device dimensional parameters for several structures as follows: the thicknesses of top silicon ($T_s = 5$ μm) and BOX ($T_{ox} = 2$ μm), and the length of drift region ($L_d = 10$ μm).

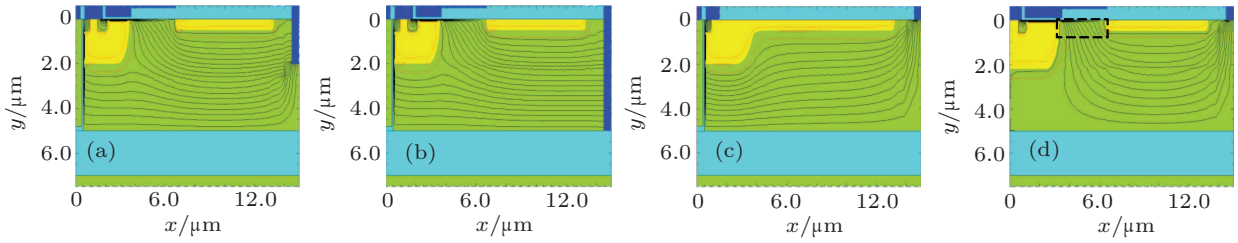


Fig. 2. (color online) Current flowline contours for (a) DGRD MOSFET (4.15 mΩ·cm^2), (b) DGTD MOSFET (4.01 mΩ·cm^2) , (c) TG MOSFET (6.46 mΩ·cm^2), and (d) conventional MOSFET (6.23 mΩ·cm^2) (1×10^{-6} A·μm^{-1}/contour with the optimal N_d for each device and the same cell pitch of 15 μm).

Figure 3 shows the current density in y direction for the four device structures in the middle of cell (at $x = 8$ μm) and in the drain side (at $x = 13.8$ μm). Owing to the recessed/trench drain for the DGRD and the DGTD MOSFETs, their current density in the middle of cell is far higher than those of the TG and the Con. MOSFETs in Fig. 3(a). The $R_{on,sp}$ of the DGRD and DGTD MOSFETs is thus lower than those of the TG and the Con. MOSFETs. In Fig. 3(b), there is a current peak in the bottom of the recessed drain for the DGRD MOSFET, while the current density in the drain side for the DGTD MOSFET is the most uniform due to the trench drain extended to the BOX. For the TG and the Con. MOSFETs with a surface n+ drain region, the current density of drain is concentrated on the surface. Therefore, the conduction area is spread and the current path shortened, resulting in the decrease in $R_{on,sp}$ for the DGRD and DGTD MOSFETs.

Figure 4 shows the equi-potential contours of the four different device structures. For the DGRD MOSFET, the Si layer below the drain shares the vertical voltage drop, while the vertical BV is just sustained by the BOX for the DGTD MOSFET. The BV of the DGRD MOSFET therefore reaches 233 V while it is 211 V for the DGTD MOSFET. In Fig. 4(a)–4(c), the extended trench gate as a field plate enhances the lateral E-field component and weakens the vertical E-field component, as shown in the dash rectangles. For the Con. MOSFET, the vertical electric field is high and SOI layer below the source shares the BV, as demonstrated in Fig. 4(d).

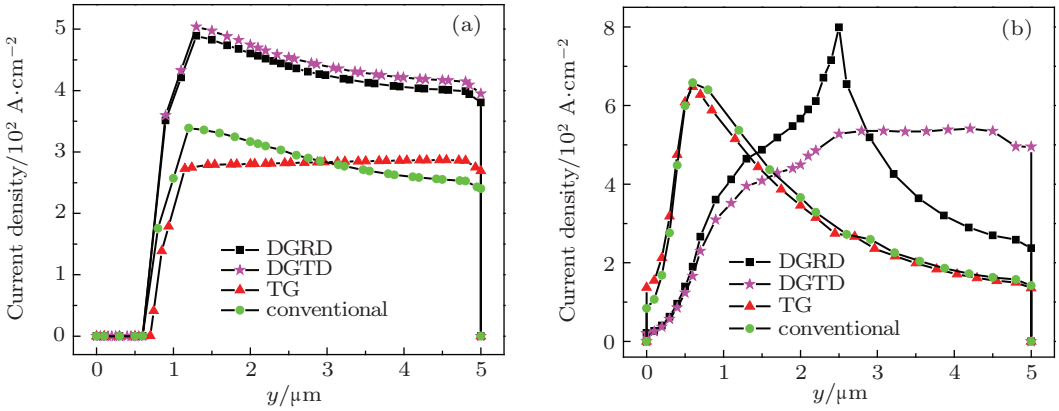


Fig. 3. (color online) current density in y direction (a) $x = 8$ μm and (b) $x = 13.8$ μm.

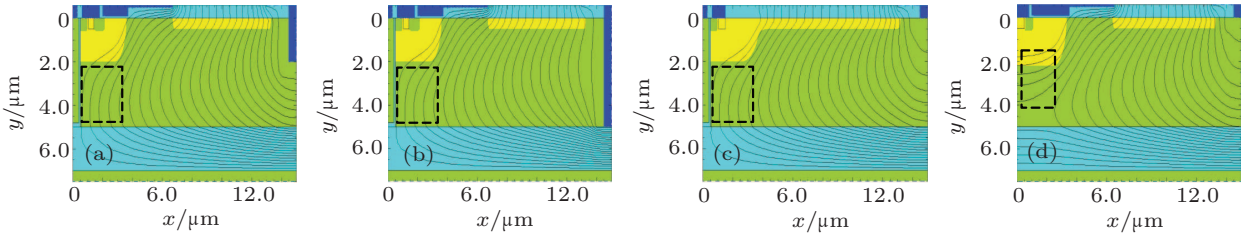


Fig. 4. (color online) Equi-potential contours at breakdown voltage for (a) DGRD (233 V), (b) DGTD (211 V), (c) TG (233 V), and (d) conventional (231 V) SOI MOSFETs (10 V/contour. The structure parameters are the same as those in Fig. 2).

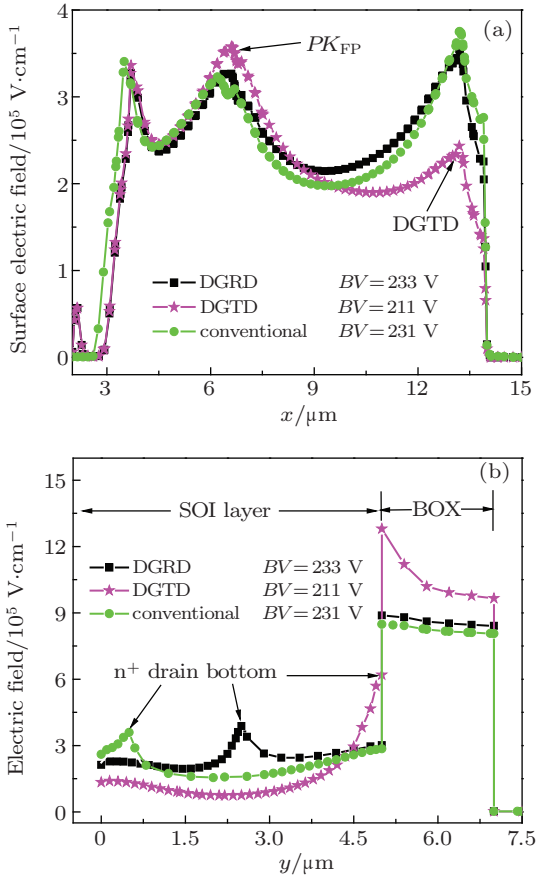


Fig. 5. (color online) Electric field distributions in (a) x direction ($y = 0.01$ μm) and (b) y direction ($x = 13.9$ μm).

Figure 5(a) shows the surface electric field distribution. The E-field peaks PK_{FP} are caused by the field plate of the planar gate for the DGRD, DGTD, and the Con. MOSFETs. It is noted that the surface field strength near the extended drain is the lowest for the DGTD MOSFET. Figure 5(b) is the E-field distribution near the drain in the y direction. The average E-field strength of the DGRD MOSFET in the SOI layer is higher than those of the others. For the DGTD MOSFET, although the E-field strength in the BOX is the highest, the E-field strength in the SOI layer and the voltage drop in the SOI layer are the lowest. The BV of the DGTD MOSFET is thus the lowest.

The values of optimized N_d, BV, $R_{on,sp}$, and FOM (figure of merit, FOM=$BV^2/R_{on,sp}$) for the DGRD, the DGTD, the DG (dual gates), the TG, and the Con. MOSFETs are given in Table 1, respectively. Owing to just the single gate, the $R_{on,sp}$ values are more than 6 mΩ·cm^2 for the TG and the Con. MOSFETs. The DG MOSFET reduces the $R_{on,sp}$ to 4.79 mΩ·cm^2. Furthermore, and the recessed/trench drain decreases the $R_{on,sp}$ to about 4 mΩ·cm^2 for the DGRD and DGTD MOSFETs at the same $V_{GS} = 15$ V and cell pitch of 15 μm. The effect of the recessed drain on reducing the $R_{on,sp}$ will be strengthened as the T_s and T_{dr} increase for a higher BV level device. The FOM of DGRD MOSFET is higher than those of the other structures, as shown in Table 1. As is mentioned before, the multiple-directional depletion is caused and strengthened by the trench gate. Consequently, the optimized N_d values for the devices with a trench gate are higher than that of the conventional MOSFET.

Figure 6 shows the influences of the left endpoint, the

right endpoint and the thickness of the P-top layer on BV and $R_{on,sp}$. In Fig. 6(a), when the left endpoint of the P-top layer and the end of field plate are merged (e.g. $L_{pf} = 0$), the electric field peak formed by the field plate is offset by the P-top layer, it thus prevents premature breakdown and results in a high BV, furthermore, the high optimal N_d and a low $R_{on,sp}$ are obtained. According to the double-RESURF criterion, when L_{pd} increases, the optimal N_d at BV_{max} (in the circles) decreases due to the decrease in the P-top impurity dose. The BV decreases at $L_{pd} \geq 3$ μm in Fig. 6(b). In Fig. 6(c), $T_p < 1.5$ μm is a good choice because the thick P-top layer consumes the conduction area on the on-state, resulting in a high $R_{on,sp}$. In short, the optimal values are $L_{pf} = 0$, $L_{pd} < 3$ μm, and $T_p < 1.5$ μm, respectively.

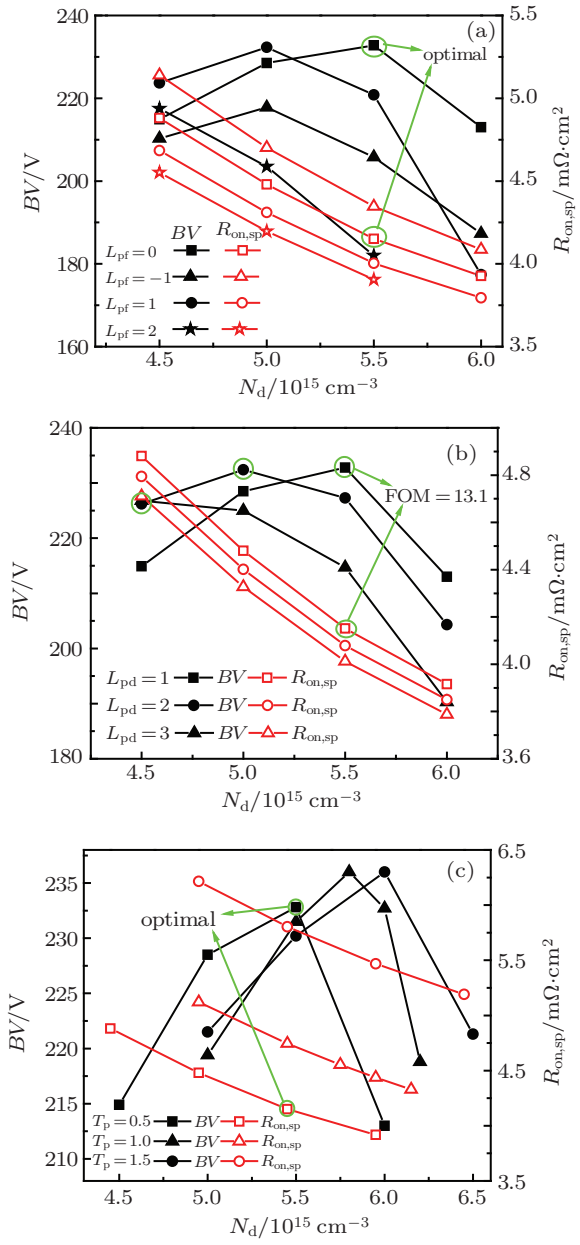


Fig. 6. (color online) Dependences of the BV and $R_{on,sp}$ on (a) L_{pf}, (b) L_{pd}, and (c) T_p for DGRD MOSFET.

Table 1. Optimized N_d, BV, and $R_{on,sp}$ for the four-type devices ($R_{on,sp}$ is the specific on-resistance at $V_{GS} = 15$ V, and half-cell pitch of 15 μm).

Device types	Optimized N_d /cm^{-3}	BV /V	$R_{on,sp}$ /mΩ·cm^2	FOM /MW·cm^2
DGRD MOSFET	5.5×10^{15}	233	4.15	13.1
DGTD MOSFET	5.5×10^{15}	211	4.01	11.1
DG MOSFET	5.4×10^{15}	235	4.79	11.5
TG MOSFET	5.7×10^{15}	233	6.46	8.4
Conventional MOSFET	5.3×10^{15}	231	6.23	8.6

Figures 7 and 8 show the influences of N_p,N_d, and T_{dr} on the BV and $R_{on,sp}$. Figure 7 shows the trade-off between the BV and $R_{on,sp}$ for MOSFETs with the different N_d and N_p. The optimized values of N_d and N_p are 5.5×10^{15} cm^{-3} and 5.5×10^{16} cm^{-3}, respectively. In Fig. 8, as the T_{dr} decreases, the BV increases because of the voltage-sustaining Si layer enlarges below the drain while the $R_{on,sp}$ increases owing to the lengthening current path. The current path increases and the N_d decreases with the decreasing T_{dr} at $T_{dr} < 1.5$ μm. It leads to the significantly increase in the $R_{on,sp}$ and the decrease in the FOM value. Considering the electrical performance and fabrication process, the optimal range of T_{dr} is 1.5 μm$\leq T_{dr} \leq 3$ μm at $T_s = 5$ μm.

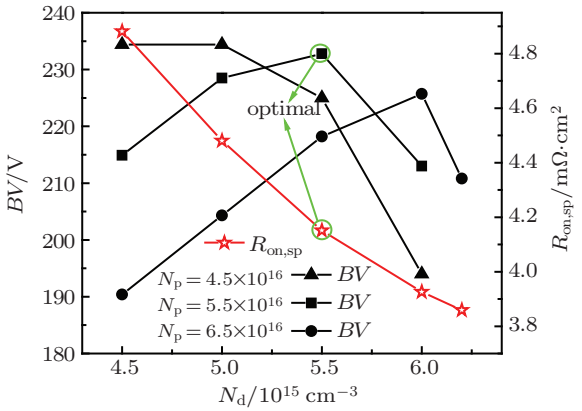


Fig. 7. (color online) Influences of N_d in different N_p on BV $R_{on,sp}$ for the DGRD MOSFET.

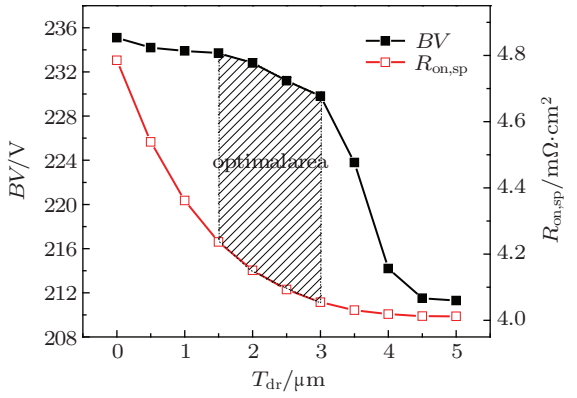


Fig. 8. (color online) Influences of the thickness of the recessed and drain T_{dr} on BV and $R_{on,sp}$ for the DGRD MOSFET at $T_s = 5$ μm.

Figure 9 shows the key fabrication steps for the DGRD MOSFET: (a) form the trench gate, including etch Si trench to the BOX, thermal oxidation to form the gate oxide, and deposition and planarization of poly-silicon; (b) form the drain trench; (c) P-top, P-well implantation and annealing; (d) angled implantation to form N^+ drain region; (e) P^+-contact and N^+-source implantation, and electrode formation.

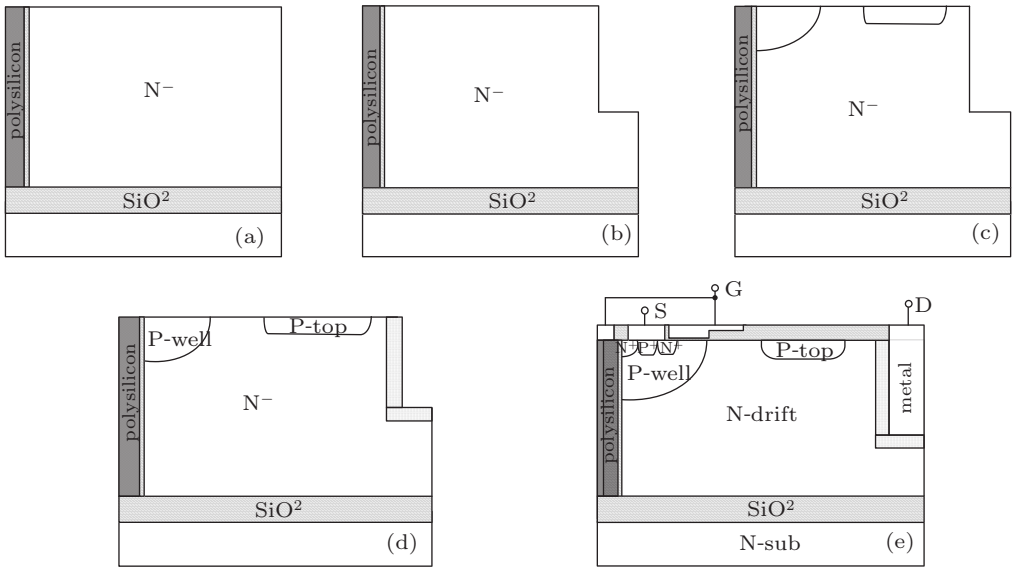


Fig. 9. Key process steps of the DGRD MOSFET: (a) form the trench gate, (b) form drain trench, (c) form P-Top, P-Well, (d) angled implantation, and (e) form P^+-contact and N^+-source to form N^+ drain implantation, and electrodes.

4. Conclusion

The SOI MOSFET with dual gates and a recessed drain is proposed and investigated by simulation. The dual gates form dual conduction channels. The extended trench gate widens the vertical conduction area and the recessed drain shortens the extra current path, resulting in a minimized $R_{on,sp}$. $BV = 233$ V and $R_{on,sp} = 4.151$ mΩ·cm^2 are obtained at 15-μm half-cell pitch. Compared with TG MOSFET and conventional MOSFET, the $R_{on,sp}$ of DGRD MOSFET decreases by 36% and 33%, respectively. Moreover, the trench gate acts as a dielectric isolation trench to remove the additional trench needed in conventional SOI high voltage integrated circuits.

References

[1] Hossain Z, Imam M, Fulton J and Tanaka M 2002 *IEEE ISPSD* **137**
[2] Kong S T, Stribley P and Lee C 2011 *IEEE ISPSD* **176**
[3] Li J H, Li P, Huo W R, Zhang G J, Zhai Y H and Chen X B 2011 *IEEE Electron. Dev. Lett.* **32** 1266
[4] Imam M, Hossain Z and Quddus M 2003 *IEEE Trans. Electron. Dev.* **20** 1697
[5] Popescu A, Udrea F, Ng R and Milne W I 2002 *IEEE Proc. Circ. Dev. Syst.* **149** 273
[6] Luo X R, Zhang W and Gu J J 2009 *J. Semicond.* **30** 1231
[7] Luo X R, Fan J, Wang Y G, Lei T F and Qiao M 2010 *IEEE Electron. Dev. Lett.* **32** 185
[8] Wang C L and Sun J 2009 *Chin. Phys.* B **18** 1231
[9] Ge R, Luo X R, Jiang Y H, Zhou K, Wang P, Wang Q, Wang Y G, Zhang B and Li Z J 2012 *J. Semicond.* **33** 074005
[10] Park I Y, Choi Y I and Chung S K 2001 *Microelectron. J.* **32** 497