The fabrication and characterization of 4H–SiC power UMOSFETs*

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(Received 22 August 2012; revised manuscript received 19 November 2012)

The fabrication of 4H–SiC vertical trench-gate metal-oxide-semiconductor field-effect transistors (UMOSFETs) is reported in this paper. The device has a 15-μm thick drift layer with 3×10^{15} cm^{-3} N-type doping concentration and a 3.1-μm channel length. The measured on-state source–drain current density is 65.4 A/cm^2 at $V_g = 40$ V and $V_{DS} = 15$ V. The measured threshold voltage (V_{th}) is 5.5 V by linear extrapolation from the transfer characteristics. A specific on-resistance ($R_{sp\text{-}on}$) is 181 mΩ·cm^2 at $V_g = 40$ V and a blocking voltage (BV) is 880 V ($I_{DS} = 100$ μA@880V) at $V_g = 0$ V.

Keywords: UMOSFETs, 4H–SiC, specific on-resistance, blocking voltage

PACS: 73.40.–c, 73.40.Qv, 73.61.Le **DOI:** 10.1088/1674-1056/22/2/027302

1. Introduction

Silicon carbide (SiC) is a very attractive semiconductor for high temperature, high-power, and high-frequency devices because of its wide band gap (∼ 3 eV) and high critical breakdown field (3 MV/cm–5 MV/cm), electron saturation drift velocity (2.0×10^7 cm/s), and thermal conductivity (3.7 W/cm·°C–4.9 W/cm·°C).[1–4] For the same blocking voltage, SiC devices offer theoretical specific on-resistance two orders of magnitude lower than that of silicon devices.[5] 4H–SiC power metal-oxide-semiconductor field-effect transistors (MOSFETs) have been recognized as attractive devices for high-voltage switching applications because of the low specific on-resistance and high breakdown critical electrical field of 4H–SiC.[6] Recently, great progress has been made in the development of SiC power MOSFETs.[7–9] For example, a 5-kV power UMOSFET in 4H–SiC (115 μm, 7.5×10^{14} cm^{-3}) was reported with a specific on-resistance of 228mΩ·cm^2.[1] In China, research on SiC materials and devices has made great progress in the past decade.[10–15] However, research has mostly focused on SiC MESFETs, SiC power SBDs, and SiC JBSs, and paid very little attention to SiC power MOSFETs. In this paper, our recent work on 4H–SiC power UMOSFETs is reported. The 4H–SiC power UMOSFETs were successfully fabricated on 15-μm thick 4H–SiC N-type epilayers and the fabricated devices exhibit specific on-resistance of 181 mΩ·cm^2, threshold voltage of 5.5 V, and a blocking voltage (BV) of 880 V, yielding a figure-of-merit (FOM) $BV^2/R_{on\text{-}sp}$ of 4.3 MW/cm.

2. Device structure and fabrication

A schematic cross section of the 4H–SiC UMOSFET is shown in Fig. 1, and figure 2 shows a top view photograph of a fabricated device with an active area of 9.88×10^{-4} cm^2. The presented 4H–SiC UMOSFET consists of nine gate fingers and a 20-μm pitch between gate fingers with no edge termination, based on active epilayer of 4H–SiC grown on a 4° off-axis N$^+$-type 4H–SiC substrate at the Key Laboratory of Wide Band Gap Semiconductor Materials and Devices, Xidian University. The epitaxial structure of the 4H–SiC UMOSFET in our study, from bottom to top, consists of 380 μm/5×10^{18} cm^{-3} N$^+$-type substrate, 15 μm/3×10^{15} cm^{-3} N$^-$-type drift layer, 3.1 μm/2.2×10^{17} cm^{-3} P$^-$-type channel layers, and 1.4 μm/1.0×10^{19} cm^{-3} N$^+$-type source layers.

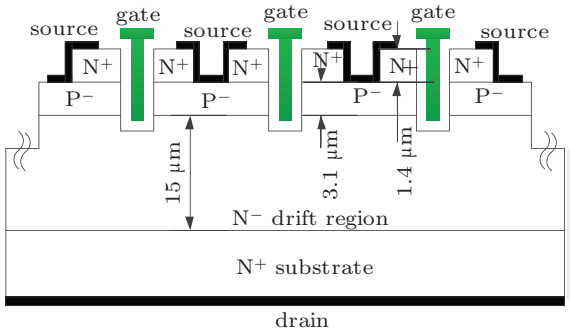


Fig. 1. (color online) Schematic cross section of the fabricated 4H–SiC UMOSFET.

*Project supported by the National Natural Science Foundation of China (Grant Nos. 61176070 and 61274079), the Doctoral Fund of Ministry of Education of China (Grant No. 20110203110010), and the Key Specific Projects of Ministry of Education of China (Grant No. 625010101).

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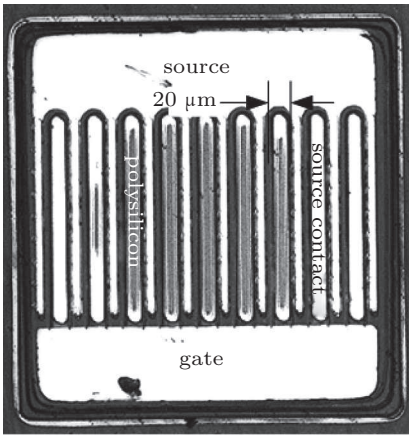


Fig. 2. Top-view of a 9-finger 4H–SiC UMOSFET.

The device fabrication started with mesa isolation approximately 15-μm deep, P-type channel layer contact trenches approximately 1.5-μm deep, and gate trenches approximately 5-μm deep, which were formed by inductively coupled plasma (ICP) etching in a gas mixture of SF_6 and O_2 using a Ni mask. Then, sacrificial oxidation was performed to consume damaged surface layers created by ICP and to smooth the trench sidewalls and corners prior to gate oxidation. The wafer was subsequently oxidized at 1150 °C to form a gate oxide layer. Next, a polysilicon film was deposited and patterned to form the gate contact. Finally, source and drain Ohmic contacts were formed by evaporating Ti/Ni/Al (50 nm/100 nm/200 nm) and annealed with rapid thermal processing (RTP). Direct current (DC) characteristics were measured by using an Agilent-B1500A semiconductor parameter analyzer, while the blocking characteristics measured by a Tektronix 370B curve tracer.

3. Results and discussion

Figure 3 shows the room-temperature transfer characteristics of the 4H–SiC UMOSFET measured at a drain voltage of 100 mV. A threshold voltage of 5.5 V is obtained by linear extrapolation from the linear region of the transfer characteristics. From the semi-log plot of the transfer characteristics, it can be seen that the device is completely pinched off with a drain current of as low as $\sim 3.0\times10^{-10}$ A at $V_g = 1.3$ V and $V_{DS} = 100$ mV.

Figure 4 shows on-state source–drain ($I_D \sim V_{DS}$) characteristics at room temperature for the 4H–SiC UMOSFET with an active area of 9.88×10^{-4} cm^2 with the gate voltage (V_g) increased from (bottom) 0 V to 40 V and the drain–source voltage (V_{DS}) increased from 0 V to 22 V. The device exhibits a drain current density of 65.8 A/cm^2 at $V_g = 40$ V and $V_{DS} = 15$ V. From the slope of the $I_D \sim V_{DS}$ characteristics in the linear region, the specific on-resistance ($R_{sp\text{-}on}$) can be calculated. Figure 5 shows the relationship between the specific on-resistance ($R_{sp\text{-}on}$) and the gate voltage (V_g), which indicates that the total specific on-resistance gradually reduces as the gate voltage increases. This is attributed to the reduced channel resistance that results from increased charge in the inversion layer and the drift region resistance gradually becomes the predominant one. The $R_{sp\text{-}on}$ of 181 mΩ·cm^2 can be obtained from the $I_D \sim V_{DS}$ characteristics at $V_g = 40$ V, as shown in Fig. 5.

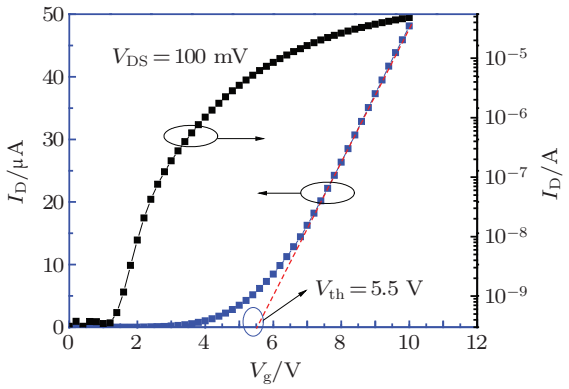


Fig. 3. (color online) Transfer characteristics of a 4H–SiC UMOSFET.

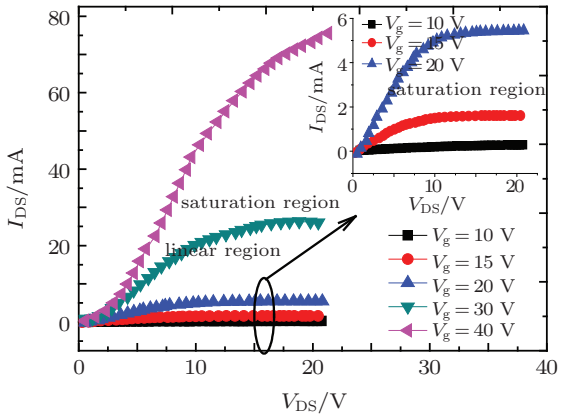


Fig. 4. (color online) On-state characteristics of the 4H–SiC UMOSFET.

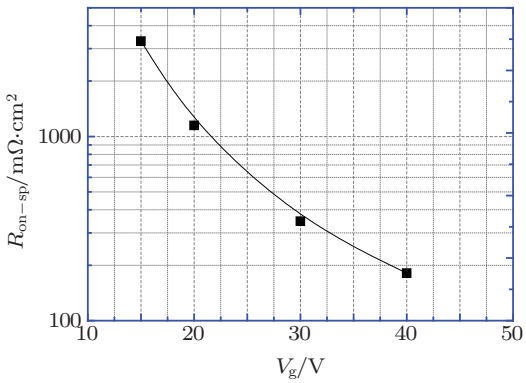


Fig. 5. Relationship between $R_{sp\text{-}on}$ and V_g.

The blocking characteristics of the 4H–SiC UMOSFET is also presented in Fig. 6. The blocking characteristics measurement was performed with a gate voltage of 0 V. The measured blocking voltage is 880 V (about 60% of the theoretical

value). Because no edge termination structure is used in this device, three-dimensional (3D) field crowding at the edges of the trench corners may play a leading role in premature breakdown of the device. The figure of merit (FOM) $BV^2/R_{\text{on-sp}}$ is 4.3 MW/cm, which is a quantity used to evaluate the performance of a power device.

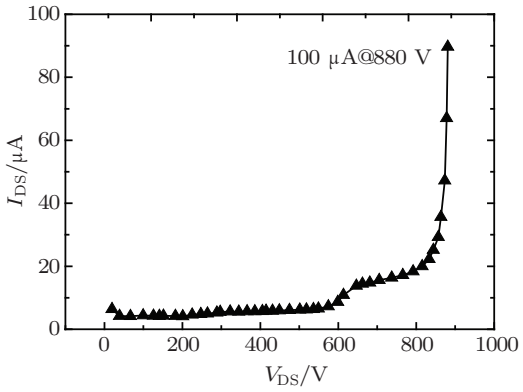


Fig. 6. Blocking characteristics of the 4H–SiC UMOSFET.

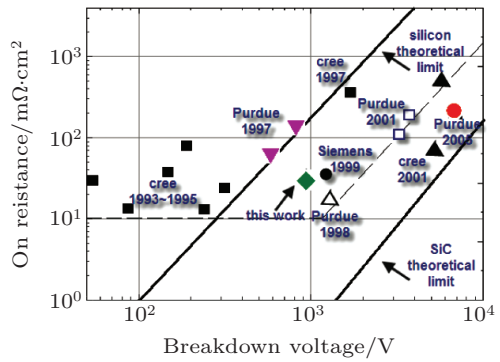


Fig. 7. (color online) On resistance and breakdown voltage of representative 4H–SiC power UMOSFETs since 1993 to date. Solid diagonal lines represent the theoretical limits for silicon and 4H–SiC, and the dashed line represents the current stat-of-the-art in 4H–SiC.

Figure 7 presents the performance of a number of SiC power UMOSFETs reported between 1993 and the present; the device fabricated in our group is included for comparison. Solid diagonal lines in the figure represent the theoretical limits for silicon and 4H–SiC, respectively, and the dashed line represents the current state-of-the-art in 4H–SiC. We can see from the figure that although our devices are fabricated on a relatively thin 4H–SiC epilayer (15 μm/3×10^{15} cm^{-3}), the performance of our fabricated device has been close to the international average level. To further improve the device performance, more work needs to be done in the future, such as ICP etch optimization, gate oxide process optimization, and edge termination technology.

4. Conclusions

A 4H–SiC UMOSFET made on a 15-μm thick drift epilayer has been fabricated and characterized. The presented device shows the V_{th} of 5.5 V and on-state drain current density of 65.8 A/cm^2 at $V_{\text{g}} = 40$ V and $V_{\text{DS}} = 15$ V. The specific on-resistance ($R_{\text{sp-on}}$) is 181 mΩ·cm^2 at $V_{\text{g}} = 40$ V and the blocking voltage (BV) is 880 V ($I_{\text{DS}} = 100$ μA@880 V) at room temperature.

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