High efficiency grating couplers based on shared process with CMOS MOSFETs*

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Grating couplers are widely investigated as coupling interfaces between silicon-on-insulator waveguides and optical fibers. In this work, a high-efficiency and complementary metal–oxide–semiconductor (CMOS) process compatible grating coupler is proposed. The poly-Si layer used as a gate in the CMOS metal–oxide–semiconductor field effect transistor (MOSFET) is combined with a normal fully etched grating coupler, which greatly enhances its coupling efficiency. With optimal structure parameters, a coupling efficiency can reach as high as $\sim 70\%$ at a wavelength of 1550 nm as indicated by simulation. From the angle of fabrication, all masks and etching steps are shared between MOSFETs and grating couplers, thereby making the high performance grating couplers easily integrated with CMOS circuits. Fabrication errors such as alignment shift are also simulated, showing that the device is quite tolerant in fabrication.

Keywords: grating coupler, optical waveguide, silicon-on-insulator, poly-silicon

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1. Introduction

Silicon-on-insulator (SOI) has been considered as a promising platform for photonic integrated circuits (PICs), largely because of its potential process compatibility with complementary metal–oxide–semiconductor (CMOS) electronics.[1,2] Besides, the high index contrast between Si and SiO_2 also enables it to construct waveguides with sub-micron cross sections and very small bending radii, leading to an ultra-high integration density of photonic devices. However, the ultra-compact mode size of the nanowire waveguide induces a large coupling loss between the SOI photonic circuit and the outside world (e.g., optical fibers) due to a huge mode mismatch. To solve this problem, grating couplers fabricated on SOI waveguides have been demonstrated,[3–8] by which sample cleaving is also avoided and wafer-scale testing is enabled with a large alignment tolerance. About 31% coupling efficiency as well as 40-nm 1-dB bandwidth has been realized previously,[3] with an additional lithography and etching step to fabricate the shallow-etched grating. To simplify the fabrication process by avoiding the shallow etching process, fully etched grating couplers are introduced,[6,7] but the reported coupling efficiency is quite low, thus restricting their practical applications. Higher coupling efficiency can be achieved by introducing a poly-Si layer.[8] However, an additional dedicated etching step (etching through the poly-Si layer until the underlying crystalline Si has partially etched) is necessary to pattern the grating structure.

In this paper, a novel high efficiency grating coupler is proposed. The poly-Si layer with the same etching profile as the gate of the metal–oxide–semiconductor field effect transistor (MOSFET) is combined with a normal fully etched grating coupler to form the new structure. With the poly-Si layer, the diffraction directionality of the grating coupler is greatly enhanced, making the coupling efficiency much higher than that of the normal fully etched grating coupler. Since the poly-Si layer process is shared between grating couplers and CMOS MOSFETs, the high performance grating couplers can be conveniently integrated with CMOS circuits without adding any additional mask and process step.

2. Device structure and fabrication process

The proposed grating coupler is shown in Fig. 1. The poly-Si layer used as a gate in the CMOS MOSFET is combined with a normal fully etched grating coupler to form a new structure. SOI wafers each with a 220-nm thick top silicon ($n_{Si} = 3.47$) layer and a 2-μm thick buried oxide (BOX, $n_{SiO_2} = 1.44$) layer are used. A CMOS MOSFET is also shown in this figure. The poly-Si layer serves as the grating coupler as well as the gate. The period of the grating is Λ and the filling factor (FF) is defined as FF=w/Λ.

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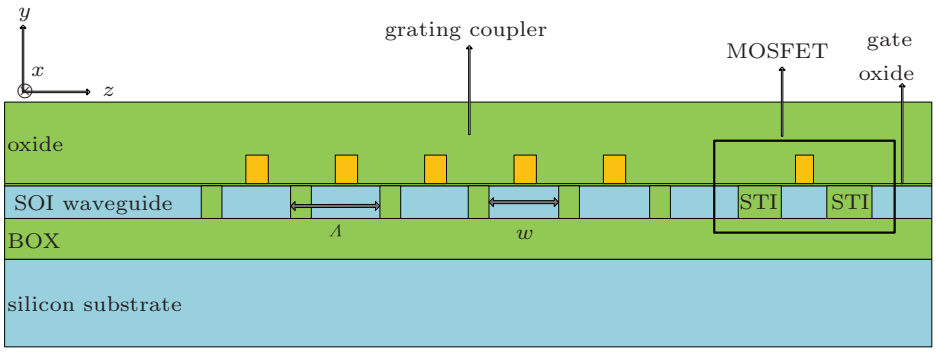


Fig. 1. (color online) Schematic configuration for the grating coupler with poly-Si loaded on a normal fully etched grating coupler.

The fabrication process for integrating both the grating couplers and MOSFETs is proposed and shown in Fig. 2. A silicon nitride (SiN) layer (typically 110-nm thick for deep sub-micrometer CMOS process) is first deposited on the SOI wafer surface. Shallow trenches are then formed using deep ultraviolet (DUV) lithography and reactive ion etching (RIE) as isolations (STIs) of MOSFETs and photonic devices, thereby defining the active regions of MOSFETs, silicon waveguides and the full-etched crystalline-Si (c-Si) part of the grating coupler. With photoresist used as the hardmask, no SiN is lost during the etching process. After filling the trenches with SiO_2 with high density plasma chemical vapor deposition (HDP CVD), a chemical mechanical polishing (CMP) process is performed to planarize the wafers with the deposited SiN serving as the polishing stop layer. The remaining SiN layer ($\sim$ 80-nm thick after CMP process) is removed with hot phosphoric acid. After that, the gate oxide and poly-Si gate layer are grown on the top of the wafer. DUV lithography and poly-Si etching are performed to define the poly-Si gates of the MOSFETs and the full-etched poly-Si part of the grating coupler.

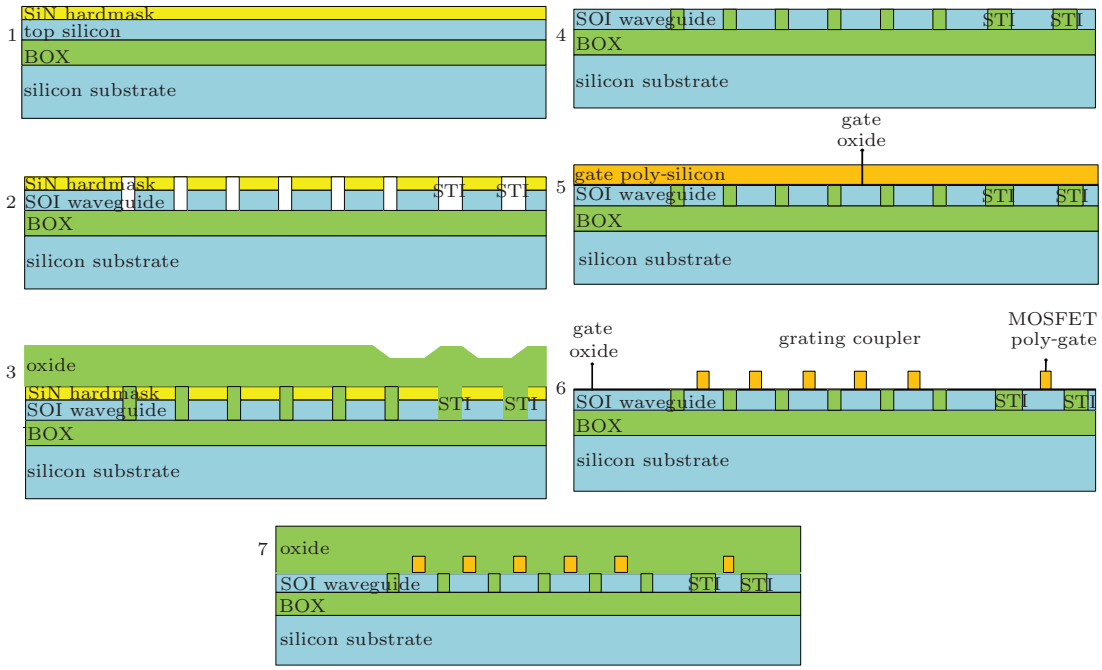


Fig. 2. (color online) Flow charts of integrating the grating couplers and CMOS MOSFET.

3. Simulation results and discussion

Typically the coupling efficiency (η) of a grating coupler can be calculated by

$$\eta = \eta_1 \cdot \eta_2 \cdot \eta_3, \tag{1}$$

where η_1 represents the power fraction that is diffracted out of plane by the gratings, and is given by

$$\eta_1 = 1 - R - T, \tag{2}$$

with R and T being the reflected and transmitted power frac-

tions, respectively; η_2 denoting the directionality, defined by the ratio of the upward power to the total out-of-plane diffracted power as expressed as

$$\eta_2 = P_{\rm up}/(P_{\rm up}+P_{\rm down}); \quad (3)$$

η_3 referring to the mode matching efficiency between the upward light mode and the fiber mode, which can be evaluated by the overlapping integral of the above-mentioned two modes.

To optimize the structure of the proposed grating coupler, CAMFR,[9] a two-dimensional full-vectorial solver based on eigen-mode expansion, is used. The transverse electric (TE) polarization and a wavelength of 1.55 μm are assumed.

The influence of FF and period Λ is first simulated and the simulation results are shown in Fig. 3. While the fully etched trenches induce a large index contrast between the grating and the waveguide, the light reflection is quite strong. The peak reflection occurs around the period that satisfies the Bragg condition. As the period deviates from the Bragg condition, reflection decreases quickly while the transmitted power begins to increase. Reflection and transmission should both be suppressed to improve η_1. The same situation appears in the case of FF. The index contrast decreases gradually as FF increases, which reduces the reflection. R and T can both reach as low as 5% (corresponding to η_1=0.9) with FF=0.9 and $\Lambda = 0.68$ μm. For such small trenches each with an aspect ratio of ~ 5, a high aspect ratio process (HARP)[10] may be required to fill the trenches with SiO_2.

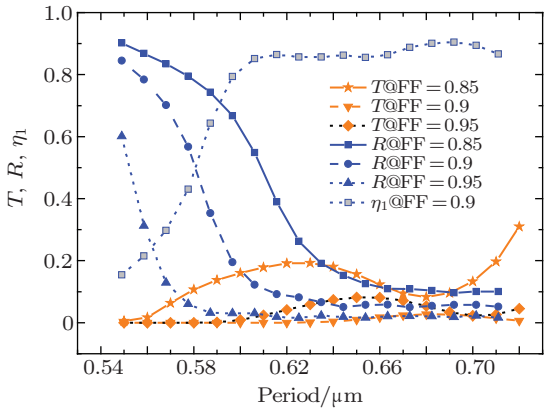


Fig. 3. (color online) R, T, and η_1 each as a function of FF and Λ of the grating.

The main effect of the poly-Si layer is to improve η_2, i.e., the directionality.[8] For a normal fully etched grating coupler as shown in Fig. 4(a), the input power is diffracted upward and downward at the same time. The directionality is no more than 50% because of vertical symmetry. For the present grating couplers with poly-Si layer, figure 4(b) shows that power diffracted downward interferes destructively while power diffracted upward interferes constructively at the same time. Therefore, the directionality can be greatly improved with proper poly-Si thickness and width. Figure 5 shows the directionalities of the two kinds of grating couplers. With the poly-Si layer introduced, the directionality can be improved from 65% to as high as 94%. Besides, the sensitivity to the BOX thickness is greatly reduced. This is because less power is diffracted downward, which alleviates the resonance of the cavity formed between the top silicon layer and the silicon substrate.

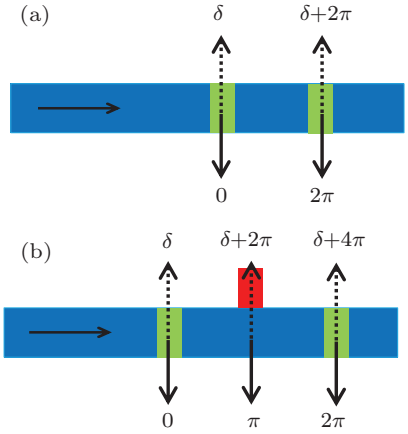


Fig. 4. (color online) Upward and downward diffraction of the grating couplers without (a) and with (b) poly-Si.

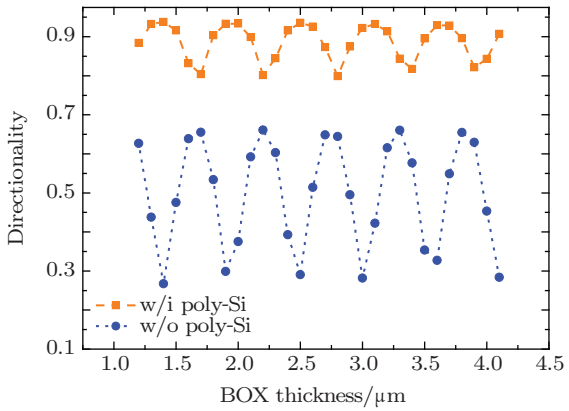


Fig. 5. (color online) Directionality η_2 for fully etched grating couplers with and without poly-Si.

The η_3, mode matching efficiency, between the upward diffracted field and fiber mode, is shown in Fig. 6 as a function of fiber tilt angle. Matching efficiency of 79% is obtained with a tilt angle of 18°, which is close to the upper limit of the matching efficiency for a uniform grating coupler.[3] The mode match can be further improved with chirped grating couplers.[3] With the optimized parameters, coupling efficiency as high as 67% is obtained by Eq. (1), which is much higher than that of the normal fully etched grating coupler.[6,7] The spectral response of the grating coupler is shown in Fig. 7 with a 3dB-bandwidth of ~ 70 nm, and it accords well with the calculated result using Eq. (1).

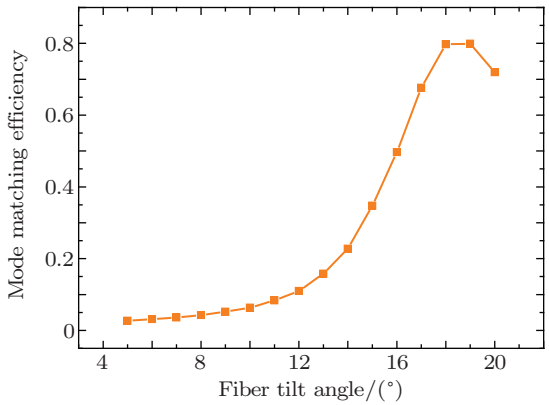


Fig. 6. (color online) Mode matching efficiency between the grating coupler and the fiber.

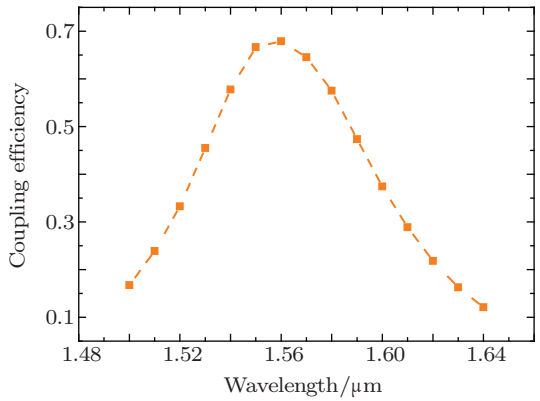


Fig. 7. (color online) Spectral response of the optimized grating coupler.

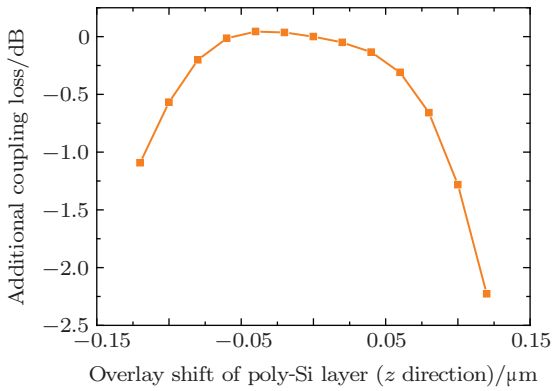


Fig. 8. (color online) Additional coupling loss due to alignment shift of the poly-Si layer (z direction).

Considering the fact that the present grating coupler is formed with two steps lithography, the influence of the alignment shift on coupling efficiency is also evaluated. The overlay error may degrade the directionality and thus the coupling efficiency as shown in Fig. 4(b). Figure 8 shows that the 1-dB performance degradation corresponds to an alignment tolerance of ± 80 nm. For DUV lithography, alignment shift less than 50 nm can be readily achieved, thereby making the fabrication quite tolerant.

4. Conclusion

A novel high efficiency grating coupler is proposed. A poly-Si layer used as the gate in the CMOS MOSFET is combined with a normal fully etched grating coupler to form a new structure. With the poly-Si layer, diffraction directionality and thus coupling efficiency of the grating coupler are greatly improved. Coupling efficiency as high as $\sim 70\%$ can be achieved at a wavelength of 1550 nm, much higher than that of the normal fully etched grating coupler. Since the poly-Si processing for the grating coupler is shared with the CMOS MOSFET, the present grating coupler (as well as the SOI waveguide) can be embedded into a CMOS process without any additional step.

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