0.15-μm T-gate $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ InP-based HEMT with f_{max} of 390 GHz*

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In this paper, 0.15-μm gate-length $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ InP-based high electron mobility transistors (HEMTs) each with a gate-width of 2×50 μm are designed and fabricated. Their excellent DC and RF characterizations are demonstrated. Their full channel currents and extrinsic maximum transconductance ($g_{m,max}$) values are measured to be 681 mA/mm and 952 mS/mm, respectively. The off-state gate-to-drain breakdown voltage (BV_{GD}) defined at a gate current of −1 mA/mm is 2.85 V. Additionally, a current-gain cut-off frequency (f_T) of 164 GHz and a maximum oscillation frequency (f_{max}) of 390 GHz are successfully obtained; moreover, the f_{max} of our device is one of the highest values in the reported 0.15-μm gate-length lattice-matched InP-based HEMTs operating in a millimeter wave frequency range. The high $g_{m,max}$, BV_{GD}, f_{max}, and channel current collectively make this device a good candidate for high frequency power applications.

Keywords: breakdown voltage, cut-off frequency, high electron mobility transistors, maximum oscillation frequency

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1. Introduction

Millimeter and submillimeter wave frequency ranges are of great interest for remote atmospheric sensing, next-generation automotive collision-avoidance radars, broadband satellite communications and low noise detectors. Benefiting from high sheet electron density, high peak drift velocity and high low-field electron mobility in channel of high electron mobility transistors (HEMTs), they have the performances of high operating frequency, low noise and high-gain, and are considered to be one of the most promising devices for these millimeter wave-band applications. Up to now, unflagging efforts have concentrated on HEMTs based on various substrate materials,[1–4] InP-based HEMTs, especially, exhibit superior frequency properties, and many high-performance InP-based HEMTs have been reported, e.g., an extrinsic maximum transconductance ($g_{m,max}$) of 1.62 S/mm, a maximum current gain frequency (f_T) of 628 GHz, and a unilateral power-gain gain frequency (f_{max}) of 331 GHz for 30-nm InAs pseudomorphic InP HEMT[5] and $f_T = 385$ GHz, $f_{max} = 1.2$ THz for sub-50-nm InP HEMT.[6] These remarkable results stem from gate size scaling and indium composition increasing in channel. However, HEMT with high indium content channel usually suffers from serious kink-effect in DC characteristics, low breakdown voltage, and high output conductance, which are caused by impact ionization. This phenomenon is even more remarkable for a short gate-length device, in which a much higher electric field exists under the gate area. The adoption of $In_{0.53}Ga_{0.47}As$ channel and an InP etching-stopper layer should be effective to avoid kink-effect.[7]

Power amplification at extremely high frequencies is very challenging for device technology development. In addition to high frequency-gain and drain current, sufficient off-state drain-to-gate breakdown voltage (BV_{DG}) should be simultaneously maintained to achieve high output power density, which means that the device must be carefully optimized for these comprehensive properties. Great strides have been made in improving off-state breakdown in HEMT through a variety of approaches, including using un-doped or lightly-doped caps, high aluminum content barrier, composite channels, quantized channels, and novel gate recess schemes.

In this paper, the design, fabrication, and characteristics of 0.15-μm gate-length $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ InP-based HEMTs are described. To improve breakdown voltage and f_{max}, lattice-matched $In_{0.53}Ga_{0.47}As$ channel is adopted, Ohmic contact is improved by using a composite cap layer and non-alloy metal, and also the gate recess process is optimized for trade-off between DC and RF performance. The measured full channel current and $g_{m,max}$ are 681 mA/mm and 952 mS/mm, respectively. The BV_{DG} of the device without passivation of SiN is 2.85 V, defined at a gate current of 1 mA/mm. f_T and f_{max} of the HEMT are 164 GHz and 390 GHz respectively.

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2. Device structure

Figure 1 shows a schematic cross section of InP HEMT. To achieve high frequency characteristics at no expense of off-state breakdown voltage, the epitaxial structure of HEMT employed in our study is designed and optimized with parameters shown in Table 1. The epitaxial layer structures are grown on 3-inch semi-insulating (100) InP substrates by molecular beam epitaxy (MBE). From bottom to top, the layers consist of an InAlAs buffer and a lattice-matched $In_{0.53}Ca_{0.47}As$ channel to degrade impact ionization, thus improving breakdown voltage. Subsequently, an unstrained InAlAs spacer layer, an 8-nm unstrained InAlAs Schottky barrier layer and an InP etching stopper layer are grown on the top of the channel layer. An Si-doped plane is inserted between the Schottky layer and spacer layer to supply electrons for current conduction. The thick barrier layer is designed to reduce the gate leakage current, and finally enhance the channel current density and BV_{DG}. Finally, a composite InGaAs cap layer consisting of an Si-doped $In_{0.6}Ga_{0.4}As$ cap layer and an Si-doped $In_{0.53}Ga_{0.47}As$ transition layer are grown to facilitate Ohmic contact formation, thus increasing $g_{m,max}$ and improving frequency property. All InAlAs layers are lattice matched with InP substrate. The two-dimensional electron gas (2DEG) sheet density is 3.266×10^{12} cm^{-2} and the mobility is 8000 cm^2/(V·s) at room temperature.

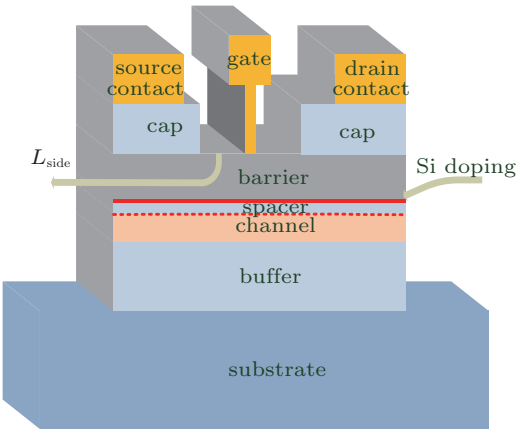


Fig. 1. (color online) Schematic cross section of the InP-based HEMT.

Table 1. Device epitaxial layer structure.

Layer	Material	Doping	Thickness
Cap layer	$In_{0.6}Ga_{0.4}As$	Si:N^{++} 3×10^{19} cm^{-3}	10 nm
Cap layer	$In_{0.53}Ga_{0.47}As$	Si:N^{+} 5×10^{18} cm^{-3}	10 nm
Etch stop layer	InP		4 nm
Barrier layer	$In_{0.52}Al_{0.48}As$	undoped	8 nm
Si planar-doped layer		5×10^{12} cm^{-2}	
Spacer layer	$In_{0.52}Al_{0.48}As$	undoped	3 nm
Channel	$In_{0.53}Ga_{0.47}As$	undoped	15 nm
Buffer layer	$In_{0.52}Al_{0.48}As$	undoped	500 nm
S.I.InP Sub			

3. Device fabrication

Figure 2 shows a plane view of the fabricated offset-gate HEMT with a gate-width of 2×50 μm. In the structure, the T-gate electrode is located at an offset position from the center toward the source. The structural improvement minimizes the gate-to-drain capacitance (C_{gd}) and the source resistance (R_s), thus enhancing the extrinsic transconductance and frequency characteristics. In our device, the spacing between source and gate foot is 0.875 μm.

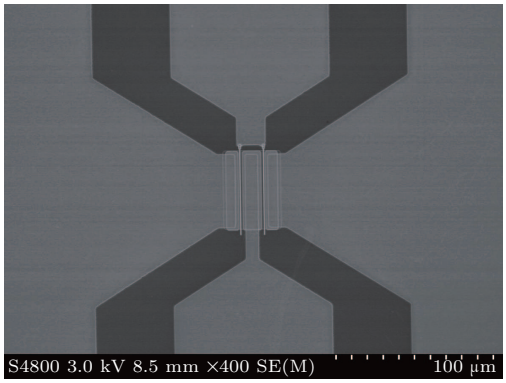


Fig. 2. The SEM image of the HEMT device (2×50-μm gate-width).

The HEMT fabrication is based on both optical and electron beam lithography (EBL). Firstly, the device isolation is achieved through mesa formation by means of a phosphorus acid-based wet chemical etching to expose the $In_{0.52}Al_{0.48}As$ buffer layer. Secondly, source and drain Ohmic contact are spaced 2.4 μm apart by a lift-off process. Then, Ti/Pt/Au is evaporated by an electron beam evaporator to achieve Ohmic metallization without annealing. Transmission Line Method (TLM) measurements reveal the contact resistance of 0.032 Ω·mm and the specific contact resistivity of 1.03×10^{-7} Ω·cm^{-2} on linear TLM patterns. Thirdly, in order to measure on-wafer DC and RF characteristics, the coplanar waveguide bond pads are formed using photoresist AZ5214, and Ti/Au connection wires are evaporated.

The final and most important process in the HEMT fabrication is the gate process, which includes gate lithography, recess, and metallization. Firstly, three layers of electron beam (EB) resist of PMMA/Al/UVIII are coated on the surface. Then EB exposure and the development of each EB resist layer are carried out in turn. Secondly, the gate recess is formed by a phosphorus acid/hydrogen peroxide wet etching till the InP etching-stopper layer, which serves as a surface passivation layer to avoid the kink-effect in DC characteristic. The reduction of side-etched region length (L_{side}) is helpful to suppress the kink-effect,[8] besides, it enhances the electric field in channel and reduces the access part of R_s and R_d, thus increasing the extrinsic transconductance, and finally improving f_T and f_{max}. However, the reduction of L_{side} is not beneficial to f_{max} due to the enlarged gate-to-drain capacitance (C_{gd}), and

also it degrades breakdown voltage due to the increased electric field between gate and drain. In order to reach a balance between the DC and RF characteristics, L_{side} is optimized to be about 422 nm (in Fig. 3) through controlling the gate recess etching time. Finally, a Ti/Pt/Au gate metal is evaporated and lifted off. The SEM image of the fabricated 0.15-μm T-gate by EBL is shown in Fig. 4.

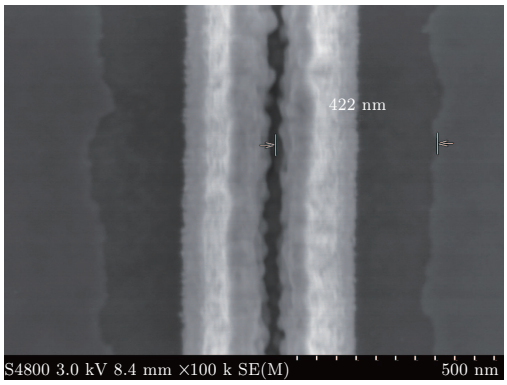


Fig. 3. The SEM image of the device gate recess region with L_{side} of 422 nm.

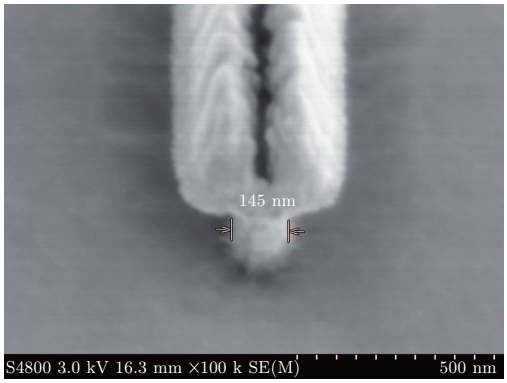


Fig. 4. The SEM image of the fabricated 0.15-μm T-gate.

4. Results and discussion

The on-wafer DC, RF, and power performance of the HEMTs are characterized by an HP4155A semiconductor parameter analyzer, Agilent E8363B PNA series vector network analyzer, and 18-GHz load pull system at room temperature.

4.1. DC Characteristics

From the *I*–*V* characteristics in Fig. 5, it may be concluded that the device exhibits no kink-effect. Also, good pinch-off, saturation drain current and output conductance characteristics are observed.

Figure 6 demonstrates the gate-bias dependence of extrinsic transconductance and drain current of the InP-based HEMT biased at $V_{DS} = 2.0$ V. The pinch-off voltage is about −0.6 V. The high dopant composite InGaAs cap layers ensure an extremely small Ohmic contact resistance of 0.032 Ω·mm, in addition, short source-drain space minimizes the access parasitic resistance. Therefore, a $g_{m,max}$ of 952 mS/mm is obtained at $V_{GS} = -0.15$ V. The measured full channel current of 681 mA/mm at V_{GS} of 0.5 V and a saturation drain-to-source current of approximately 418 mA/mm at V_{GS} of 0 V are demonstrated.

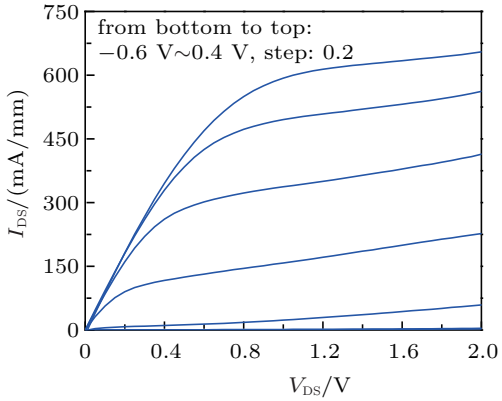


Fig. 5. (color online) Drain currents of the InGaAs/InAlAs HEMT each as a function of V_{GS}.

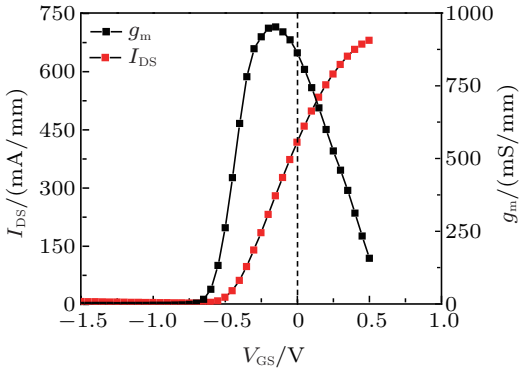


Fig. 6. (color online) Extrinsic transconductance and the drain current each as a function of V_{GS}.

Besides high $g_{m,max}$ and channel current, a well-designed power device is one that features a relatively high breakdown voltage compared with the threshold voltage. The off-state breakdown event in InAlAs/InGaAs/InP HEMT is believed to happen by two steps: electrons are initially injected from the gate edge into the high-field drain-gate region of the wide band-gap InAlAs layer by thermionic-field emission. Subsequently, as a consequence of large channel electric field and substantial conduction-band offset between InAlAs layer and InGaAs channel, the electrons entering into the channel may be hot, and relax their energy through impact ionization.

Drain–current injection technique[9] is used to measure off-state breakdown voltage. There is no ambiguity in the selection of gate–source voltage. The measuring configuration by HP4155A semiconductor parameter analyzer and a typical result are shown in Fig. 7. In the measurement, a fixed predefined current of $I_D = 1$ mA/mm is injected into the drain. The V_{GS} is scanned from −2 V to 0 V, which includes the

linear, saturation, and breakdown region. Then, the drain-to-gate voltage (V_{DG}) and the gate current (I_G) versus V_{GS} are monitored. The BV_{DG} defined at $I_D = -I_G = 1$ mA/mm unambiguously is 2.85 V. The BV_{DG} increases to more than 4.1 V, after the device has been fully passivated with 500 Å SiN deposited by plasma-enhanced chemical vapor deposition (PECVD). The excellent BV_{DG} benefits from the following aspects: firstly, the suppressed gate leakage current due to a long distance of 15 nm from gate to channel; secondly, the optimized gate recess etching, which is balanced among good DC characteristics, high extrinsic transconductance and high BV_{DG}; lastly, low indium composition channel material that is adopted to weaken impact ionization. The high BV_{DG} means a larger operating voltage in power application and a larger logic swing in digital circuits.

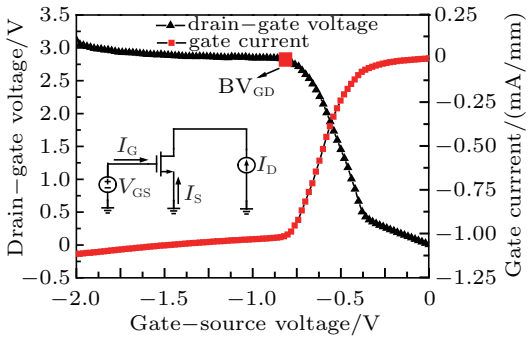


Fig. 7. (color online) Illustration of the drain-current injection technique to measure BV_{DG}.

4.2. RF characteristics

The *S*-parameter measurements are carried out at frequencies ranging from 0.1 GHz to 40 GHz in steps of 0.1 GHz. Open and short pads are also performed on the same wafer in order to calibrate the parasitic capacitance and inductance components related to the pad metal. The value of f_T is determined by extrapolating the current gain (H_{21}), and the value of f_{max} is obtained by extrapolating the maximum available/stable power gain (MAG/MSG) of the HEMT using a least-square fitting with a −20 dB/decade slope after subtracting the parasitic parameters.

As shown in Fig. 8, when HEMT is approximately biased at the maximum transconductance point of $V_{GS} = -0.15$ V and $V_{DS} = 2$ V, the extrapolated f_T from H_{21} is 164 GHz and f_{max} based on MAG/MSG is over 390 GHz. However, MSG of 19.6 dB is measured in the instrumentation limit of 40 GHz; at that frequency the device is still potentially unstable ($K < 1$). Extrapolating the gain at −20 dB per decade from this point indicates a larger actual f_{max} than 390 GHz.

The enhanced $g_{m,max}$ by excellent Ohmic contact and short source–drain space, and optimized gate recess process, enable f_{max} of our device to be one of the highest values in the reported 0.15-μm gate-length InP-based HEMTs operating in the millimeter wave frequency range as shown in Table 2.

Improving the comprehensive performances of the millimeter-wave device needs to enhance its amplifying capability. The high f_{max} ensures a sufficient device gain at millimeter-wave frequencies, which is given by

$$G_{max} = 20\log\left(\frac{f_{max}}{f}\right). \quad (1)$$

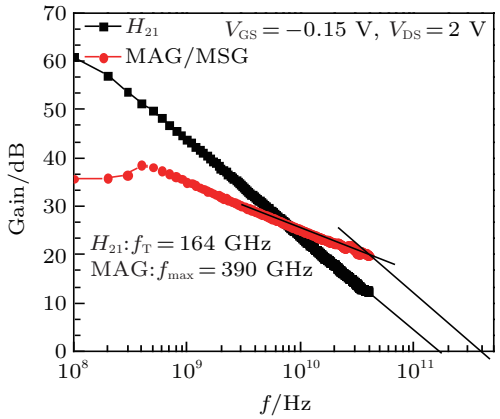


Fig. 8. (color online) Plots of H_{21} and MAG/MSG versus frequency of the 0.15-μm gate-length HEMT.

Table 2. Comparison with published InP HEMT with a gate-length of 150 nm.

Device	L_g/nm	f_T/GHz	f_{max}/GHz	Reference
InP PHEMT	150	165	500	[10]
InP HEMT	150	120	270	[11]
InP PHEMT	150	166	255	[12]
InP E-HEMT	150	151	188	[13]
InP LMHEMT	150	140	–	[14]
InP LMHEMT	150	164	390	this work

Figures 9(a) and 9(b) demonstrate that the variations of f_T with V_{GS} and V_{DS} are different from that of f_{max}. While f_{max} saturates or continues to increase slightly above $V_{DS} = 1.3$ V, f_T reaches its maximum at this bias point. This behavior is expected because f_T and f_{max} are mainly governed by different small signal parameters as shown in the following equations:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})}, \quad (2)$$

$$f_{max} = \frac{f_T}{\sqrt{4g_{ds}(R_i+R_s+R_g)+\frac{2C_{gd}}{C_{gs}}\left(\frac{C_{gd}}{C_{gs}}+g_m(R_i+R_s)\right)}}, \quad (3)$$

where C_{gd} and C_{gs} are the gate–drain capacitance and the gate–source capacitance respectively, g_{ds} is the output conductance, and R_i is the channel resistance. With the increase of V_{DS}, the depletion region of the drain side will expand till being saturated, so C_{gd} would decrease and finally keep constant. On the other side, C_{gs} has less relationship with V_{DS}, and it would increase slowly with the increase of V_{DS}. It can be induced that f_{max} will continue to increase slightly after the device has been saturated at V_{DS} of 1.3 V, however, f_T reaches its maximum value at this bias point.

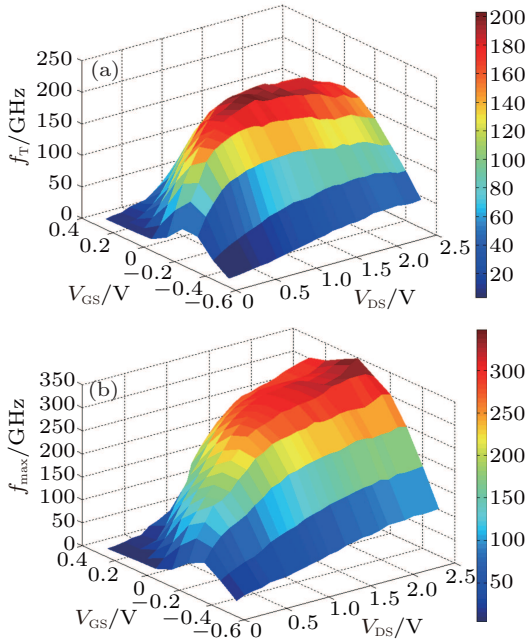


Fig. 9. (color online) Dependences of RF characteristic on V_{GS} and V_{DS}: (a) Dependences of f_T on V_{GS} and V_{DS}. (b) Dependences of f_{max} on V_{GS} and V_{DS}.

4.3. Power performance

An on-wafer load pull test is performed on the 2×50-μm coplanar device. The measurement is restricted by the tuner in a frequency range of 0.8 GHz–18 GHz. The measured output power, power gain and power added efficiency are plotted in Fig. 10, while the device biased at the maximum transconductance point with $V_{GS} = -0.15$ V and $V_{DS} = 2$ V. The highest saturated power, 201 mW/mm, is achieved with a power gain of 17 dB and power added efficiency (PAE) of 42%. To our knowledge, the power gain is one of the highest ever reported in this frequency range for this material system.

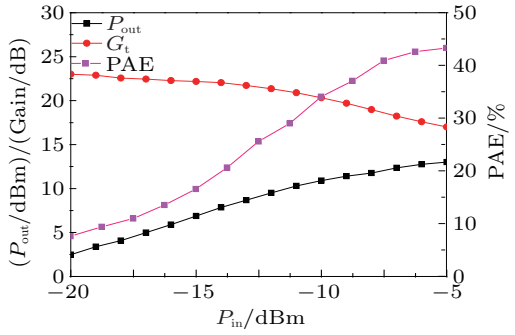


Fig. 10. (color online) Measured P_{in}–P_{out} curves of the HEMT with a 2×50-μm gate-width at 18 GHz, where P_{in} and P_{out} denote input power and output power, respectively.

5. Conclusion

The 0.15-μm gate-length $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ InP-based HEMTs each with an offset T-gate structure are fabricated. Their epitaxial structures are designed and their gate-recess processes are optimized to gain excellent DC and RF performances. The measured full channel current and the extrinsic maximum transconductance are 681 mA/mm and 952 mS/mm, respectively. The off-state gate-to-drain breakdown voltage defined at a gate current of -1 mA/mm is 2.85 V. The values f_T and f_{max} of the HEMTs are 164 GHz and 390 GHz respectively. The value of f_{max} measured from our devices is one of the best performances reported in the 0.15-μm gate-length lattice-matched InP-based HEMTs operating in the millimeter wave frequency range.

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References

[1] Zhang X F, Wang L, Liu J, Wei L and Xu J 2013 *Chin. Phys. B* **22** 017202
[2] Li D L and Zeng Y P 2006 *Chin. Phys. B* **15** 2735
[3] Kong X, Wei K, Liu G G and Liu X Y 2012 *Chin. Phys. Lett.* **29** 078502
[4] Kong X, Wei K, Liu G G and Liu X Y 2012 *Chin. Phys. B* **21** 128501
[5] Kim D H and del Alamo J A 2008 *IEEE Electron Dev. Lett.* **29** 830
[6] Lai R, Mei X B, Deal W R, Yoshida W, Kim Y M, Liu P H, Lee J, Uyeda J, Radisic V, Lang M, Gaier T, Samoska L and Fung A 2007 *IEEE International Electron Devices Meeting*, December 10–12, 2007, Washington, DC, USA, p. 609
[7] Somerville M H, Ernst A and del Alamo J A 2000 *IEEE Trans. Electron Dev.* **47** 922
[8] Zhong Y H, Wang X T, Su Y B, Cao Y X, Jin Z, Zhang Y M and Liu X Y 2012 *J. Semicond.* **33** 054007
[9] Bahl S R and del Alamo J A 1993 *IEEE Trans. Electron Dev.* **40** 1558
[10] Chertouk M, Dammann M, Köhler K and Weimann G 2000 *IEEE Electron Dev. Lett.* **21** 97
[11] Boudrissa M, Delos E, Wallaert X, Thbron D and De Jaeger J C 2001 *International Conference on Indium Phosphide and Related Materials Conference Proceedings*, May 14–18, 2001, Nara, Japan, p. 196
[12] Yoon H S, Lee J H, Shin J Y, Hong J Y, Kang D M, Kim H C, Lee K H and Kim B W 2004 *J. Korean Phys. Soc.* **45** S594
[13] Kim S and Adesida I 2006 *IEEE Electron Dev. Lett.* **27** 873
[14] Mei X B, Farkas D, Luo W B, Lin C H, Lee L J, Liu W, Liu P H, Cavus A and Lai R 2009 *IEEE International Conference on Indium Phosphide & Related Materials*, May 10–14, 2009, Newport Beach, CA, USA, p. 204