Effects of NPB anode buffer layer on charge collection in ZnO/MEH-PPV hybrid solar cells*

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(Received 24 July 2013; revised manuscript received 19 August 2013)

We investigate the effects of (N,N'-diphenyl)-N,N'-bis(1-naphthyl)-1,1'-biphenyl-4,4'-diamine (NPB) buffer layers on charge collection in inverted ZnO/MEH-PPV hybrid devices. The insertion of a 3-nm NPB thin layer enhances the efficiency of charge collection by improving charge transport and reducing the interface energy barrier, resulting in better device performances. S-shaped light *J*–*V* curve appears when the thickness of the NPB layer reaches 25 nm, which is induced by the inefficient charge extraction from MEH-PPV to Ag. Capacitance–voltage measurements are performed to further investigate the influence of the NPB layer on charge collection from both simulations and experiments.

Keywords: NPB, capacitance–voltage measurement, charge collection, buffer layer

PACS: 84.60.Jt, 84.37.+q, 82.45.Mp **DOI:** 10.1088/1674-1056/22/12/128402

1. Introduction

The interface engineering between active layer and electrode has been carried out to improve device charge extraction. In order to modify the interface between the active layer and electrodes, many buffer layers have been reported, such as LiF,[1–3] MoO_3,[4–6] WO_3,[7,8] V_2O_5,[9] Alq_3,[10] BCP,[11] and $CsCO_3$[12,13] to improve the device performances. Understanding the physics of buffer layers on charge transport in photovoltaic devices is necessary to improve their properties. (N,N'-diphenyl)-N,N'-bis(1-naphthyl)-1,1'-biphenyl-4,4'-diamine (NPB) has been widely used as a hole-transporting layer in organic light-emitting diodes,[14–16] however, it is seldom used in solar cells. NPB would be a candidate anode buffer material with many of the same functions as that which the MoO_3 has.

The current density–voltage (*J*–*V*) scan is a widely used tool to characterize photovoltaic device performances. However, *J*–*V* curves provide limited information for the analysis of the device charge transport mechanism. Capacitances relate to electronic carrier accumulation in the device, which would be a direct way to describe charge collection properties. Capacitance and admittance spectroscopies were used to analyze charge transport in organic semiconductor devices.[17–19] The charge accumulation effect was studied experimentally by the capacitance–voltage (*C*–*V*) measurement in planar bilayer heterojunction organic solar cells.[20]

In this article, we focus on the study of NPB serving as an anode buffer layer in a ZnO/MEH-PPV (poly(2-methoxy-5-(2-ethylhexyloxy)-1,4-phenylenevinylene)) hybrid solar cell and investigate its effect on charge collection by capacitance–voltage measurements. We perform *C*–*V* simulations by using the software SCAPS[21–23] and compare the simulations with experimental results in the device of ITO/ZnO/MEH-PPV/NPB(0, 3, 5, 10, 25 nm)/Ag. The 3-nm NPB buffer layer improves device hole transport and reduces the energy barrier of the MEH-PPV/Ag interface so as to facilitate the charge collection. However, an S-shaped light *J*–*V* curve appears when the thickness of the NPB layer reaches 25 nm, which is induced by the inefficient charge extraction from MEH-PPV to Ag. It is demonstrated that the device capacitances are smaller with more efficient charge collections in the bias region of reverse and before the peak position of maximum capacitance (V_{Cmax}) under illumination.

2. Experiment

All the devices were fabricated on indium tin oxide (ITO) pre-coated glass substrates. The patterned ITO substrates were cleaned using acetone, ethanol, and deionized water sequentially and dried by nitrogen. A thin seed layer was deposited by spin-coating zinc acetate dehydrate solution at 3000 rpm and baked at 360 °C for 20 min in an atmospheric environment. ZnO nanorods were grown by the hydrothermal method. A precursor solution was prepared by mixing zinc nitrate hexahydrate ($Zn(NO_3)_2{\cdot}6H_2O$) and hexamethylenetri-

*Project supported by the National Basic Research Program of China (Grant No. 2010CB327704), the National Natural Science Foundation of China (Grant No. 51272022), the Program for New Century Excellent Talents in University of Ministry of Education of China (Grant No. NCET-10-0220), the Research Fund for the Doctoral Program of Higher Education, China (Grant No. 20120009130005), and the Fundamental Research Funds for the Central Universities, China (Grant No. 2012JBZ001).

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amine ($C_6H_{12}N_4$) in distilled water, which were magnetically stirred at room temperature and finally both reached a concentration of 0.025 mol/L. Then the ITO substrates with the seed layer were placed vertically in the precursor solution and maintained at 92 °C for 15 min. Subsequently, all the samples were cleaned with ethanol and deionized water repeatedly, then baked at 400 °C for 30 min in atmospheric environment. A 5-mg/ml solution of MEH-PPV in chlorobenzene was spin-coated at 1000 rpm on the prefabricated ZnO nanorods, then annealed at 80 °C for 15 min. NPB layers were deposited by thermal evaporation under 3×10^{-4} Pa. Finally, a 50-nm thick Ag was deposited on all the devices.

The current density–voltage characteristics were measured using a Keithley 4200-SCS Source Measure Unit GPIB-interfaced to a computer. A solar simulator (ABET Sun 2000) with an AM 1.5 G output of 100 mW/cm^2 was used for the light *J*–*V* measurements. The capacitance–voltage was measured using a Keithley 4200-SCS with a *C*–*V* unit. All of the *C*–*V* scans were performed at 2 kHz.

3. Results and discussion

The device structure is shown in Fig. 1 and the morphologies of the prepared ZnO nanorods are characterized in our previous study.[24]

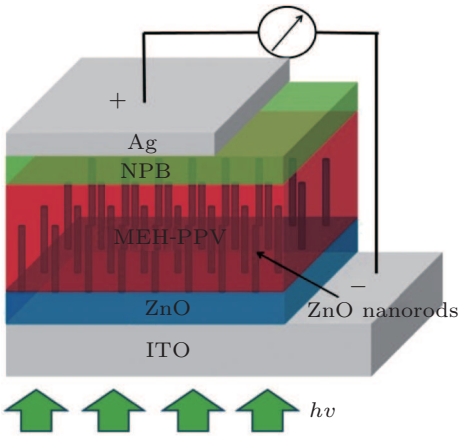


Fig. 1. (color online) Structures of hybrid solar cell devices with different NPB thicknesses: ITO/ZnO/MEH-PPV/NPB(0, 3, 5, 10, 25 nm)/Ag.

3.1. *J*–*V* properties

The inverted configurations of ITO/ZnO/MEH-PPV/NPB(0, 3, 5, 10, 25 nm)/Ag were used to investigate the influences of NPB on the photovoltaic properties of the devices. The current density–voltage curves of the devices with different thickness values of NPB buffer layers are shown in Fig. 2. The device without NPB modification produces large reverse leakage currents under dark and illumination respectively. This is because some of the ZnO nanorods are not fully covered by MEH-PPV, thereby resulting in the direct contact between a few ZnO nanorods and the top electrode Ag. After modifying the NPB, the reverse leakage currents are significantly suppressed, which is attributed to the isolation between ZnO and Ag by the inserting of NPB. The dark forward current decreases with the increasing of the thickness of the NPB layer, which is probably due to the increased resistance of NPB. It is noticed that when the thickness of NPB reaches 25 nm, the dark forward current becomes very small which implies that too large resistances and bad charge injection from Ag to the device occur.

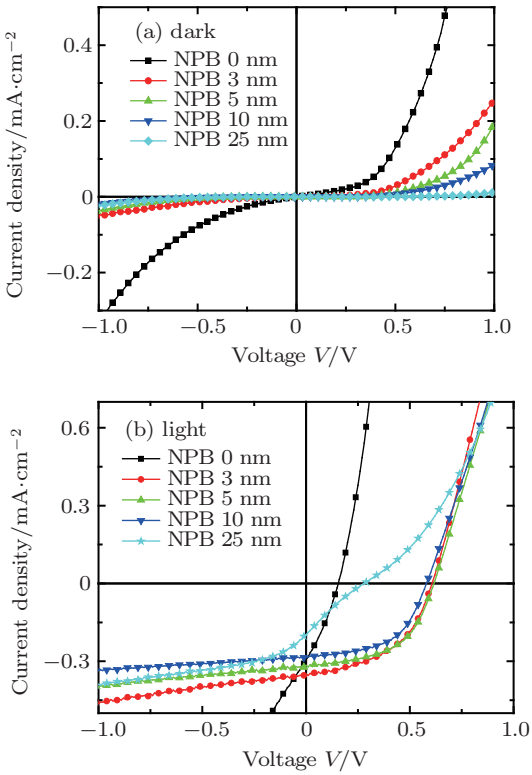


Fig. 2. (color online) Device current density–voltage curves under (a) dark and (b) light with different NPB thicknesses. Device structures are ITO/ZnO/MEH-PPV/NPB(0, 3, 5, 10, 25 nm)/Ag.

The device without NPB modification is shunted as it can be seen in Fig. 2(b) (square symbol line) that the leakage currents are very large. The leakage currents under illumination are suppressed and the *J*–*V* curve becomes relatively flat in the reverse bias region after inserting the NPB layers. Furthermore, the open-circuit voltages (V_{oc}) are significantly enhanced by NPB thin layers. Compared with the unmodified device, 3–10-nm NPB modified devices produce high V_{oc}, which can be expected according to the Shockley equation as a consequence of reduced leakage currents.[25,26] The forming of a tunneling junction to increase the built-in voltage (V_{bi}), or an interfacial dipole layer to shift the work function of electrodes is considered as an underlying reason.[27–29]

An S-shaped light *J*–*V* curve appears when the thickness of the NPB layer reaches 25 nm. The photo-generated charges can be relatively easy to collect from MEH-PPV to Ag within the 3 nm–10 nm thick NPB layers. However, the

photo-generated charges cannot be efficiently collected by Ag, but they can either accumulate at the interface between NPB and MEH-PPV or recombine in the device in the case of the too thick NPB layer. Such a thick NPB layer causes charge to accumulate or recombine in the device, thereby obstructing the charge collection and leading to an S-shaped light J–V curve.

3.2. Capacitance–voltage characteristics

Capacitance–voltage measurements were performed under 100-mW/cm^2 illuminations to further investigate the effects of different thickness values of the NPB layers on charge collection. The device capacitance under illumination is depicted by the differential capacitance per unit area

$$C = \frac{\mathrm{d}Q}{\mathrm{d}V}, \tag{1}$$

where Q is the electric charge.

Applied voltage will affect the transport and extraction of photo-generated carriers, and therefore influences the values of capacitance in our measurements. The fewer charges accumulate in the device, the smaller capacitances are generated according to Eq. (1). The C–V curve will be relatively low in the reverse bias region if the photo-generated carriers can be effectively collected before being recombined. The parameters that influence the values of capacitance were analyzed from charge carrier mobilities and charge collection barriers in this paper.

Charge carrier mobilities can largely affect the shapes of J–V and C–V curves. It is reported that imbalanced charge carrier mobilities will cause charge accumulation in the device and even lead to S-shaped J–V curves under illumination.[20,30,31] Many buffer layers such as LiF,[1,2] MoO_3,[4,5] and PFN[25,32,33] were used to modify the electrode in order to facilitate charge collection, for which one of the reasons is that the buffer layers can balance charge transport.[25] Here the NPB buffer layer has the same role in improving the hole transport.

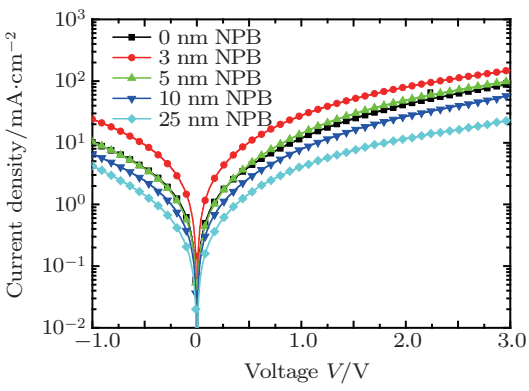


Fig. 3. (color online) Dark J–V curves of the devices ITO/PEDOT:PSS/MEH-PPV/NPB(0, 3, 5, 10, 25 nm)/Ag.

The space charge limited current (SCLC) model is one of the most commonly used methods to measure charge carrier mobility. We did not make a numerical evaluation on the hole mobility through SCLC, but we adopted the hole-only device structure to investigate the influence of the thickness of the NPB layer on the hole transport properties. In order to achieve a hole-only structure in the experiment of hole transport property investigation, PEDOT:PSS was used to transport holes and prevent electrons from transporting in the device. The device structure used in this section is ITO/PEDOT:PSS/MEH-PPV/NPB(0, 3, 5, 10, 25 nm)/Ag. Figure 3 shows the dark J–V curves of the devices with different thickness values of NPB thin layers. It is noticed that the currents of all the devices are almost symmetric in a bias range from −1 V to 1 V, which implies that this structure can be considered to have a hole-only transport in the devices since the currents are nearly the same no matter which electrodes the holes are injected from. The 3-nm NPB modified device produces higher currents than the one without NPB modification. While, with the increase of NPB layer thickness, the currents are decreased which is caused by the large resistance of NPB. The 5-nm NPB modified device almost exhibits the same current as the unmodified one. The currents of the devices with the more-than-5-nm NPB modification are even smaller than those without NPB modification. The enhanced currents after inserting 3-nm NPB in these measurements are caused by the changes of injection barriers and entire device hole transport. The underlying mechanism of the NPB buffer layer is that due to the forming of a tunnelling junction, the built-in electric field is increased or due to the forming of an interfacial dipole layer, the work function of electrodes is shifted. And the increased V_{bi} across the device due to the 3-nm NPB interlayer is conducive to the charge carriers escaping from shallow traps, thereby improving the carrier mobility of the entire device (including active material and buffer layer).[25] Kim *et al.*[34] reported that the devices with four types of PEDOT:PSS buffer layers show different hole mobilities, and emphasized that the mobility value is not for the active layer but for the cell including the active and the buffer layers. Therefore, the 3-nm NPB improves the device hole transport. This hole transport-improved effect is treated as being equivalent to the enhancing of device hole mobility in our simulations here. The influence of injection barriers on capacitance will be investigated sequentially.

Table 1. Parameters used for the simulations.

Parameter	Symbol	Numerical value
Thickness of active layer	L	100 nm
Temperature	T	300 K
Frequency	F	2 kHz
Bandgap	E_{g}	0.8 eV
Relative dielectric permittivity	ε_{r}	3.8
Effective density of states	N_{c}, N_{v}	1×10^{19} cm^{-3}

The effects of the charge carrier mobility on the value of capacitance under illumination were simulated by using the

software SCAPS[21–23] with parameters given in Table 1. Figure 4(a) shows that under illumination at reverse bias, the device with the higher hole mobility exhibits a lower capacitance value which corresponds to better carrier collection of the device.

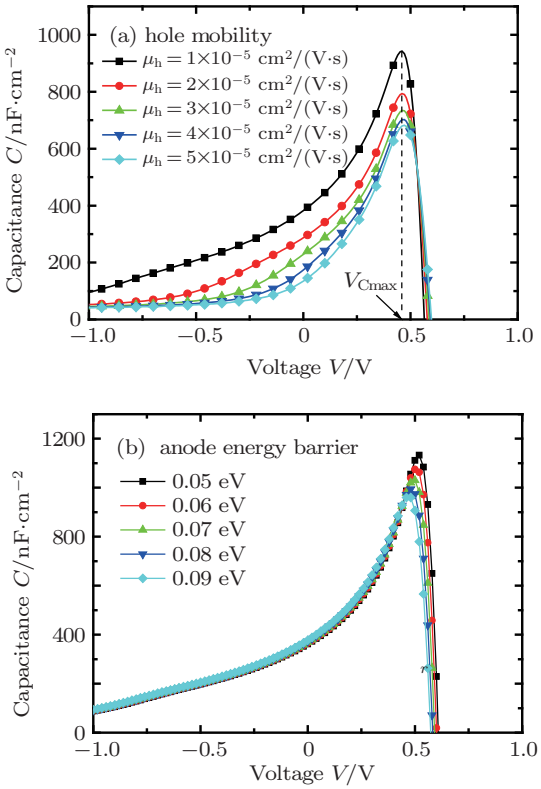


Fig. 4. (color online) Simulated capacitance–voltage curves for a 100-nm thick cell under illumination in the cases where (a) the electron mobility is set to be 1×10^{-4} cm^2/(V·s) and the hole mobility varies from 1×10^{-5} cm^2/(V·s) to 5×10^{-5} cm^2/(V·s), and (b) the cathode energy barrier is fixed to be 0 eV and the anode energy barrier for hole changes from 0.05 eV to 0.09 eV.

The charge collection barrier is another parameter that influences C–V curves. For efficient charge collection, work functions of anode and cathode should be matched to the highest occupied molecular orbit (HOMO) of donor and the lowest unoccupied molecular orbit (LUMO) of acceptor respectively. The work functions of the two electrodes determine the built-in voltage (V_{bi}) of a device. Small V_{bi} will normally lead to a low fill factor (FF) and an even S-shaped J–V curve.[35] The more charges which are extracted out of the device, the smaller capacitances are generated according to Eq. (1). Figure 4(b) illustrates how energy barriers influence the capacitance voltage curves by fixing the cathode energy barrier to be 0 eV and varying the anode energy barriers from 0.05 eV to 0.09 eV. Figure 5 illustrates the meanings of the parameters used in simulation. The anode energy barriers are changed through varying the anode work functions. It is seen that in the bias region of reverse and before max capacitance peak position (V_{Cmax}), the capacitances of the devices with higher V_{bi} are slightly lower than the ones with lower V_{bi}, which is due to the fact that the photo-generated charge carriers can be more efficiently collected. The peak positions of the C–V curves are different. A recent study found that there is no offset between the V_{oc} and the peak position of maximum capacitance in several polymeric bulk heterojunction devices.[36]

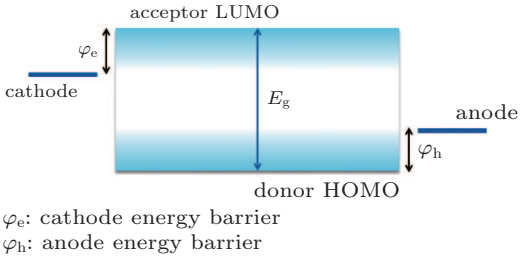


Fig. 5. (color online) Band diagram of the inverted organic solar cell used in simulation.

Experimental results of the capacitance–voltage measurements under illumination are shown in Fig. 6(a). The device structure used in C–V measurements is the same as that used in J–V measurements. In the bias region of reverse and before V_{Cmax}, the capacitance of device with 3-nm NPB modification is smaller than the one without NPB modification, which implies more effective charge carrier collection in the former. This is in consistence with the results from Eq. (1) and simulations, the more charges extracted out of the device, the smaller the generated capacitance is. The improved charge collection by 3-nm NPB can be explained from two aspects: (i) 3-nm NPB layer improves the energy matching between Ag and MEH-PPV to facilitate the charge collection; (ii) 3-nm NPB layer improves the charge carrier transport of the device. Figure 6(b) shows how these two aspects influence the capacitances by simultaneously reducing charge collection barriers and increasing hole mobilities. When simultaneously reducing the charge collection barrier and increasing the hole mobilities, the capacitances of the device with 3-nm NPB are smaller than those of the unmodified device, which is consistent with our experimental result. From the C–V measurement we conclude that reducing the collection barrier and increasing the hole transport property by 3-nm NPB modification are conducive to charge collection and lead to smaller capacitances under illumination.

However, the capacitances under illumination are small, and the C–V curve is relatively flat in the whole bias range when the thickness of NPB increases to 25 nm, which means that just very little charges accumulated in the device. As analyzed previously, the hole transport property of the device with 25-nm NPB is poorest and simulations show that the capacitances should be larger than those of any other devices discussed in this paper. This phenomenon of small capacitance but with poor hole transport property can be explained by the process of charge recombination. The uncollected photo-generated charges can accumulate in the device if the charge

recombination mechanism is not dominant. Besides the efficient charge collection, the quantity of charges in a device can also be quite low when the recombination mechanism dominates, thereby resulting in a small capacitance value.

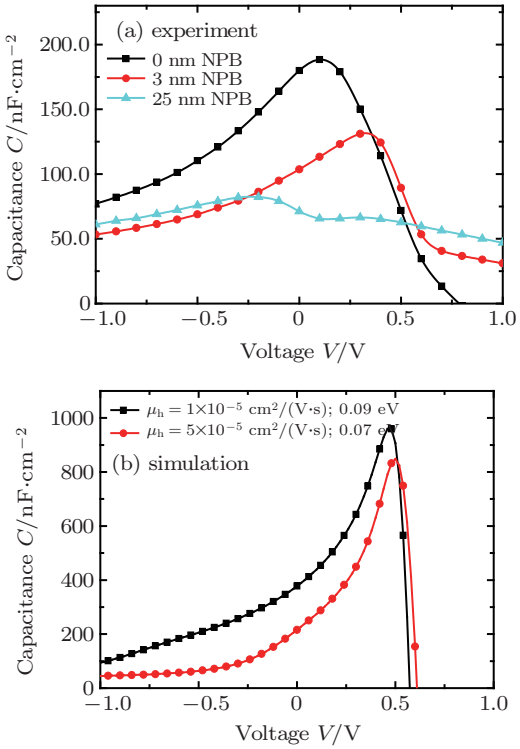


Fig. 6. (color online) Measured (a) and simulated (b) capacitance–voltage curves of the device with 3-, 25-nm NPB and without NPB modification under illumination. All the measurements were performed at 2 kHz. In simulation, the hole mobility and anode energy barrier of the device without NPB were set to be 1×10^{-5} cm^2/(V·s) and 0.09 eV; the hole mobility and anode energy barrier of the device with 3-nm NPB were set to be 5×10^{-5} cm^2/(V·s) and 0.07 eV.

Figure 7 shows the J_{ph}–V_{eff} curves under illumination and the results are plotted as the net current ($J_{ph} = J_L - J_D$) versus the effective applied voltage ($V_{eff} = V_0 - V$), where J_L and J_D are the current density under illumination and dark respectively, V is the applied voltage, V_0 is the compensation voltage at the place where $J_{ph} = 0$.[37] At $V_{eff} = 1.5$ V, J_{ph} reaches saturation for both devices, suggesting that all photo-generated excitons in each device were dissociated into free carriers and all carriers were collected at the electrodes.[38,39] In the low effective voltage range ($V_{eff} < 0.4$ V), J_{ph} of the device with 25-nm, NPB decreased more than the one with 3-nm NPB, which implies that there is either a reduced exciton dissociation efficiency or charge collection efficiency in the former, with the latter suggesting that bimolecular recombination begins to dominate and usually leads to a lower FF.[25,40] The reduced exciton dissociation and increased bimolecular recombination result in a small quantity of charges accumulated in the device, thereby leading to low capacitance values.

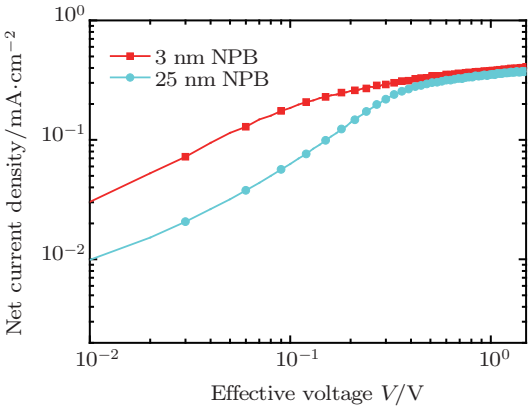


Fig. 7. (color online) Plots of net current density ($J_{ph} = J_L - J_D$) versus effective applied voltage ($V_{eff} = V_0 - V$) of devices with 5-nm (square symbol line) and 25-nm (circle symbol line) NPB modification under illumination.

4. Conclusions

NPB is used to modify the inverted ZnO/MEH-PPV hybrid solar cells. The insertion of 3-nm NPB enhances the efficiency of the charge carrier collection by improving the device hole transport and reducing the interface energy barrier between MEH-PPV/Ag, resulting in higher V_{oc} and FF. The photo-generated charges cannot be efficiently collected by Ag but recombine in the device when the thickness of NPB reaches 25 nm. Capacitance–voltage measurements are performed to analyze the influences of NPB from the aspects of device charge transport and interface energy barriers. Under light illumination and in the bias region of reverse and before V_{Cmax}, the capacitance of the device with a 5-nm NPB buffer layer is smaller than that of the device without an NPB buffer layer, which implies more effective charge carrier collection in the former.

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