High-voltage SOI lateral MOSFET with a dual vertical field plate*

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A new silicon-on-insulator (SOI) power lateral MOSFET with a dual vertical field plate (VFP) in the oxide trench is proposed. The dual VFP modulates the distribution of the electric field in the drift region, which enhances the internal field of the drift region and increases the drift doping concentration of the drift region, resulting in remarkable improvements in breakdown voltage (BV) and specific on-resistance ($R_{on,sp}$). The mechanism of the VFP is analyzed and the characteristics of BV and $R_{on,sp}$ are discussed. It is shown that the BV of the proposed device increases from 389 V of the conventional device to 589 V, and the $R_{on,sp}$ decreases from 366 mΩ·cm^2 to 110 mΩ·cm^2.

Keywords: breakdown voltage, specific on-resistance, vertical field plate, oxide trench

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1. Introduction

For high-voltage metal oxide semiconductor field effect transistors (MOSFETs) in high-voltage power applications, the long drift region, which is essential for obtaining a high breakdown voltage (BV), limits the improvement in the specific on-resistance ($R_{on,sp}$). In order to improve the $R_{on,sp}$ characteristic while maintaining a high BV, the trench technologies are used in the fabrication of power lateral MOSFETs.[1–6] By implanting the oxide trench in the drift region, the power lateral MOSFETs can achieve reduced $R_{on,sp}$ because of the shortened cell pitch.[7–9] A two-dimensional analytical model is then developed to explore the physical mechanism of the oxide trench in the silicon-on-insulator (SOI) trench lateral MOSFETs.[10] On the basis of the trench technology, a trench gate is integrated in the oxide trench to obtain a reduced $R_{on,sp}$.[11–14]

Based on the authors' investigation of high-voltage trench lateral MOSFETs,[15] a novel high-voltage SOI lateral trench MOSFET (DFPT MOSFET) with dual vertical field plate (VFP) is proposed and investigated. In the proposed structure, two VFPs are integrated in the oxide trench and form a dual VFP. The assisted depletion effect of the dual VFP leads to an increased BV and a reduced $R_{on,sp}$ for the DFPT MOSFET. In comparison with the conventional SOI lateral trench MOSFET (CT MOSFET), the tradeoff between BV and $R_{on,sp}$ is therefore improved in the DFPT MOSFET. The characteristics of BV and $R_{on,sp}$ are analyzed by means of the MEDICI TCAD simulator in this paper.

2. Device structure and mechanism

The schematic cross section view of the proposed DFPT MOSFET is depicted in Fig. 1. The oxide trench is formed between the source and the drain to sustain the BV. The two VFPs in the oxide trench are connected with the gate and the drain contacts, respectively. Here w_T and t_T are the width and depth of the oxide trench, respectively; t_{PF} is the depth of the dual VFP; w_{PF} is the width of the oxide between the VFP and the drift region; t_S and N_d are the thickness and doping concentration of the SOI layer, respectively; and t_I is the thickness of the buried oxide layer. Figure 1 shows the x and y directions in simulation. The results are obtained by using the two-dimensional device simulator MEDICI. The physical models of IMPACT. I, CCSMOB, AUGER, FLDMOB, CONSRH, and BGN are mainly used in the simulation. The NEWTON solution method is carried out with two types of carriers and the parameters of ITLIMIT = 30 and STACK = 15.

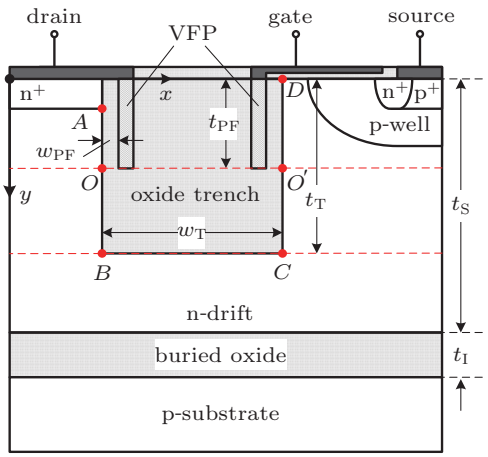


Fig. 1. (color online) Schematic cross section of DFPT MOSFET.

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In the proposed DFPT MOSFET, the VFP, the oxide, and the n-drift region compose a metal–insulator–semiconductor (MIS) structure. It helps to deplete the drift region in the off-state. Two electric field peaks are introduced in the drift region due to the assisted depletion effect of the dual VFP, resulting in an enhancement of the average electric field strength in the drift region and hence improves the BV of the DFPT MOSFET. Moreover, the assisted depletion effect of the dual VFP also increases N_d when the DFPT MOSFET achieves the maximum BV. Owing to the increased N_d, the resistance of the drift region is reduced and thus decreases $R_{on,sp}$ in the on-state.

3. Simulation results and discussion

Figure 2 shows the equipotential contours at breakdown for a DFPT MOSFET (see Fig. 2(a)) and a CT MOSFET (see Fig. 2(b)). By comparing Fig. 2(a) with Fig. 2(b), the enhancement and reshaping effects of the dual VFP can be clearly observed. Since the two VFPs are respectively connected with the gate contact and the drain contact, the equipotential lines cannot pass through the VFPs. In the oxide trench of the DFPT MOSFET, as shown in Fig. 2(a), the equipotential lines are sandwiched between the two VFPs and have to cross from the ends of the two VFPs. The distribution of the equipotential lines in the drift region is therefore reshaped. Compared with the CT MOSFET, a more uniform equipotential line distribution is obtained for the DFPT MOSFET, resulting that the BV is increased by 51.4%.

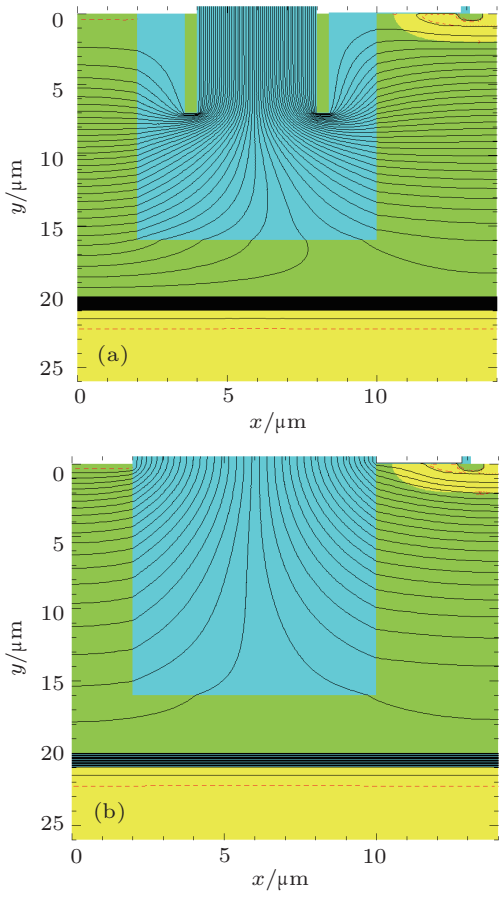


Fig. 2. (color online) Equipotential contours at breakdown for (a) DFPT MOSFET (589 V) and (b) CT MOSFET (389 V). Here N_d is optimized to obtain the maximum BV for each device ($t_S = 20$ μm, $t_I = 1$ μm, $w_T = 8$ μm, $t_T = 16$ μm, $w_{PF} = 1.6$ μm, $t_{PF} = 7$ μm; 10 V/contour).

Figure 3 shows the influences of V_d on the electric field distribution around the oxide trench for the DFPT MOSFET (see Fig. 3(a)) and the CT MOSFET (see Fig. 3(b)) in the off-state. With the increase in V_d, as shown in Fig. 3, the depletion region is gradually extended from the source side (near the D point) to the drain side (near the A point) in the drift region. The drift region is fully depleted when the breakdown occurs. For the CT MOSFET, the breakdown occurs at the surface because of the high electric field peaks near the source and the drain. The low average field strength in the drift region leads to a low BV of 389 V. By comparing Fig. 3(a) with Fig. 3(b), it can be observed that two electric field peaks are generated near the O and O' points for the proposed DFPT MOSFET owing to the dual VFP. The two field peaks lower the surface field peaks and enhance the electric field strength in the drift region, resulting that the BV of the DFPT MOSFET increases from 389 V for the CT MOSFET to 589 V.

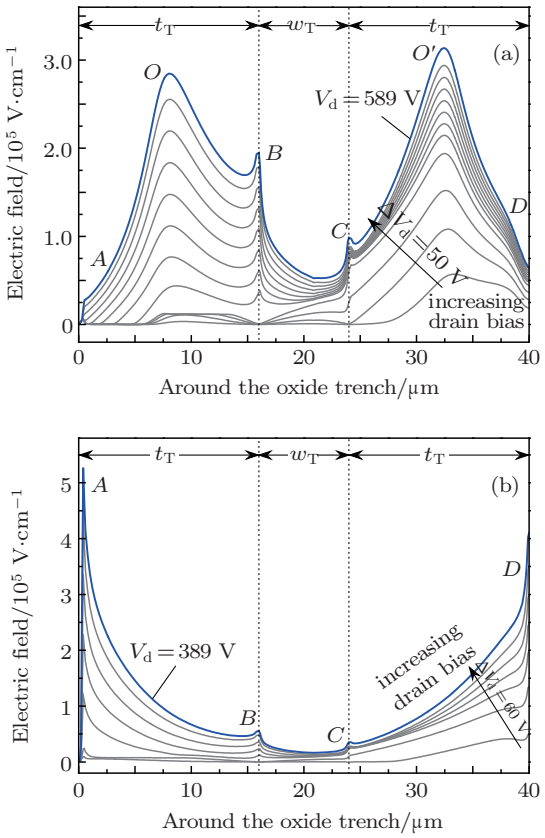


Fig. 3. (color online) Influences of V_d on electric field distribution for (a) DFPT MOSFET and (b) CT MOSFET. The electric field distributions are obtained along the *ABCD* line shown in Fig. 1. The structure parameters are the same as those in Fig. 2.

Figure 4 shows the lateral electric fields along a line of surface (see Fig. 4(a)), $y = 7$ μm (OO' line in Fig. 1) (see

Fig. 4(b)), and $y = 16$ μm (*BC* line in Fig. 1) (see Fig. 4(c)) for the DFPT MOSFET and the CT MOSFET. In Fig. 4(a), the high electric field is distributed between the two VFPs in the DFPT MOSFET. Although the voltage sustaining region is narrowed at the surface for the DFPT MOSFET, the field strength is much higher than that of the CT MOSFET. Compared with the CT MOSFET with the same V_d of 389 V, the field strength in the middle of the oxide trench ($x = 6$ μm) increases from 4×10^5 V/cm to 9.7×10^5 V/cm for the DFPT MOSFET, as illustrated in Fig. 4(a). With V_d further increased to 589 V, the field strength between the VFPs increases to 1.5×10^6 V/cm. Meanwhile, the internal electric field of the SOI layer is also increased by the dual VFP. As shown in Fig. 4(b), for the CT MOSFET, the field strength in the oxide trench is only 1.7×10^5 V/cm at $V_d = 389$ V. However the field strength in the middle of the oxide trench ($x = 6$ μm) is increased to 8×10^5 V/cm at $V_d = 389$ V and 1.2×10^6 V/cm at $V_d = 589$ V for the DFPT MOSFET. Compared with the CT MOSFET in Fig. 4(c), the internal field strength of the drift region is obviously enhanced for the DFPT MOSFET.

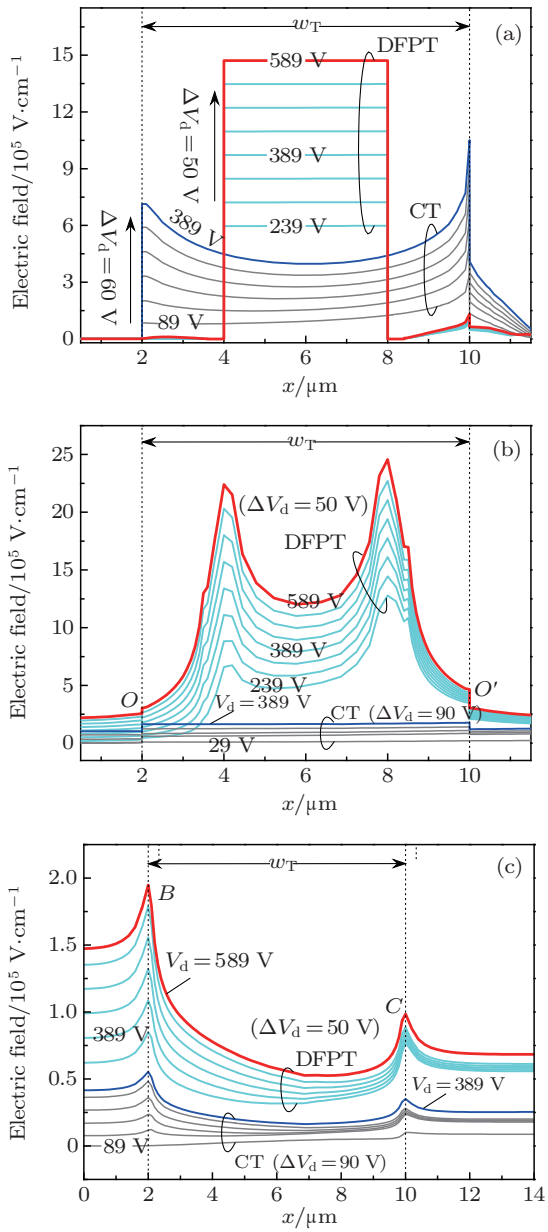


Fig. 4. (color online) Influences of V_d on electric field distribution along (a) the surface ($y = 0$ μm), (b) the *OO*′ line ($y = 7$ μm), and (c) the *BC* line in Fig. 1 ($y = 16$ μm), with the same structure parameters as those in Fig. 2.

A detailed investigation indicates that the voltage drop sustained by the buried oxide, V_I, remains unchanged in the proposed DFPT MOSFET while t_I increases. Figure 5 shows the hole concentration and electric field distributions along the y direction at breakdown. When the breakdown occurs in the DFPT MOSFET, an inversion layer is formed at the bottom of the n-drift region. It can be observed from Fig. 5 that the hole concentration in the inversion layer decreases as t_I increases. In the inversion layer, the maximum hole concentration of 4.1×10^{19} cm^{-3} is obtained at $t_I = 1$ μm, while it decreases to 3.5×10^{18} cm^{-3} at $t_I = 4$ μm. Moreover, the electric field strength at the bottom of the n-drift region, E_S, decreases from 3×10^5 V/cm to 1.8×10^5 V/cm with t_I increasing from 1 μm to 4 μm. Based on Gauss's law, the field strength in the buried oxide, E_I, can be approximately written as

$$E_I = (\varepsilon_S E_S + qQ_P)/\varepsilon_I, \tag{1}$$

where Q_P is the inversion hole density, q denotes the electronic charge, and ε_S and ε_I are the permittivities of Si and SiO_2, respectively. According to Eq. (1), E_I will decrease with t_I increasing. As shown in Fig. 5, E_I decreases from 2.8×10^6 V/cm to 0.7×10^6 V/cm when t_I increases from 1 μm to 4 μm. Since $V_I = t_I E_I$, V_I remains at 280 V no matter how thick the buried oxide is. But E_I should be less than the critical field of SiO_2 to prevent the premature breakdown from occurring in the buried oxide, which will cause the reduction in BV.

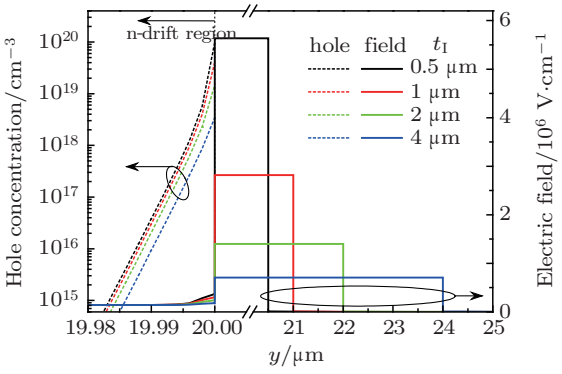


Fig. 5. (color online) Hole concentration and electric field distributions along the y direction ($x = 1$ μm) with different values of t_I. ($t_S = 20$ μm, $w_T = 8$ μm, $t_T = 16$ μm, $w_{PF} = 1.6$ μm, $t_{PF} = 7$ μm.)

The dual VFP not only improves the BV but also increases the optimal N_d ($N_{d,O}$) due to the assisted depletion effect. Figure 6(a) shows the dependence of the BV on N_d for different values of t_{PF}. As shown in this figure, $N_{d,O}$ increases from 3.7×10^{14} cm^{-3} to 9.5×10^{14} cm^{-3} with t_{PF} increasing

from 0 μm (CT MOSFET) to 7 μm. In the on-state, the resistance of the drift region, R_{dr}, can be expressed as

$$R_{dr} = \frac{L_{d,eff}}{qN_d\mu_n W t_{d,eff}}, \tag{2}$$

where W, $L_{d,eff}$, and $t_{d,eff}$ are the width, the effective length, and the effective thickness of the drift region, respectively; and μ_n is the electron mobility in the drift region. Since the total resistance of a device can be simply split into drift (R_{dr}) and channel (R_{ch}) resistance components, $R_{on,sp}$ can be written as

$$R_{on,sp} = LW\left(R_{dr} + R_{ch}\right), \tag{3}$$

where L is the length of the device in the x direction. In the DFPT MOSFET and the CT MOSFET, the oxide trench folds the drift region, which helps to result in reduced L and $R_{on,sp}$ in comparison with the conventional MOSFET without an oxide trench. Since R_{dr} is more than 90% of $R_{on,sp}$ for a 600 V class MOSFET, the $R_{on,sp}$ of a DFPT MOSFET is mainly determined by R_{dr}. According to Eq. (2), the increased $N_{d,O}$ will result in the reduction in R_{dr}, and consequently, $R_{on,sp}$ is reduced for the DFPT MOSFET. The output characteristics of DFPT MOSFETs and CT MOSFETs are compared in Fig. 6(b). The reduced R_{dr} of DFPT MOSFETs leads to an improvement in the drain current. For the DFPT MOSFET with $V_{ds} = 3$ V and $V_{gs} = 5$ V, the drain current of 3.7 mA/mm is achieved, while that of the CT MOSFET is only 1.2 mA/mm. The current flowline contours at $V_{ds} = 1$ V and $V_{gs} = 5$ V for DFPT MOSFET and CT MOSFET are shown in Figs. 6(c) and 6(d), respectively. It is clear that the drain current for the DFPT MOSFET is increased to 1.3 mA/mm from 0.4 mA/mm of the CT MOSFET. The $R_{on,sp}$ of 110 mΩ·cm^2 is therefore obtained for the DFPT MOSFET at $V_{gs} = 5$ V, which is reduced by 69.9% in comparison with 366 mΩ·cm^2 for the CT MOSFET.

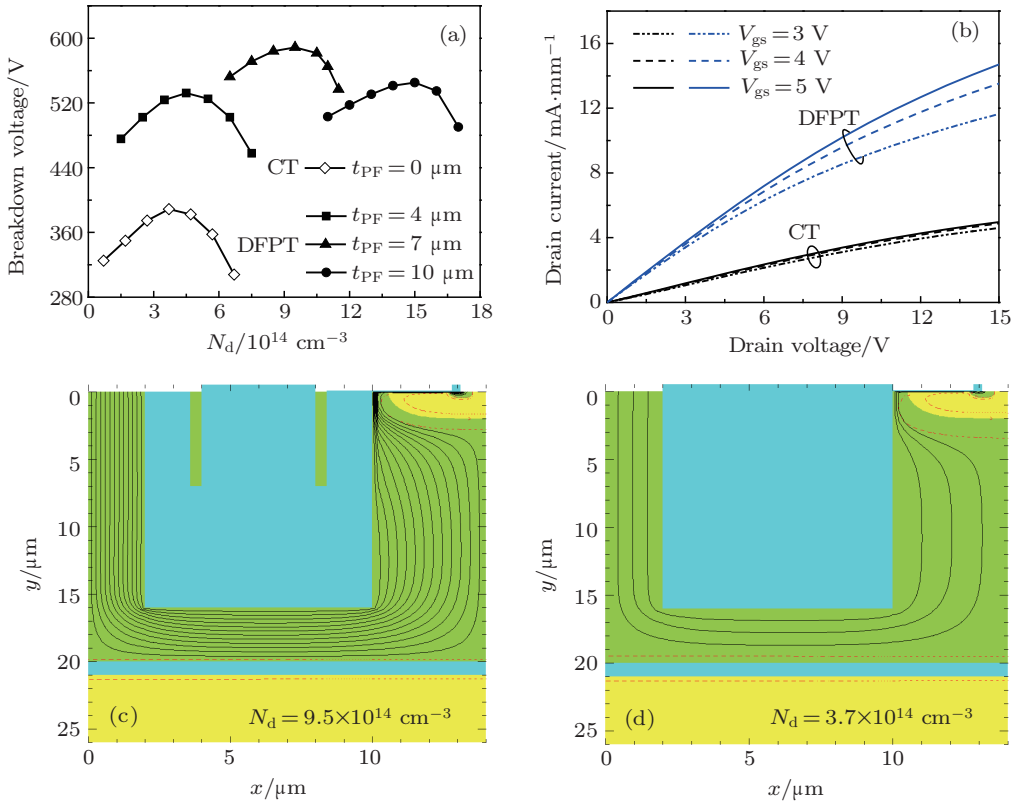


Fig. 6. (color online) (a) Dependence of BV on N_d and (b) transfer characteristic curves of I_{ds}–V_{ds} for DFPT MOSFETs and CT MOSFETs. Current flowline contours for (c) a DFPT MOSFET ($I_{ds} = 1.3$ mA/mm) and (d) a CT MOSFET ($I_{ds} = 0.4$ mA/mm). ($t_S = 20$ μm, $t_I = 1$ μm, $w_T = 8$ μm, $t_T = 16$ μm, $w_{PF} = 1.6$ μm. $t_{PF} = 7$ μm is used for the DFPT MOSFETs in panels (b) and (c). 0.1 mA·mm^{-1}/contour in panels (c) and (d).)

The influence of t_{PF} on the electric field distribution is shown in Fig. 7. It can be observed from Fig. 7 that the two electric field peaks generated near the O and O' points move toward the bottom of the oxide trench with t_{PF} increasing. Although the electric field along the $OBCO'$ line (in Fig. 1) is enhanced, the electric field near the surface is lowered. As a result, the BV first increases and then decreases with t_{PF} increasing from 4 μm to 10 μm. The highest average electric field is thus obtained at $t_{PF} = 7$ μm and the maximum BV of 589 V is obtained for DFPT MOSFETs, as illustrated by Fig. 7.

Figure 8 shows the influences of t_{PF} and w_{PF} on the BV and $R_{on,sp}$. Owing to the reshaping effect of the dual VFP, as mentioned in Fig. 7, the BV first increases from 389 V

to 589 V with t_{PF} increasing from 0 μm (CT MOSFET) to 7 μm, and then decreases to 545 V with t_{PF} further increasing to 10 μm. The $N_{d,O}$ is also influenced by the reshaping effect of the dual VFP. Owing to the increased $N_{d,O}$, $R_{on,sp}$ is thus reduced from 366 mΩ·cm^2 at $t_{PF} = 0$ μm (CT MOSFET) to 73 mΩ·cm^2 at $t_{PF} = 10$ μm, as shown in Fig. 8(a). In Fig. 8(b), the BV decreases as w_{PF} decreases due to the premature breakdown at the O and O' points. Although more and more electrons are accumulated beside the gate field plate, $R_{on,sp}$ still increases with decreasing w_{PF} at $w_{PF} \leq 1.4$ μm because of the reduced $N_{d,O}$. With w_{PF} increasing from 1.4 μm to 2 μm, $R_{on,sp}$ is also increased due to the reduced $N_{d,O}$, and thus the lowest $R_{on,sp}$ of 108 mΩ·cm^2 is obtained at $w_{PF} =$ 1.4 μm. According to Figs. 8(a) and 8(b), the optimal ranges of 7 μm $\leq t_{PF} \leq$ 10 μm and 1.2 μm $\leq w_{PF} \leq$ 1.8 μm are obtained for the DFPT MOSFETs with $t_S = 20$ μm, $w_T = 8$ μm, and $t_T = 16$ μm.

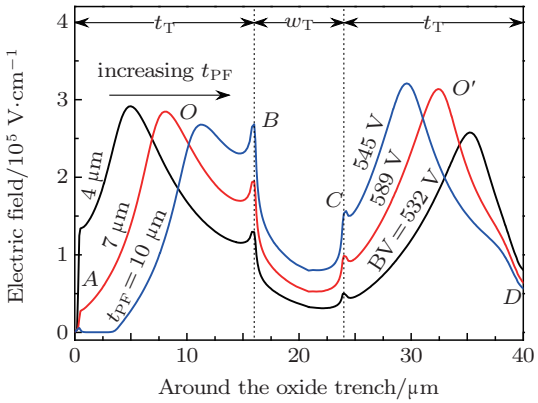


Fig. 7. (color online) Electric field distributions around the oxide trench for different values of t_{PF}. ($t_S = 20$ μm, $t_I = 1$ μm, $w_T = 8$ μm, $t_T = 16$ μm, $w_{PF} = 1.6$ μm. N_d is optimized to obtain the maximum BV for each t_{PF}.)

The dependencies of the BV and $R_{on,sp}$ on t_T and w_T for DFPT MOSFETs and CT MOSFETs are illustrated in Fig. 9. It is clear that the effective length of the drift region is lengthened when t_T and w_T increase, which results in the improvement in BV. It is easy to observe from Figs. 9(a) and 9(b) that the BV is enhanced by the increased t_T and w_T for both DFPT MOSFETs and CT MOSFETs. However, with t_T increasing from 10 μm to 16 μm, the BV of DFPT MOSFETs increases from 477 V to 589 V, while it just increases from 379 V to 389 V in the CT MOSFETs. Although the increasing t_T helps to increase the BV, $R_{on,sp}$ increases dramatically as t_T increases at $t_T \geq 16$ μm due to the narrowed conduction path under the oxide trench, as shown in Fig. 9(a). As a result, with the optimal t_T of 16 μm, the lowest $R_{on,sp}$ of 110 mΩ·cm^2 is obtained for DFPT MOSFETs and the $R_{on,sp}$ of 366 mΩ·cm^2 is achieved for CT MOSFETs. Moreover, $R_{on,sp}$ is increased by increasing w_T because of the increased length of the MOSFET.

The optimal results for DFPT MOSFETs and CT MOSFETs are summarized in Table 1. For a CT MOSFET with $w_T = 8$ μm and $t_T = 16$ μm, BV of 389 V and $R_{on,sp}$ of 366 mΩ·cm^2 are obtained. With the same structure parameters, the BV is increased to 589 V and $R_{on,sp}$ is decreased to 110 mΩ·cm^2 for DFPT MOSFETs owing to the dual VFP. Compared with the CT MOSFETs, the BV of the DFPT MOSFETs is increased by 51.4% and $R_{on,sp}$ is reduced by 69.9%.

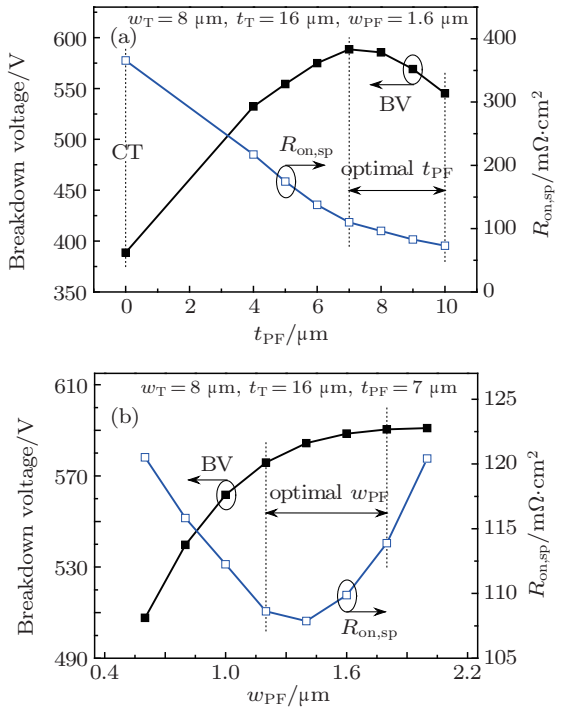


Fig. 8. (color online) Dependences of BV and $R_{on,sp}$ on (a) t_{PF} and (b) w_{PF} for DFPT MOSFETs. ($t_S = 20$ μm, $t_I = 1$ μm, $w_T = 8$ μm, $t_T = 16$ μm.)

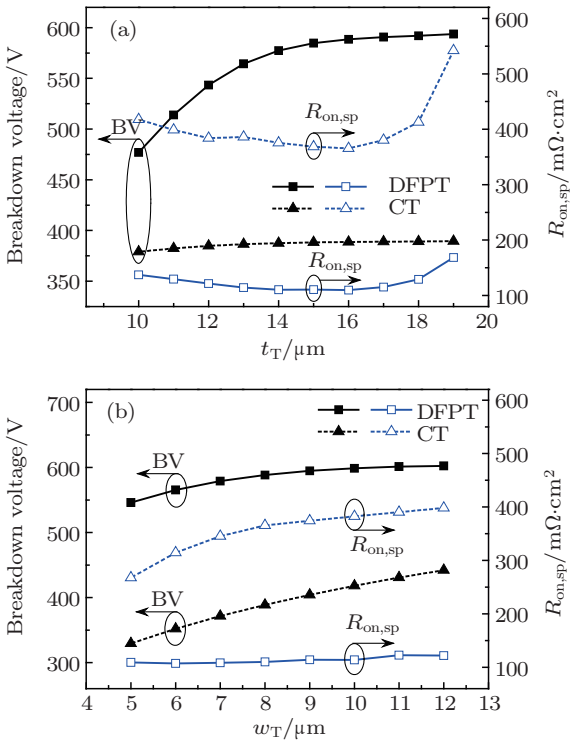


Fig. 9. (color online) Dependences of BV and $R_{on,sp}$ on (a) t_T and (b) w_T for DFPT MOSFETs and CT MOSFETs. ($t_S = 20$ μm, $t_I = 1$ μm, $w_{PF} = 1.6$ μm, $t_{PF} = 7$ μm.)

Table 1. Optimal results for DFPT MOSFETs and CT MOSFETs ($t_S = 20$ μm, $t_I = 1$ μm).

Device parameter	DFPT MOSFET	CT MOSFET
Width of the oxide trench, w_T/μm	8	8
Depth of the oxide trench, t_T/μm	16	16
Width of the oxide between the VFP and the drift region, w_{PF}/μm	1.6	–
Depth of the dual VFP, t_{PF}/μm	7	–
Doping concentration of the n-drift region, $N_d/10^{14}$ cm^{-3}	9.5	3.7
Breakdown voltage, BV/V	589	389
Specific on-resistance, $R_{on,sp}$/mΩ·cm^2	110	366

4. Conclusion

A novel high voltage SOI lateral MOSFET has been proposed and investigated by simulation. The vertical field plate technology is used in the proposed high voltage MOSFET to improve the characteristics of breakdown voltage and specific on-resistance. The assisted depletion effect caused by the dual VFP enhances the internal electric field of the drift region and thus increases the BV. Moreover, the optimal N_d is also increased and results in a dramatically reduced $R_{on,sp}$. Consequently, the proposed DFPT MOSFET increases the BV by 51.4% and decreases $R_{on,sp}$ by 69.9% compared with those of the CT MOSFETs.

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