Scaling effects of single-event gate rupture in thin oxides

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The dynamics of the excess carriers generated by incident heavy ions are considered in both SiO_2 and Si substrate. Influences of the initial radius of the charge track, surface potential decrease, external electric field, and the LET value of the incident ion on internal electric field buildup are analyzed separately. Considering the mechanisms of recombination, impact ionization, and bandgap tunneling, models are verified by using published experimental data. Moreover, the scaling effects of single-event gate rupture in thin gate oxides are studied, with the feature size of the MOS device down to 90 nm. The value of the total electric field decreases rapidly along with the decrease of oxide thickness in the first period (12 nm to 3.3 nm), and then increases a little when the gate oxide becomes thinner and thinner (3.3 nm to 1.8 nm).

Keywords: single-event gate rupture (SEGR), heavy ion, thin oxides, TCAD simulation

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1. Introduction

Single-event gate rupture (SEGR) has been studied for years. It is well known that SEGR can initiate permanent damage in power MOSFETs, MOS capacitors, antifuse devices, etc.[1–5] Meanwhile, simulation methods have been used to help understand the underlying mechanism of single-event effects or predict the vulnerability of specified devices.[6–8] These methods can also help to deal with single event gate rupture.[9–11] Empirical models were firstly developed. Wheatley and Titus introduced one based on power MOSFETs, which reflected that $1/E_{CR}$ behaves a linear dependence on LET.[12,13] Furthermore, to take into account the physics resulting in the SEGR, Nicholas *et al.* suggested solving the simplified drift–diffusion equation and the Poisson equation in SiO_2.[14] Whereas, the influence of bandgap tunneling and excess carriers pileup on Si–SiO_2 interface has not been considered. Researchers from Padova University have introduced a three-dimensional (3D) simulation tool to study the SEGR effect in MOS capacitors.[3,4] Therefore, other researchers have studied the SEGR effect in power MOSFETs using simulation tools.[6–8] However, they all focused on the excess holes pileup on the Si–SiO_2 interface and neglected the physical mechanisms within oxides.

In this paper, generation, recombination, transport, etc of excess carriers are considered in both SiO_2 and Si substrate, to better understand the underlying mechanisms and more accurately predict the SEGR threshold. Firstly, the influence of the initial radius of charge track, surface potential decrease, external electric field, and the LET value of an incident ion to internal electric field buildup are analyzed separately. Secondly, besides drift and diffusion, other mechanisms like recombination, impact ionization, and bandgap tunneling are considered too. Then, the models combining these mechanisms together are verified by using experimental data from Ref. [13]. Finally, the scaling effects of SEGR in thin gate oxides are studied, with the feature size of MOS devices down to 90 nm.

2. Models and discussion

DESSIS is a device simulator allowing three-dimensional simulation. Here, it is introduced to simulate the device response of SEGR. Figure 1 presents the cross section of nMOS device model used in this paper.

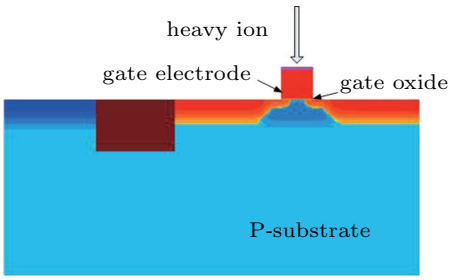


Fig. 1. (color online) Schematic of one nMOS device model.

As an ion strikes the MOS device, a thin passage of electron–hole pairs is created within a short period on the picosecond scale. Early in 1913, Jaffe postulated the initial charge distribution as follows:[15]

$$n(r,0) = \frac{N_0}{\pi b^2} \exp\left(\frac{-r^2}{b^2}\right), \tag{1}$$

where N_0 is the density of charge pairs (proportional to LET), and b is the initial radius of the Gaussian distribution. Jaffe postulated $b \approx 5$ nm for α in SiO_2.[15] After that, Oldham deeply studied the initial charge distribution of incident heavy charged SiO_2 particles, and made the conclusion that $b \approx$

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3.5 nm for protons in SiO_2.[16] Several researchers have taken the initial radius of single particle tracks in Si to be about 100 nm.[17]

The charge generation rate is assumed to be a Gaussian in time, with the peak being at 6 ps (the strike time). The temporal standard deviation is taken to be 2 ps.

In Fig. 1, the width and length of the gate oxide are both 1 μm, which are bigger than the size of the charge distribution (3.5–100 nm). Since the main purpose of this section is to study the contributions of different mechanisms, the rule or comparative value rather than the precise value would be needed. To ascertain high enough precision, the size of each grid should be sufficiently small compared to the size of the charge track because of the high density of excess carriers in this region. Therefore, the value of b should not be too small in this section, and it is chosen to be 100 nm in calculation, as shown in Figs. 3–7.

Considering the worst case that the ion traverses through the gate region and the substrate (see Fig. 1), the electron–hole pairs will be generated in both of the two regions. For SiO_2, the hole mobility is about 10^{-4} $cm^2/V{\cdot}s$ and the electron mobility is 20 $cm^2/V{\cdot}s$.[18,19] When the gate electrode of the MOS device is biased at positive voltage and the substrate zero or negative voltage, the electron generated in the SiO_2 will be collected by the gate electrode really fast.

First, let us just consider carriers drift and diffusion. Using the Poisson equation as follows:

$$\frac{d^2\psi}{dx^2} = -\frac{q}{\varepsilon_{SiO_2}}Q, \tag{2}$$

where Q is the net charge density in the SiO_2 region. On a time scale of picosecond, holes would stay almost immobile in the place generated. Consequently, the value of b (initial radius of charge track) would dramatically influence the maximum value of internal electrical field caused by excess carriers in the dielectric (E_{ox}). Figure 2 presents the E_{ox} as a function of b at 4 ps after the ion incidence, where LET = 0.3 pC/μm and the oxide thickness $t_{ox} = 2.58$ nm.

Under this circumstance, since the net charge density is mainly due to the pileup of holes, we can assume the value of E_{ox} would behave a linear relationship with t_{ox} when the LET is specified. Figure 3 presents E_{ox} as a function of t_{ox}, where the applied biases are chosen to make sure that the electric field before the ion incidence (E_{ext}) are equal to 5 MV/cm. It can be seen that the relationship of E_{ox} and t_{ox} do behave a good linear dependence.

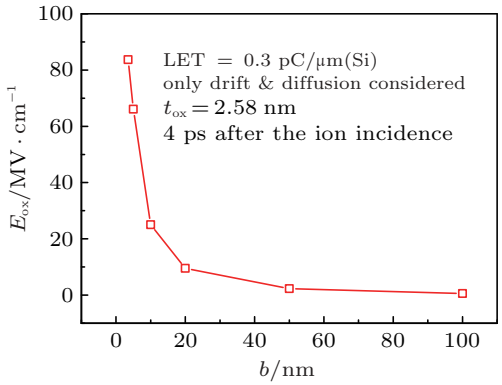


Fig. 2. (color online) The maximum value of the internal electric field caused by excess carriers in oxide (E_{ox}) as a function of the initial radius of charge track at 4 ps after the ion incidence, where LET = 0.3 pC/μm and $t_{ox} = 2.58$ nm.

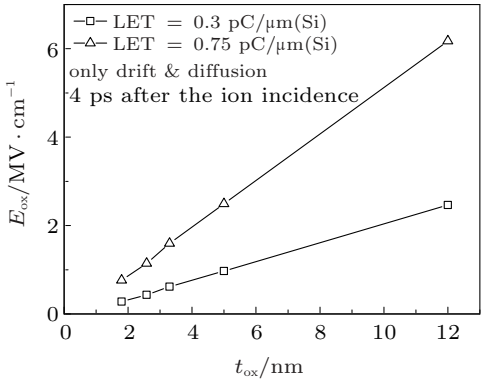


Fig. 3. E_{ox} as a function of t_{ox} at 4 ps after the ion incidence, where $b = 100$ nm and $E_{ext} = 5$ MV/cm.

In the meantime, the potential on the SiO_2/Si interface (V_{Si/SiO_2}) would fall temporarily due to the electrons pileup at the side of Si substrate. Figure 4 presents the surface potential as a function of time. We can see that V_{Si/SiO_2} reaches its minimum at 2 ps before the peak of charge generation rate. When the maximum value of electric field in the oxide region E_{ox} reaches its maximum, V_{Si/SiO_2} does not return to the the value before ion strike. Thus, the decrease in V_{Si/SiO_2} would make contribution to the maximum electric field in oxide.

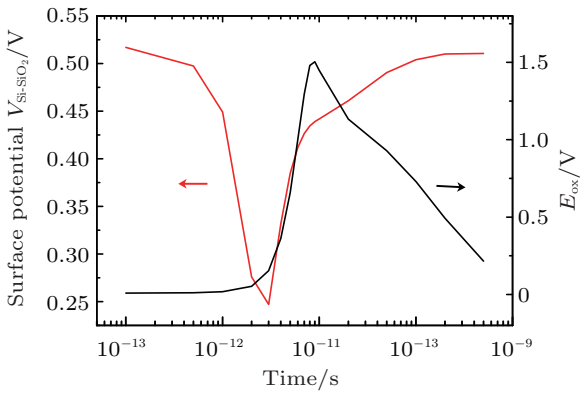


Fig. 4. (color online) Surface potential V_{Si/SiO_2} and the maximum value of internal electrical field caused by excess carriers in oxide (E_{ox}) as a function of time. The ion incidence occurs at 6 ps.

In the above discussion, only drift and diffusion of excess carriers are considered. This is a simplified model to study the influences of the initial radius of charge tracks, the LET value of incident ions, and the decrease in surface potential on internal electric field buildup. Then, other mechanisms would be introduced to better understand the whole physical process.

From former studies, recombination is much stronger in SiO_2 than in Si due to the smaller initial radius of charge tracks and stronger interactions with the lattice.[18] Figure 5 presents E_{ox} as a function of external electric field and SRH lifetime. SRH lifetime is defined as the ratio of the excess carrier density to the net recombination rate. Then, let τ_p be the SRH lifetime of holes, $1/\tau_p$ would represent the probability of recombination for each excess hole. When the SRH lifetime gets smaller, the probability of recombination would be higher, or rather recombination gets stronger, the internal electric field will be weaker. Meantime, the fractional yield to escape recombination would be higher with stronger external electric field, so the internal electric field would be stronger.

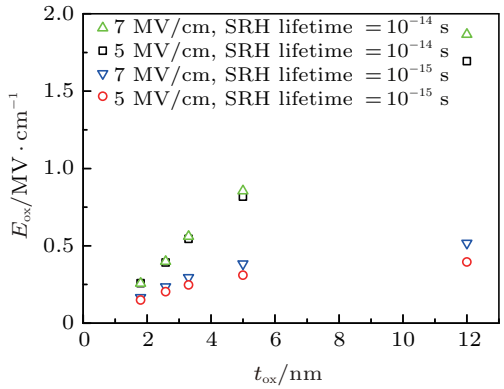


Fig. 5. (color online) E_{ox} as a function of external electric field, SRH lifetimes, and t_{ox}, where $b = 100$ nm.

Other than recombination, impact ionization due to high fields and bandgap tunneling due to thin oxide should also be considered. To study the comparative contribution of each mechanism, we calculate them separately with only charge generation, drift, and diffusion included. Figure 6 presents the increment of E_{ox} after the impact ionization is turned on as a function of external electric field and LET. When the total electric field of the SiO_2 gets stronger, due to either the external electric field or the internal field resulting from ion incidence, the contribution of impact ionization would get bigger. Furthermore, when the oxide gets thicker, the probability of impact ionization would be more obvious too.

Unlike impact ionization, increment due to bandgap tunneling does not show a clear tendency with t_{ox} or external electric field (see Fig. 7), whereas this mechanism does contribute more to the internal electric field when the value of LET is bigger.

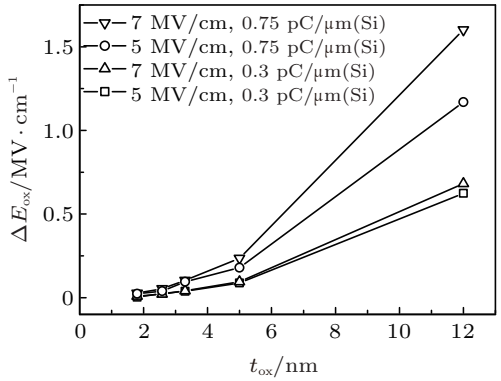


Fig. 6. Increment of E_{ox} when impact ionization is turned on as a function of external electric field, LET values, and t_{ox}, where $b = 100$ nm.

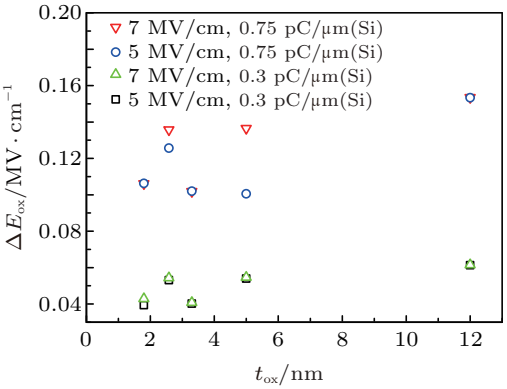


Fig. 7. (color online) Increment of E_{ox} when the bandgap tunneling is turned on as a function of external electric field, LET values, and t_{ox}, where $b = 100$ nm.

3. Verification of our method by comparing with experimental results

After discussing the contributions of several mechanisms to internal electric field buildup, we need to combine them together and consider the whole contributions to SEGR effect.

The mechanisms considered in the gate oxide include drift–diffusion transport model, Schottky–Read–Hall (SRH) recombination, impact ionization, and bandgap narrowing.

Meantime, the mechanisms considered in other regions include: 1) drift–diffusion transport model; 2) doping dependence mobility; 3) mobility degradation in the channel; 4) high field velocity saturation; 5) transverse field dependence mobility; 6) Schottky–Read–Hall (SRH) recombination; 7) impact ionization; 8) Auger recombination; 9) bandgap narrowing.

First of all, there are a few parameters needed to be verified, like the initial radius of the charge track and the SRH lifetime. To do this, we choose to calibrate them using experimental results of Sexton *et al.*[13] In this paper, they measured the critical voltages for SEGR in capacitors with different oxide thicknesses. Figure 8 presents the experimental data in Ref. [13] and our simulation results for comparison. As can be seen, the simulation curve fits well with the data points, where $b = 10$ nm, SRH lifetime is 2×10^{-17} s, and $E_{crit} = 15$ MV/cm (the critical electric field for SiO_2 to breakdown).

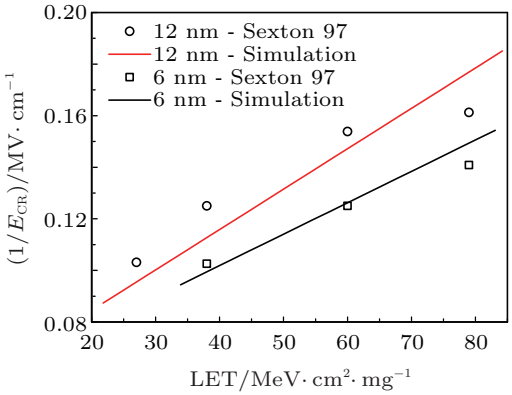


Fig. 8. (color online) Comparison between experimental data from Sexton *et al.* and our simulation results, where $b = 10$ nm and the SRH lifetime is 2×10^{-17} s.

Using these parameters values, physical images of carriers distribution and corresponding electric field in oxide are calculated. Figure 9 presents the hole density, electron density, and electric field as functions of the distance above the Si/SiO_2 interface, where $E_{ext} = 5$ MV/cm and LET = 0.15 pC/μm. Since carrier recombination plays an important role in this process, unlike the circumstance where only carriers drift and diffusion are considered, the value of hole density is very high only in the edge of oxide, other than almost equal along the whole charge track. Otherwise, the distributions of electrons are very similar for the two circumstances. Consequently, electric field reaches its maximum near the Si/SiO_2 interface, shows a trend of decrease close to the Si/PolySilicon interface, and almost keep the same in the middle part of the oxide region.

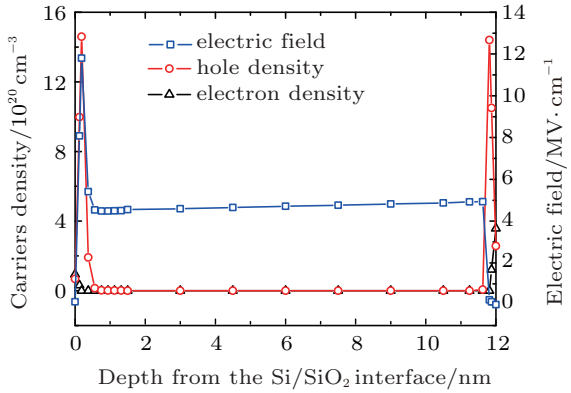


Fig. 9. (color online) Calculated hole density, electron density, and electric field in oxide at 4 ps after the ion incidence as a function of the distance above the Si/SiO_2 interface, where $t_{ox} = 12$ nm.

4. Scaling effects of SEGR in thin oxides

As the density of integrated circuits increases, the thickness of gate oxides shrinks continually. MOS devices with five different feature sizes and corresponding thickness of oxides, doping density in channel region are presented in Table 1.

From the discussion above, no all the related physical mechanisms show the same trend with the decrease in oxide thickness. Keeping the parameters' value the same as the one calibrated in Section 3, contributions of internal electric field due to charge pileup in oxide (ΔE_{ox}) and decrease in surface potential (ΔE_{sub}) are calculated according to oxide thickness ranging from 1.8 nm to 12 nm. The real electric field E_{total} in oxide would be a combination of three factors, namely,

$$E_{total} = E_{ext} + E_{ox} + E_{sub}. \tag{3}$$

Once the value of E_{total} is bigger or equal to E_{crit} due to heavy ion incidence, we can tell that SEGR occurs.

Table 1. Information about MOS devices with five different feature sizes.

t_{ox}/nm	Corresponding feature size of MOS device	Doping density in channel region/cm^{-3}
1.8	90 nm	4.0×10^{17}
2.58	0.13 μm	3.5×10^{17}
3.3	0.18 μm	3.0×10^{17}
5	0.25 μm	2.5×10^{17}
12	0.6 μm	2.0×10^{17}

With different values of E_{ext} and LET, the relationships of E_{ox}, E_{sub}, and t_{ox} are presented in Fig. 10. E_{ox} would become smaller with the decrease in oxide thickness when choosing the same E_{ext} and LET values. Otherwise, E_{sub} would become bigger with the decrease in oxide thickness since the value of surface potential would be very similar to t_{ox} in this range.

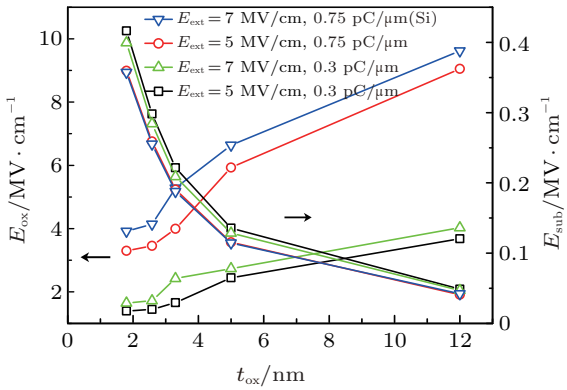


Fig. 10. (color online) Calculated E_{ox} and E_{sub} as functions of t_{ox} with different external electric field and LET.

Considering the different trends of E_{ox} and E_{sub} as functions of t_{ox}, the value of E_{total} would decrease rapidly along with the decrease in t_{ox} when t_{ox} is not very small (12 nm to 3.3 nm), then the trend will not continue and E_{total} may even increase a little bit with the decrease in t_{ox} (3.3 nm to 1.8 nm), as shown in Fig. 11.

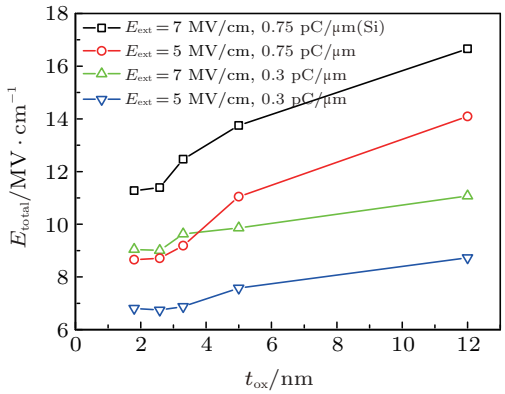


Fig. 11. (color online) Calculated E_{total} as a function of t_{ox} with different external electric field and LET.

5. Conclusion

Dynamics of excess carriers generated by incident heavy ion are considered using TCAD simulation in both SiO_2 and Si substrate of nMOS devices. The influence of initial radius of charge track, surface potential decrease, external electric field, and LET value of incident ion to internal electric field buildup are analyzed separately. To verify the method combining several mechanisms together and further predict the SEGR threshold of nMOS devices with different oxide thicknesses, experimental data from former literatures are used for reference. The simulation results show good agreement with the measured data of $t_{ox} = 6$ nm and $t_{ox} = 12$ nm.

The scaling effects of single-event gate rupture in thin gate oxides are investigated, with t_{ox} ranging from 12 nm to 1.8 nm, the feature size of the MOS device from 0.6 μm to 90 nm correspondingly. Considering the different trend of E_{ox} and E_{sub} changing with t_{ox}, the value of E_{total} would decrease rapidly along with the decrease in t_{ox} when t_{ox} is not very small (12 nm to 3.3 nm), then the trends will not continue and E_{total} may even increase a little bit when the gate oxide becomes thinner and thinner (3.3 nm to 1.8 nm).

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