A high performance HfSiON/TaN NMOSFET fabricated using a gate-last process*

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A gate-last process for fabricating HfSiON/TaN n-channel metal-oxide-semiconductor-field-effect transistors (NMOSFETs) is presented. In the process, a HfSiON gate dielectric with an equivalent oxide thickness of 10 Å was prepared by a simple physical vapor deposition method. Poly-Si was deposited on the HfSiON gate dielectric as a dummy gate. After the source/drain formation, the poly-Si dummy gate was removed by tetramethylammonium hydroxide (TMAH) wet-etching and replaced by a TaN metal gate. Because the metal gate was formed after the ion-implant doping activation process, the effects of the high temperature process on the metal gate were avoided. The fabricated device exhibits good electrical characteristics, including good driving ability and excellent sub-threshold characteristics. The device's gate length is 73 nm, the driving current is 117 μA/μm under power supply voltages of $V_{GS} = V_{DS} = 1.5$ V and the off-state current is only 4.4 nA/μm. The lower effective work function of TaN on HfSiON gives the device a suitable threshold voltage (~ 0.24 V) for high performance NMOSFETs. The device's excellent performance indicates that this novel gate-last process is practical for fabricating high performance MOSFETs.

Keywords: HfSiON, TaN, gate-last process, planarization

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1. Introduction

With the continuous scaling down of complemetentary metal-oxide-semiconductor (CMOS) devices, the traditional poly-Si/SiO_2 gate stack cannot meet the requirements for low power and high performance in CMOS devices because of the large leakage current and serious poly-Si gate depletion effect. Metal gates and high dielectric constant (high-k) gate dielectrics have been introduced as a replacement for the conventional poly-Si gates and SiO_2 gate dielectrics.[1–4] High-k gate dielectrics can realize the same equivalent oxide thickness (EOT) as SiO_2 while having thicker physical thicknesses, which greatly reduces the gate leakage current. Metal gates have no poly-Si gate depletion effect and a weaker Fermi-level pinning effect on the high-k gate dielectrics, both of which are helpful in fabricating high performance CMOS devices.

The ideal high-k/metal-gate (HKMG) CMOS technology requires the gate dielectrics to have a suitable higher k value, a low gate leakage current, and excellent thermal stability, and requires the metal gate to have a suitable effective work function (EWF) and a weaker Fermi-level pinning effect in order to get a low threshold voltage (V_{th}). It is difficult to meet all these requirements at the same time. The thermal stability of an HKMG during the conventional gate-first CMOS process is considered to be one of the fundamental limitations of HKMG integration. Many high-k materials exhibit low crystallization temperatures.[5,6] For example, hafnium oxide (HfO_2) has been a focus due to its suitable dielectric constant (~ 23), relatively wide band gap, and sufficiently high band offset with a Si substrate. In addition, it has a lower crystallization temperature (~ 500 °C). Grain boundaries in crystallized HfO_2 films may act as fast paths for the diffusion of oxygen into the gate dielectric, which will cause an undesirable growth of the interfacial layer, defects, and electrical instability. These limit the application of HfO_2 as a gate dielectric for advanced CMOS technology. Another problem is that the EWF of metal gate electrodes becomes unstable during the high temperature treatment. This is because metal gate electrodes are not refractory and easily react with the high-k gate dielectric, which shifts the EWF toward midgap and shifts V_{th} upward.

In order to overcome these problems, a novel and practical gate-last process is developed to fabricate high-performance HKMG devices. In this process, Si and N are introduced into HfO_2, forming a HfSiON gate dielectric, to improve the gate dielectric's crystallization temperature. Poly-Si is deposited on the HfSiON gate dielectric as a dummy gate and is replaced by a TaN metal gate after source/drain (S/D) formation. Because the ion-implant doping activation at high temperature (about 1000 °C or higher) is performed before the metal gate is formed, the gate-last process keeps the work function of the metal gate stable, making low V_{th}

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MOSFETs[7,8] possible.

2. Device fabrication

The NMOSFET device for this study was fabricated on a 4-inch P(100) Si wafer. The fabrication process flow is shown in Fig. 1. After the local oxidation of silicon (LOCOS) process, novel super-steep retrograde channel doping was performed using heavy ion implantation ($^{11}B^{+}+^{115}In^{+}$).[9] After a standard cleaning process, the Si wafer was treated in hydrofluoric acid (HF)+isopropanol (IPA)+H_2O solution to remove the natural oxide from its surface. A 7 Å SiO_2 interfacial layer (IL) was grown on the Si substrate by rapid thermal oxidation. The HfSiON film was deposited onto the SiO_2 IL using reactive sputtering that alternated between Hf and Si targets in an N_2/Ar ambience, followed by a post-deposition annealing (PDA) in N_2 ambience with a trace of O_2 at 900 °C for 30 s. The poly-Si layer, 1800 Å thick, was deposited by low pressure chemical vapor deposition (LPCVD), patterned using electron-beam lithography, and dry-etched using Cl_2 + HBr mixed gas. After gate patterning, a thin Si_3N_4 sidewall was made beside the gate stack and ultra-shallow S/D extension regions were formed by low energy ion implantation (I/I). Before the S/D implantation, the oxide sidewall was made to form a double sidewall structure to improve the short channel effect (SCE). Then, As atoms with a dose of 4×10^{15} cm^{-2} were implanted into the S/D regions and post annealing was performed at 1000 °C for doping activation. After Ni silicidation, SiO_2 was deposited on the wafer using low-temperature oxidation (LTO) and spin-on glass (SOG) was spun onto it, making the wafer surface nearly planar. After thermal treatment of the SOG, the SOG and LTO were etched back to expose the top of the poly-Si dummy gate. The poly-Si dummy gate was removed to form a gate groove by wet-etching in a hot tetramethylammonium hydroxide (TMAH) solution. A TaN metal gate was deposited in the groove and a T-type metal gate was patterned by photolithography and dry-etching using BCl_3+ SF_6 mixed gas.[10] As the final step, Al metallization was performed. In order to investigate the characteristics of the HfSiON gate dielectric, capacitors with a HfSiON gate dielectric and a TaN metal gate were fabricated at the same time.

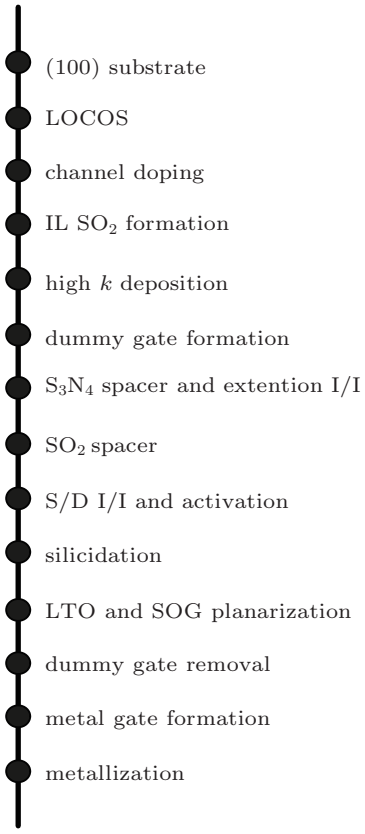


Fig. 1. Fabrication flow of the gate-last process for an HKMG NMOSFET.

3. Investigation of key processes

3.1. HfSiON/TaN gate stack prepared by PVD

The physical characteristics of the HfSiON gate dielectric prepared by physical vapor deposition (PVD) were investigated using high-resolution transmission electronic microscopy (HRTEM), as shown in Fig. 2. Note that the HfSiON gate dielectric has a uniform thickness and remains amorphous after 900 °C PDA, which indicates that the HfSiON gate dielectric has a high crystallization temperature and excellent thermal stability. The high-frequency (1 MHz) capacitance–voltage (C–V) characteristics of the HfSiON gate dielectric were measured at room temperature using an MDC C–V analyzer, as shown in Fig. 3. The EOT of 10 Å is extracted by fitting the measured data to a C–V simulation with a quantum mechanical simulator. According to the HRTEM analysis and the EOT extracted from the C–V data, it is calculated that the average k value of the HfSiON gate dielectric is 14. The current–voltage (I–V) measurements using a Keithley 4200 semiconductor parameter analyzer reveal that the leakage current (J_g) of the HfSiON gate dielectric with EOT of 10 Å is only 1.9×10^{-3} A/cm^2 at $V_g = V_{fb} - 1$ V, where V_g and V_{fb} are the gate voltage and the flat-band voltage, respectively, as shown in Fig. 4. It is about four orders of magnitude lower than SiO_2 with the same EOT,[10,11] as shown in Fig. 5. The stress-induced leakage current (SILC) of the HfSiON gate dielectric is measured at the constant gate voltage stress V_{stress} of −3 V for 300 s. A small increase of SILC is found in the dielectric, which reveals that it has excellent SILC characteristics, and its interface states-assisted tunneling is smaller. In order to determine the exact EWF of the TaN metal gate on the HfSiON gate dielectric, HfSiON films were prepared with different EOTs. According to the formula for calculating the metal gate's work function, the EWF of the TaN metal gate on the HfSiON gate dielectric is 4.3 eV, which meets the EWF requirement for a metal gate in an NMOSFET.

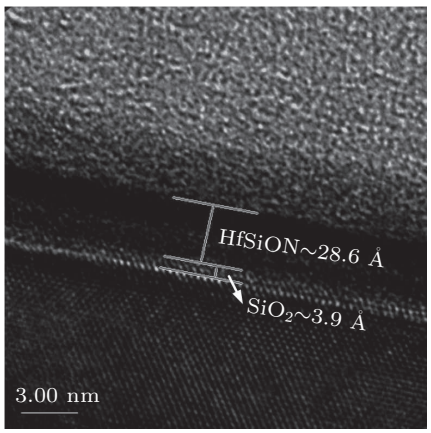


Fig. 2. HRTEM image of a HfSiON gate dielectric after 900 °C PDA.

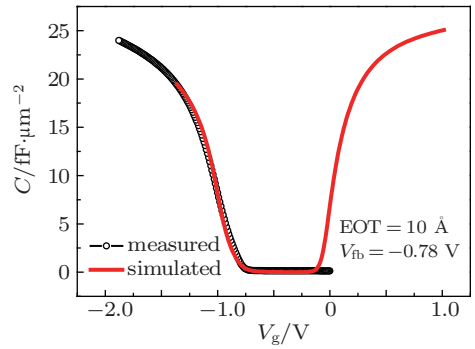


Fig. 3. (color online) The *C*–*V* curve at 1 MHz of an NMOS capacitor with a HfSiON/TaN gate stack.

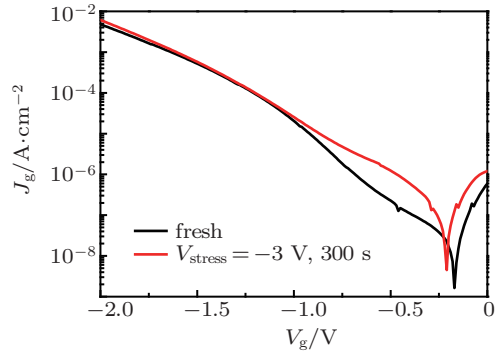


Fig. 4. (color online) SILC characteristics of an NMOS capacitor with a HfSiON/TaN gate stack.

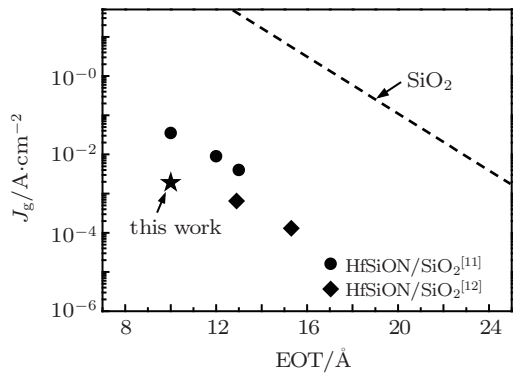


Fig. 5. EOT dependence of the gate leakage current at $V_g = V_{fb} - 1$ V for a HfSiON gate dielectric.

3.2. LTO + SOG planarization

In order to remove the poly-Si dummy gate in the gate-last process, a plane wafer surface is required. In our experiment, a novel LTO+SOG planarization process is developed and its detailed steps are shown in Fig. 6.

After the S/D formation and Ni silicidation, 8000 Å SiO_2 was deposited on the wafer by LTO. Then, 3500 Å SOG was spun onto it, followed by a thermal treatment. The SOG is a type of glass that can be applied as a liquid and annealed to form a layer of glass having characteristics similar to those of SiO_2; it has better step coverage and robust gap filling. After the thermal treatment, a nearly planar surface was obtained. Next, the SOG and LTO were etched back by a reactive ion etching (RIE) process to expose the poly-Si dummy gate, which is named the "recessed 3-step etchback process" and based on a carbon tetrafluoride (CF_4) and trifluoromethane (CHF_3) mixture. In the 3-step etchback process, the 1st-step etch is designed for etching the SOG layer to the interface between the SOG and the LTO layers, forming a recessed profile across the whole wafer. Usually, the SOG etch rate around the wafer edge is faster than that at the wafer center and a convex profile is formed because of the wafer edge's micro-loading effect, which brings difficulties to the subsequent planarization process. In order to avoid the convex profile of the SOG formation, a SOG RIE process with a convex etch-rate profile distribution across the whole wafer is developed by modifying the etch parameters (reactive gas pressure, radio-frequency (rf) power, inserting an additional step of Ar/O_2 polymer treatment during etching). The SOG etch rate at the wafer center is faster than that around the wafer edge, which is helpful for forming a concave profile of SOG. After the SOG etchback, the 2nd-step etch is designed for trimming the interface profile between SOG and LTO layers and adjusting the extent of the recess formed in the previous step. The RIE parameters in the 2nd etch step yield a concave etched profile, which is just the opposite of the convex etched profile of the 1st etch step. The 1st and the 2nd etch steps together are capable of resolving the etch uniformity issues and obtaining a planar surface. The 3rd etch step has no uniformity issues and is designed for etching the LTO to expose the dummy poly gate top. The planar topography fabricated by the recessed 3-step etch-back process is investigated using scanning electron microscopy (SEM), as shown in Fig. 7. The figures indicate a relatively uniform etch-back planarization. The LTO thickness difference is below 13%. The residual LTO is about 142 nm thick – thinner than the residual poly-Si dummy gate (162 nm) – which is helpful for poly-Si removal. The final LTO profile across the whole wafer is like a flat-bottomed bowl. The effective wafer diameter is greater than 90% of the original wafer size (100 mm). The uniformity within the effective area is over 95%, which is much closer to the result of complete global planarization by the chemical mechanical planarization (CMP).

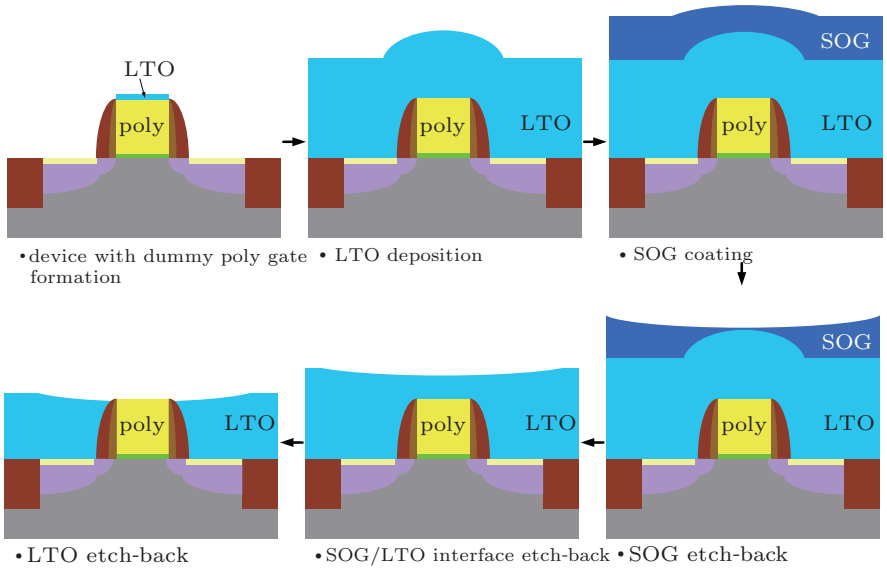


Fig. 6. (color online) Steps of LTO + SOG planarization.

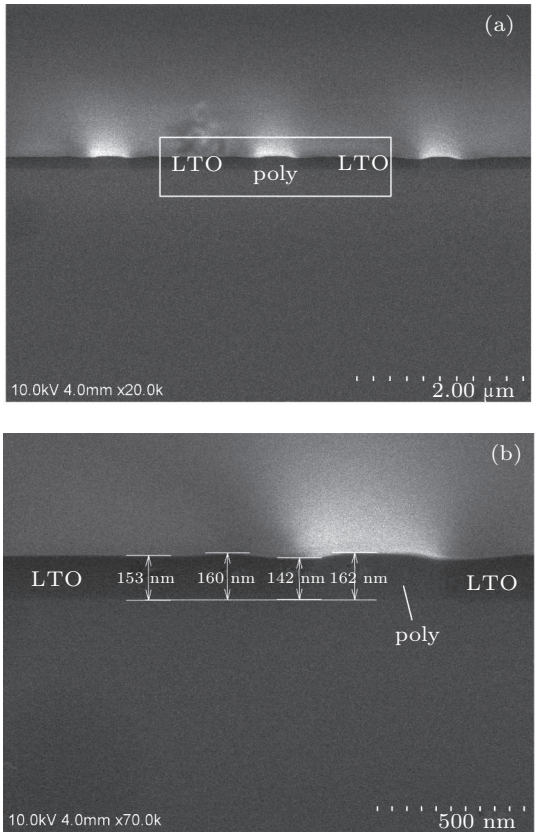


Fig. 7. Cross sectional SEM micrographs of planarization on the gate stack by the recessed 3-step etch-back process: (a) global view, (b) zoomed view of the white box in panel (a).

3.3. Poly-Si dummy gate removal

After the LTO+SOG planarization, the poly-Si dummy gate was removed by wet-etching in a hot TMAH solution. The process conditions were 10 vol.% TMAH solution and 60 °C process temperature. Under these conditions, the etch rate (ER) selectivity of poly-Si was at least 300 higher than HfSiON, Si_3N_4, and LTO. Before the poly-Si dummy gate removal, the wafer should be dipped into dilute HF solution to remove the SiO_2 hard mask residue on the poly-Si dummy gate. This is because the ER of SiO_2 in the hot TMAH solution is very low and even a very thin SiO_2 residue on the poly-Si dummy gate will prevent the wet-etching of the poly-Si. The cross sectional SEM micrograph of the poly-Si dummy gate removed by TMAH is shown in Fig. 8. The depth of the gate groove is about 68 nm and its length is 73 nm. From the figure, we can see that the poly-Si dummy gate is completely removed and no over-etching is observed due to the high ER selectivity of poly-Si relative to HfSiON and the other materials.

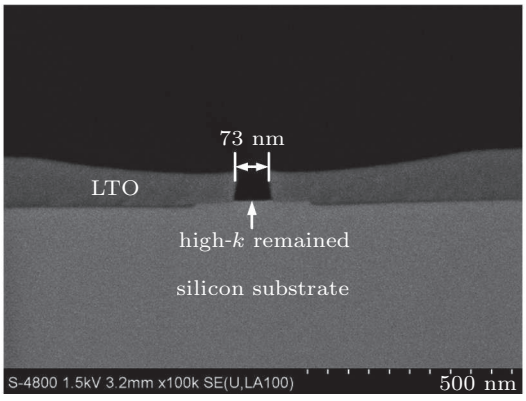


Fig. 8. Cross sectional SEM micrograph of the gate groove after poly-Si dummy gate removal by TMAH.

4. Results and discussion

By integrating the key processes mentioned above, high performance HfSiON/TaN NMOSFETs with 73 nm gate length have been fabricated. Figures 9 and 10 show the I_{DS}–V_{DS} and I_{DS}–V_{GS} characteristics of the device, where I_{DS} is

the drain current, V_{DS} is the drain–source voltage, and V_{GS} is the gate–source voltage. At $V_{GS} = V_{DS} = 1.5$ V, the measured saturation driving current I_{on} is 117 μA/μm. The off-state current I_{off} is only 4.4 nA/μm. The ratio of I_{on}/I_{off} is more than 10^4. The V_{th} of saturation is 0.24 V measured at $I_{DS} = 1$ μA/μm, which is consistent with the EWF measured in the NMOS capacitors previously mentioned. The subthreshold slope (SS) of the device is 101 mV/dec measured at $V_{DS} = 1.5$ V. The drain induced barrier lowering (DIBL) is 41.5 mV/V. These results show that the fabricated NMOSFET with the HfSiON/TaN gate stack has good electrical characteristics, including good driving ability and excellent subthreshold characteristics. We believe that if the process conditions are optimized and mobility enhancement processes are integrated, the electrical characteristics of the device can be further improved.

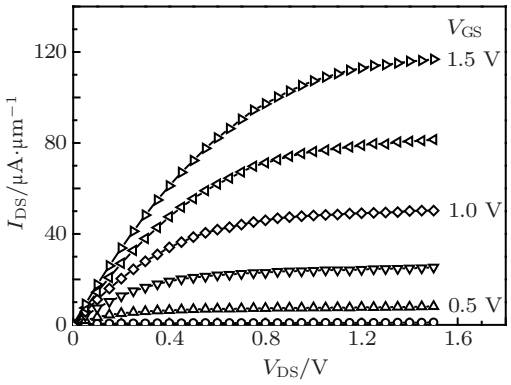


Fig. 9. The I_{DS}–V_{DS} characteristics for NMOSFET with HfSiON/TaN gate stack (V_{GS} starts from 0 to 1.5 V in steps of 0.25 V).

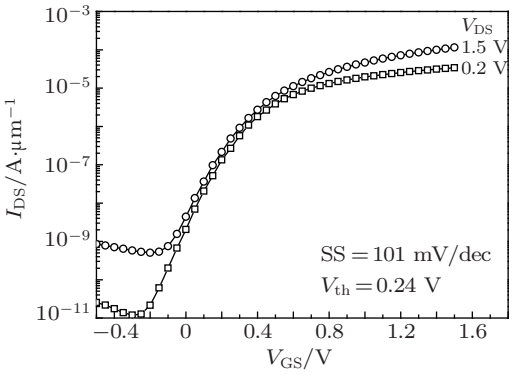


Fig. 10. The I_{DS}–V_{GS} characteristics of NMOSFET with a HfSiON/TaN gate stack (V_{DS} of 0.2 V and 1.5 V).

5. Conclusion

A novel and practical gate-last process is presented to fabricate NMOSFETs with HfSiON/TaN gate stacks. In the process, many key processes have been developed, such as the preparation of the HfSiON gate dielectric by PVD, the Si_3N_4/SiO_2 double sidewall scheme, LTO+SOG planarization, removal of the poly-Si dummy gate by TMAH wet-etching and replacing it by the TaN metal gate. Because of the introduction of Si and N, the HfSiON gate dielectric exhibits good physical and electrical characteristics, such as good thermal stability up to 900 °C, a low gate leakage current, and a small EOT. The TaN metal gate on the HfSiON gate dielectric has a lower EWF (∼ 4.3 eV). Because of forming the TaN metal gate after the S/D high temperature process, the metal gate has good work function stability, which gives the device a low V_{th} (∼ 0.24 V). The LTO+SOG planarization is a simple and cheap method to get global planarization closer to the traditional CMP process. With poly-Si dummy gate removal by TMAH wet-etching, a sub-100 nm gate groove is easy to be achieved. By integrating the key processes mentioned above, a high performance HfSiON/TaN NMOSFET has been fabricated. The excellent electrical characteristics of the device indicate that this gate-last process is a possible solution for advanced CMOS device fabrication.

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