Low voltage program-erasable Pd-Al_2O_3-Si capacitors with Ru nanocrystals for nonvolatile memory application*

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(Received 4 March 2013; revised manuscript received 23 April 2013)

Pd-Al_2O_3-Si capacitors with Ru nanocrystals are fabricated and electrically characterized for nonvolatile memory application. While keeping the entire insulator Al_2O_3 thickness fixed, the memory window has a strong dependence on the tunneling layer thickness under low operating voltages, whereas it has weak dependence under high operating voltages. As for the optimal configuration comprised of 6-nm tunneling layer and 22-nm blocking layer, the resulting memory window increases from 1.5 V to 5.3 V with bias pulse increasing from 10^{-5} s to 10^{-2} s under ±7 V. A ten-year memory window as large as 5.2 V is extrapolated at room temperature after ±8 V/1 ms programming/erasing pulses.

Keywords: metal-oxide-semiconductor capacitors, nonvolatile memory, Ru nanocrystals, atomic-layer-deposition

PACS: 73.40.Qv, 73.61.–r **DOI:** 10.1088/1674-1056/22/11/117308

1. Introduction

With the down-scaling of memory devices, nonvolatile memories based on discrete nanocrystal charge storage nodes are attracting more and more attention due to their low programming/erasing voltages, fast operating speeds, good scalabilities, and endurance characteristics.[1–4] Regarding nanocrystal materials, it is considered that metallic nanocrystals are more advantageous than semiconducting ones, which is attributed to a wide range of available work functions, high density of states around the Fermi level, and small energy perturbation due to carrier confinement, etc.[5] Among various metallic materials, ruthenium (Ru) has a high work function (∼ 4.7 eV) and good compatibility with complementary metal-oxide-semiconductor (CMOS) technology.[6,7] Accordingly, Ru nanocrystals could be a promising candidate for the memories. However, most efforts are focused on the preparation and characterization of Ru nanocrystals.[8–12] Recently, Mao *et al.*[13] reported on Ru nanocrystal memory devices with a SiO_2 insulator and an Al gate, demonstrating program and erase functions under very high operating voltages (18 V–20 V).[13] We previously investigated the electrical performances of Al-electrode-based MOS capacitors with atomic-layer-deposition (ALD) Ru nanocrystals embedded in ALD Al_2O_3, exhibiting programmable rather than erasable characteristics because of a small e-injection barrier height under the erase mode.[8] Therefore, to realize high performance memories, continuous efforts should be made to explore new materials and optimal gate stack configurations.

As a critical part of memory cells, high density nanocrystals are indispensible to achieve an enough charge storage capability. To date, ALD and rapid thermal anneal (RTA) agglomeration are generally used for the formation of Ru nanocrystals, and both of them have good compatibility with the conventional memory process.[7–13] The former exhibits a high sensitivity to the substrate surface chemistry as well as relevance to the precursor properties.[7] However, for the latter, the nanocrystal density and size depend on its starting film thickness and RTA temperature in despite of the surface chemistry. Therefore, it is easier to control the density and morphology of nanocrystals by process optimization.

In this article, high density Ru nanocrystals are formed by RTA agglomeration of a sputtered ultra-thin Ru film. Metallic palladium (Pd) is used as an electrode material due to its high work function (5.22 eV), aiming to suppress additional electron injection from the gate under the erase mode due to an enhanced barrier height for electron injection.[14] In addition, ALD Al_2O_3 films are used as both the tunneling and blocking layers, owing to its large band gap (8.7 eV), higher permittivity (k ∼9) than SiO_2, good chemical stability with silicon substrate, particularly high temperature thermal stability that ensures its amorphous nature after high temperature annealing.[15] Therefore, the Pd-Al_2O_3-Si (MOS) capacitors with Ru nanocrystals embedded are fabricated, and the physical thicknesses of both the tunneling layer and the blocking layer are optimized. As a result, the fabricated memory capacitors demonstrate robust program-erasable and charge retention characteristics.

*Project supported by the National Key Technology Research and Development Program of China (Grant No. 2009ZX02302-002), the National Natural Science Foundation of China (Grant No. 61274088), and the Program for New Century Excellent Talents in University of Ministry of Education of China (Grant No. NCET-08-0127).

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2. Experimental procedures

(100)-orientated p-type Si wafers with resistivities ranging from 8 Ω·cm to 12 Ω·cm were used as starting substrates. After the standard RCA cleaning, the remaining chemical oxide was removed by diluted HF acid rinsing. Subsequently, the cleaned wafer was transferred into the ALD system, and a 9-nm Al_2O_3 film was deposited as a tunneling layer using $Al(CH_3)_3$ and H_2O precursors at 300 °C. After that, a nominal 2-nm Ru layer was sputtered onto the Al_2O_3 tunneling layer with a deposition rate of ~ 0.9 nm/min in a magnetron sputtering system. To form nanocrystals, an RTA step was performed at 900 °C for 30 s in N_2. Then, an 18-nm Al_2O_3 film was deposited as a blocking layer by ALD. Further, post-deposition RTA at 800 °C for 30 s was carried out in order to improve the quality of the blocking Al_2O_3 film. Finally, around 100-nm thick Pd electrodes with a diameter of 100 μm were formed by means of a lift-off technique. The back-side of the Si substrate was also coated with 1-μm Al for ohmic contact after the removal of the native oxide. For comparison, a reference sample of the MOS capacitor without a nanocrystal was also fabricated. To investigate the influence of both the tunneling-layer (T) and blocking-layer (B) thicknesses on the memory performances, three configurations of T/B were employed while maintaining a constant thickness sum of T and B, i.e., T/B = 4 nm/24 nm, 6 nm/22 nm, and 8 nm/20 nm.

Transmission electron microscopy (TEM) and atomic force microscopy (AFM) were used to show the formed nanocrystal morphology. Capacitance–voltage (C–V) measurements were performed on an LCR meter (Keithley 590) at room temperature, and the programming/erasing pulses were generated by a pulse/patten generator (Keithley Model 3402).

3. Results and discussion

Figures 1(a) and 1(b) show the AFM image and planar-view TEM image of the annealed Ru film on the Al_2O_3 film. It is found that the RTA results in the formation of uniform and spherical nanocrystals with dimensions of 4 nm–7 nm, and the extracted density approximates to 1.2×10^{12} cm^{-2}. Furthermore, the electron-diffraction image of the selected area reveals that the resulting nanocrystals are polycrystalline.

Figure 2(a) shows typical C–V hysteresis loops of the MOS capacitors with Ru nanocrystals in comparison with the counterpart without nanocrystals for the gate sweep voltages ranging from −11 V to +11 V. It is found that the introduction of nanocrystals causes a much larger hysteresis window than the absence of the nanocrystals, i.e., 11.2 V versus 0.2 V. This indicates that the Ru nanocrystals can offer a superior charge storage capacity. Further, plotting of flat-band voltage (V_{fb}) versus maximum gate voltage for both backward and forward C–V sweeps, and plotting of hysteresis window versus maximum gate voltage are all shown in Fig. 2(b). In terms of the backward C–V sweep, V_{fb} moves continuously up to +4.1 V with maximum gate voltage increasing up to 11V, corresponding to electron trapping. As for the forward C–V sweep, V_{fb} shifts quickly from around zero to −7.0 V, revealing efficient electron de-trapping. Furthermore, the resulting hysteresis window goes up to around 11 V as the maximum gate voltage increases to 11 V. This manifests that our fabricated nanocrystal capacitors exhibit superior memory effects.

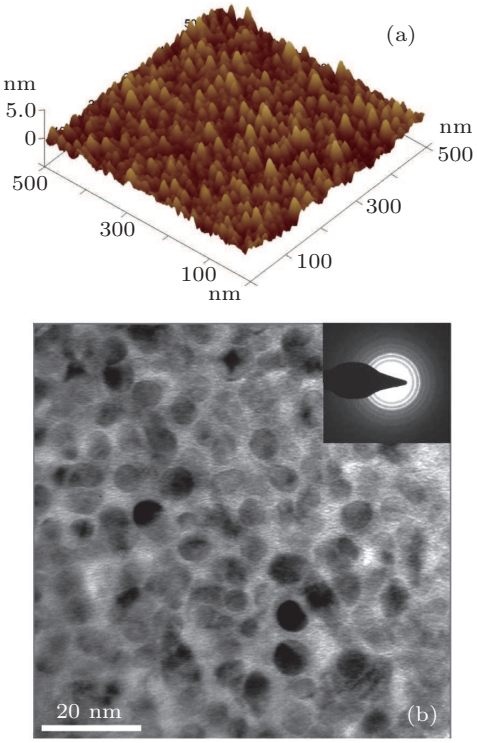


Fig. 1. (color online) (a) AFM image and (b) plan-view TEM image of the annealed Ru layer on the Al_2O_3 film together with electron-diffraction image of the selected area.

Figure 3 illustrates the programming and erasing characteristics of the memory capacitor under different operating voltages. According to the accumulative capacitance, the equivalent oxide thickness is calculated to be 13.9 nm. In the case of a 0.1 ms programming pulse, V_{fb} shifts remarkably from 0.4 V to 2.8 V as the programming voltage (V_p) increases from +6 V to +11 V. Regarding a 0.1-ms erasing pulse, V_{fb} changes from −0.7 V to −2.8 V with erasing voltage (V_e) increasing from −6 V to −11 V. For the programming/erasing voltage of $+/-8$ V, the obtained memory window is as large as 3.7 V. The aforementioned results suggest that the nanocrystal memory capacitor can offer good program-erasable characteristics even under low voltages.

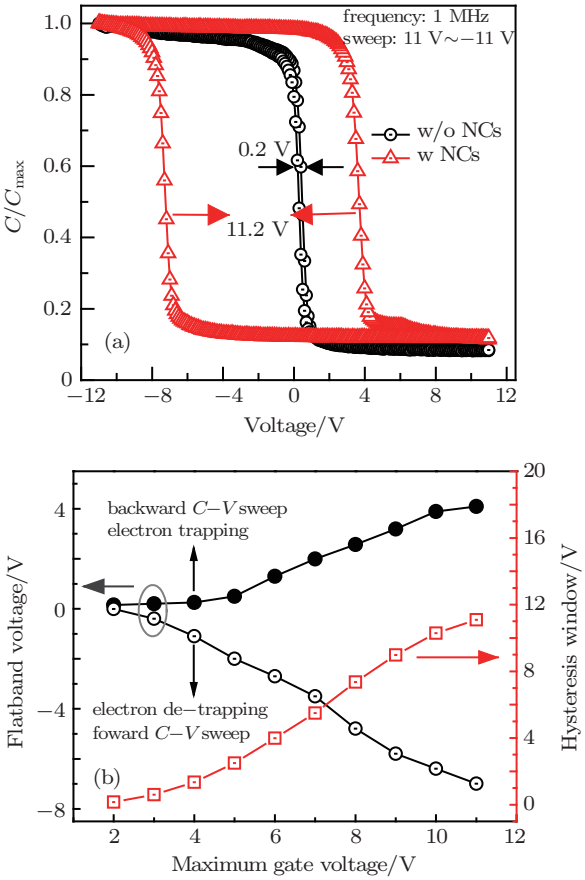


Fig. 2. (color online) (a) The C–V hysteresis curves of the Pd-Al_2O_3-Si (MOS) capacitor with Ru nanocrystals (w NCs) compared with the counterpart without nanocrystals (w/o NCs) for +11 V–−11 V gate sweeping voltages at 1 MHz; (b) dependence of the resulting flat-band voltage and hysteresis window on maximum gate voltage for the MOS capacitor with Ru nanocrystals in the case of backward and forward C–V sweeps. Herein, the maximum gate voltage means the sweeping voltage range, for example, a maximum gate voltage of 2 V represents a sweeping voltage range of +2 V–−2 V.

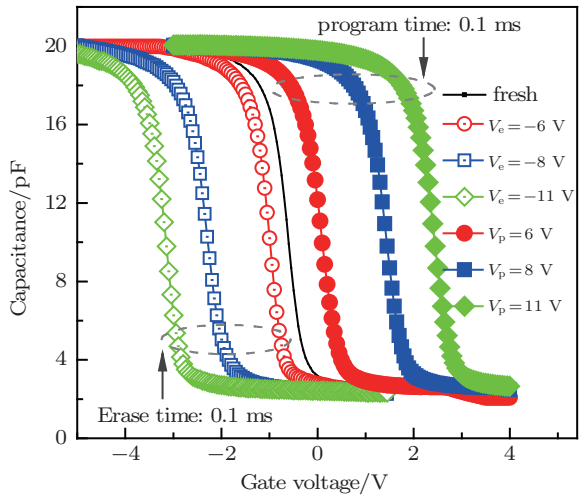


Fig. 3. (color online) The programming and erasing characteristics of the MOS capacitors with Ru NCs as a function of operating voltage for 0.1 ms pulse time, V_p and V_e represent the programming and erasing voltages, respectively.

In order to observe the effect of the T/B thickness on the device performances, the evolutions of V_{fb} with operating voltage are shown in Fig. 4 for the programming and erasing modes, respectively. It is seen that the absolute value of V_{fb} exhibits marked difference for various T/B configurations in the case of 5 V operating voltage, and the extracted memory window decreases from 2.69 V to 0.65 V with tunneling layer thickness increasing from 4 nm to 8 nm. Further, as the operating voltage increases up to 9 V, the memory windows for different T/B configurations become closer and closer, for example, they are equal to 6.8 V and 6.3 V for the 4 nm and 8 nm tunneling layers, respectively. This can be explained as follows. For quite a low operating voltage (e.g., 5 V), the mechanism of charge transportation through the T is dominated by direct tunneling, thus the tunneling probability of charges is determined by the T thickness. That is to say, the thinner the tunneling layer is, the larger the tunneling probability of charges is. Accordingly, the largest memory window is achieved for the thinnest T (i.e., 4 nm). As the operating voltage increases, the electric field drop across the T becomes so large that the charges can tunnel through a small triangle barrier, and the charge transportation through the T is dominated by the Fowler–Nordheim tunneling mechanism. As a result, the tunneling probabilities of charges going through different thickness T become much closer, hereby resulting in close memory windows under high operating voltages.

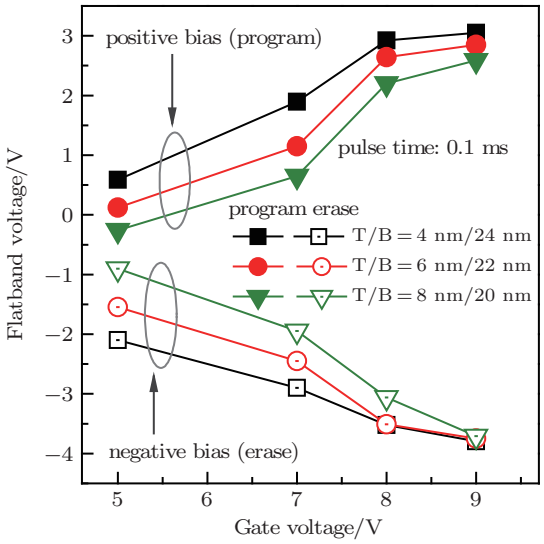


Fig. 4. (color online) Dependence of the resulting flat-band voltage (V_{fb}) on the gate voltage (i.e., absolute operating voltage) under the erase and program modes, respectively, for different T/B configurations.

Figure 5 shows the dependence of the flat-band voltage shift (ΔV_{fb}) on pulse time under +7 V and −7 V, respectively, for various T/B configurations. It is found that ΔV_{fb} increases with the increase of pulse time under the program and erase modes, respectively. However, when the pulse time surpasses 10^{-3} s, ΔV_{fb} exhibits a slight increase, suggesting a tendency to programming and erasing saturation. In terms of the configuration of 6 nm T/22 nm B, the extracted memory window

increases from 1.5 V to 5.3 V with pulse time increasing from 10^{-5} s to 10^{-2} s. This reveals that the present memory capacitors have robust programming and erasing performances under low operating voltages.

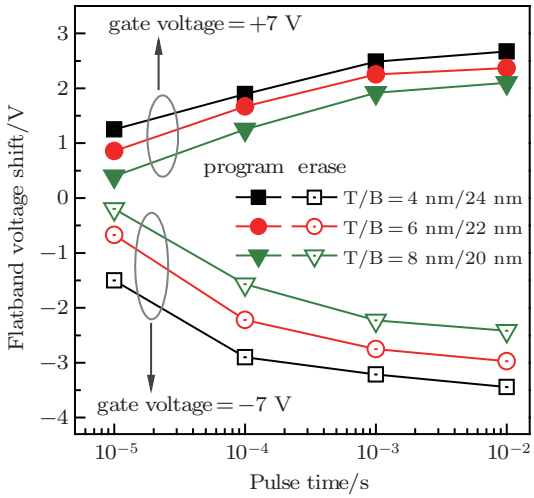


Fig. 5. (color online) Typical evolutions of the resulting flat-band voltage shift ($\Delta V_{\rm fb}$) against pulse time for various T/B configurations in the case of +7 V programming and −7 V erasing, respectively.

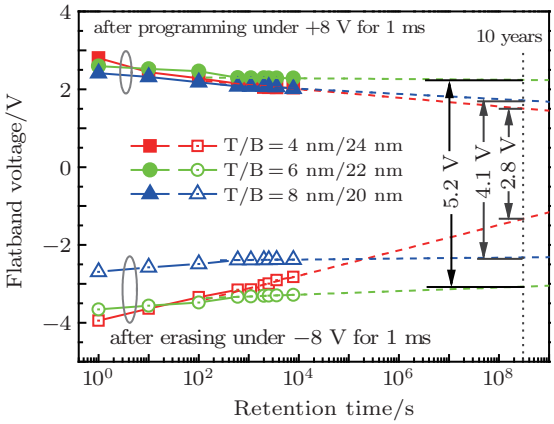


Fig. 6. (color online) Dependence of the flat-band voltage ($V_{\rm fb}$) on retention time under zero gate voltage for the memory capacitors with various T/B configurations after +8 V programming and −8 V erasing for 1 ms, respectively, at room temperature.

Figure 6 shows the charge retention characteristics of the memory capacitors with different T/B configurations after programming/erasing under $+/-8$ V, respectively, for 1 ms at room temperature. It is found that the configuration of T/B (4 nm/24 nm) results in a larger degradation rate of $V_{\rm fb}$ than the other two configurations under the program and erase modes, respectively. This is because the thick T can suppress effectively direct back-tunneling of the stored charges, which is considered as a dominant mechanism of charge loss at room temperature.[16] Further, ten-year memory windows are extrapolated. It is seen that the configuration of T/B (6 nm/22 nm) can achieve the largest memory window of 5.2 V after ten years, which is ascribed to the fact that such a proper configuration of T/B can offer efficient programming and erasing, and prevent fast loss of the stored charges under zero gate voltage. Furthermore, when the programming/erasing voltage decreases to $+/-7$ V, the deduced ten-year memory window is still as large as 4.2 V for 6 nm T/22 nm B (not shown here). To our knowledge, the storage capacity and retention of charges are determined mainly by the nanocrystal potential-well depth, which is related to the work function of nanocrystal; thereby, it is inferred that the integration of Al_2O_3 and Ru nanocrystals can afford an deep enough potential well even after high temperature annealing.

4. Conclusion

High density Ru nanocrystals are formed by RTA agglomeration of sputtered ultra-thin Ru film, and the MOS capacitors with Ru nanocrystals demonstrate efficient programming and erasing characteristics even under low operating voltages of $+/-6$ V. Further, the tunable memory characteristics of the capacitors are evidenced by varying the thickness ratio of T/B, i.e., the resulting memory window increases with the reduction of the T thickness for low operating voltages and becomes gradually close under high operating voltages. Moreover, the superior charge retention characteristics are achieved for the configuration of 6 nm T/22 nm B. In short, the concept of our fabricated memory capacitors is very promising for low power consumption memories.

References

[1] Choi S, Choi H, Kim T W, Yang H, Lee T, Jeon S, Kim C and Hwang H 2005 *IEDM Tech. Dig.* p. 173
[2] You H C, Hsu T H, Ko F H, Huang J W and Lei T F 2006 *IEEE Electron. Device Lett.* **27** 644
[3] Samanta S K, Singh P K, Yoo W J, Samudra G, Yeo Y C, Bera L K and Balasubramanian N 2005 *IEDM Tech. Dig.* p. 177
[4] Ping M A O, Zhang Z G, Pan L Y, Xu J and Chen P Y 2009 *Chin. Phys. Lett.* **26** 056104
[5] Liu Z, Lee C, Narayanan V, Pei G and Kan E C 2002 *IEEE Trans. Electron. Devices* **49** 1606
[6] Zhong H, Heuss G and Misra V 2000 *IEEE Electron. Device Lett.* **21** 593
[7] Zhang M, Chen W, Ding S J, Wang X P, Zhang D W and Wang L K 2007 *J. Vac. Sci. Technol. A* **25** 775
[8] Zhang M, Chen W, Ding S J, Liu Z Y, Huang Y, Liao Z W and Zhang D W 2008 *J. Phys. D: Appl. Phys.* **41** 032007
[9] Farmer D B and Gordon R G 2007 *J. Appl. Phys.* **101** 124503
[10] Yim S S, Lee M S, Kim K S and Kim K B 2006 *Appl. Phys. Lett.* **89** 093115
[11] Maikap S, Wang T Y, Tzeng P J, Lin C H, Lee L S, Yang J R and Tsai M J 2007 *Appl. Phys. Lett.* **90** 253108
[12] Yim S S, Lee D J, Kim K S, Lee M S, Kim S H and Kim K B 2008 *Electrochem. Solid-State Lett.* **11** K89
[13] Mao P, Zhang Z, Pan L, Xu J and Chen P 2008 *Appl. Phys. Lett.* **93** 242102
[14] Tsai P H, Chang-Liao K S, Yang D W, Chung Y B, Wang T K, Tzeng P J, Lin C H, Lee L S, Tsai M J and Chin A 2008 *Appl. Phys. Lett.* **93** 252902
[15] Ding S J, Huang Y J, Huang Y, Pan S H, Zhang W and Wang L K 2007 *Chin. Phys.* **16** 2803
[16] Yang Y L and White M H 2000 *Solid State Electron.* **44** 949