The degradation mechanism of an AlGaN/GaN high electron mobility transistor under step-stress*

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Step-stress experiments are performed in this paper to investigate the degradation mechanism of an AlGaN/GaN high electron mobility transistor (HEMT). It is found that the stress current shows a recoverable decrease during each voltage step and there is a critical voltage beyond which the stress current starts to increase sharply in our experiments. We postulate that defects may be randomly induced within the AlGaN barrier by the high electric field during each voltage step. But once the critical voltage is reached, the trap concentration will increase sharply due to the inverse piezoelectric effect. A leakage path may be introduced by excessive defect, and this may result in the permanent degradation of the AlGaN/GaN HEMT.

Keywords: AlGaN/GaN HEMT, reliability, degradation mechanism, inverse piezoelectric effect

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1. Introduction

Due to the many outstanding material properties of GaN, such as high breakdown electric field ($> 3 \times 10^6$ V/cm),[1] high sheet carrier density ($> 10^{13}$ cm^{-2}),[2] and high electron mobility (> 1500 cm^2/V·s),[3] the AlGaN/GaN HEMT has shown extraordinary performance at a wide range of frequency in RF power applications. One of the greatest impediments today affecting the further development of GaN HEMT technology is its limited electrical reliability. In order to achieve solid reliability, a thorough understanding of the physical mechanism behind the device degradation is of great importance.

Although many studies have been conducted attempting to gain insights into the electrical degradation of GaN HEMT, the detailed failure mechanism has not been identified. Joh and del Alamo[4] proposed that there is a critical drain-to-gate voltage beyond which GaN HEMT begins to degrade in electrical-stress experiments. Degradation is dependent on electric field and commonly attributed to the generation of defects through inverse piezoelectric effect.[5–7] Meneghini *et al.*[8] found that for sufficient long stress time, the degradation occurs even below the "critical voltage", and demonstrated that before permanent degradation the gate current would become noisy, indicating an increase in defect concentration. Recent reports[9,10] suggested that the degradation of some device parameters is recoverable, arising from the high field-induced electron detrapping beyond a critical voltage or the recovery of surface state after the step-stress.

In this paper, step-stress experiments are performed to investigate the mechanism of device degradation in AlGaN/GaN HEMT. It is found that the stress current shows a recoverable decrease during each voltage step and there is a critical voltage beyond which stress current starts to increase sharply, but gate current does not become noisy during the whole experiment.

2. Devices and experiments

The AlGaN/GaN HEMT epitaxial structure was grown by metal organic chemical vapor deposition (MOCVD) on (0001) sapphire substrate. The epitaxial growth was initiated with an AlN nuclear layer followed by a 1.3-μm unintentionally doped (UID) GaN layer. This was followed by a 1-nm thick AlN interlayer and a 29-nm thick $Al_{0.3}Ga_{0.7}N$ barrier layer. The sample was capped with an *in-situ* growth 1-nm thick GaN. The devices fabrication started with mesa isolation which was performed by reactive ion etching (RIE) with an etch-depth of 150 nm. Ohmic contact consisting of Ti/Al/Ni/Au (22 nm/140 nm/55 nm/45 nm) was annealed in a nitrogen ambient at 850 °C for 30 s, yielding a contact resistance typically around 0.5 Ω·mm. Then surface passivation was done by depositing about 60-nm Si_3N_4 through the plasma-enhanced chemical vapor deposition (PECVD). Gate patterns were determined by optical lithography with $L_g = 0.8$ μm and $W_g = 50$ μm. The gate-to-source spacing L_{gs} is 0.7 μm and gate-to-drain spacing L_{gd} is 2.5 μm. Finally, a 200-nm thick Si_3N_4 was deposited as a second surface passivation film.

A typical device used in the study shows I_{dmax} of 900 mA/mm, V_t of -3.5 V, and G_{mmax} of 200 mS/mm. We carried out step-stress experiments in the $V_{ds} = 0$ V state as shown

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in Fig. 1. In the experiments V_g was stepped from −10 V to −50 V in steps of 1 V while keeping $V_d = V_s = 0$ V, the device was stressed for 2 min at each step. During each voltage step stress currents I_{gate}, I_{drain}, and I_{source} were sampled respectively every 20 s. At the end of each step, some measurements were performed in a short time (less than 30 s) to characterize the device. Then the next voltage step was applied immediately. We repeated this cycle at a certain frequency until the end of the step-stress experiment.

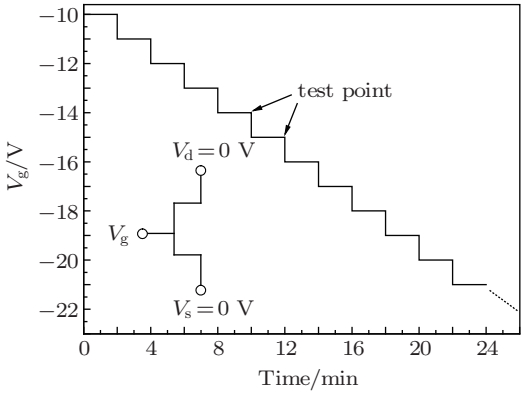


Fig. 1. Stress scheme used in this study: V_g is stepped from −10 V to −50 V in steps of 1 V while keeping $V_d = V_s = 0$ V, the device is stressed for 2 min in each voltage step.

3. Results and discussion

Figure 2 shows the changes in stress current I_{gate}, I_{drain}, and I_{source} with stress time in a step-stress experiment in the $V_{ds} = 0$ V state ($V_d = V_s = 0$ V, $V_g = -10$ V∼ −50 V, −1 V/2 min). Under this condition, there is no current flowing through the channel of the device, and both sides of the device can be stressed simultaneously. The main behaviors are described below.

(i) Stress current shows a recoverable decrease during each voltage step, which is denoted as the recoverable degradation and permanent degradation respectively as shown in Fig. 2.

(ii) Before a certain stress voltage value ($V_g = -35$ V in this experiment) is reached, the stress current increases slightly. But once this critical voltage is reached, the degradation in the stress current starts sharply and continues to increase as the stress experiment proceeds.

(iii) For a low stress voltage level, the source current is smaller in value than the drain current, but when the stress voltage reaches its critical value, the source current increases suddenly, surpassing the drain current by several orders of magnitude.

(iv) Gate current does not become noisy during the whole experiment, which is different from the phenomenon observed in Ref. [8].

Figure 3 shows the Schottky characteristics of the device under study, measured at the end of different stress steps. The gate voltage V_g sweeps from −10 V to 0 V while keeping the drain voltage $V_d = 0$ V and the source terminal open during each measurement. Before the "critical voltage" ($V_g = -35$ V) is reached, the gate leakage current almost remains unchanged. Then a sudden and irreversible increase in leakage current occurs at the "critical voltage" ($V_g = -35$ V), which is consistent with the change of stress gate current illustrated in Fig. 2.

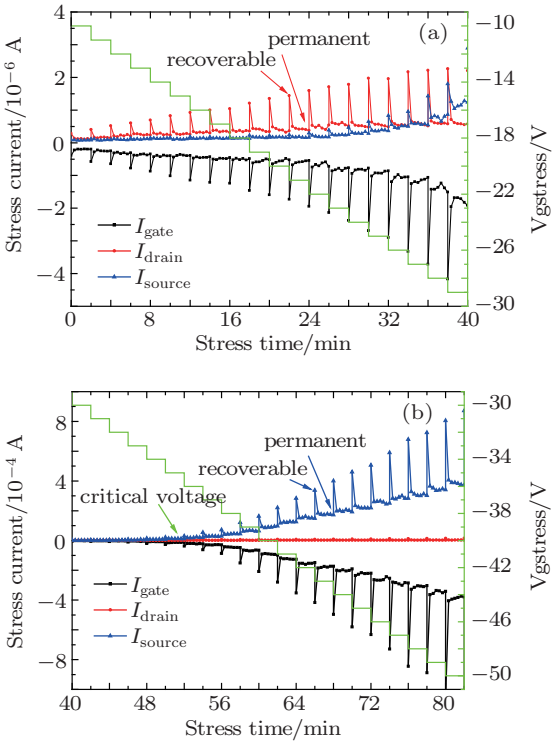


Fig. 2. (color online) Changes in the stress current I_{gate}, I_{drain}, and I_{source} with stress time in a step-stress experiment in the $V_{ds} = 0$ V state ($V_d = V_s = 0$ V, $V_g = -10 \sim -50$ V, −1 V/2 min), from 0 min to 40 min (V_g from −10 V to −29 V) (a) and from 40 min to 82 min (V_g from −30 V to −50 V) (b).

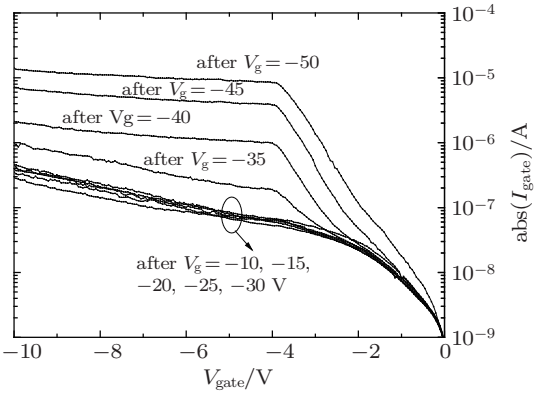


Fig. 3. Schottky characteristics of the device under study, measured at the end of different stress steps. The gate voltage V_g sweeps from −10 V to 0 V while keeping the drain voltage $V_d = 0$ V and the source terminal open during each measurement.

Based on the results presented above, we propose the following model to explain the degradation mode of the device during step-stress. At the beginning of the experiment, the field-emission tunneling from the metal into the semiconductor was negligible since the stress voltage is low.[11] However,

the electrons that tunnel from the gate electrode can conduct along the surface by a trap-to-trap hopping mechanism,[12] creating a gate-to-drain "surface leakage" path as shown in Fig. 4(a). As the step-stress experiment proceeds, traps may be randomly generated within AlGaN layer due to the high electric field under the edge of the gate. The electrons that tunnel from the gate electrode can inject into these traps at the very beginning of each voltage step, resulting in the increase of gate leakage current. Once the traps are all filled with negative charges, gate leakage current will decrease immediately, which explains the "recoverable" decrease of the stress current during each voltage step as denoted in Fig. 2. Besides, trap-assisted tunneling may be more and more significant as the stress voltage increases,[13] contributing to the increase of "permanent" stress current with stress time in Fig. 2.

Beyond the critical voltage ($V_g = -35$ V), crystallographic defects can form in the AlGaN barrier due to the inverse piezoelectric effect.[14] When the defects in the AlGaN barrier become excessive, they overlap with each other and result in the generation of a leakage path between the gate and the channel as shown in Fig. 4(b). The electrons passing through the leakage path in the AlGaN barrier layer can lead to the sudden increase of gate leakage current and a permanent degradation of the device (as can be seen from both Fig. 2 and Fig. 3).

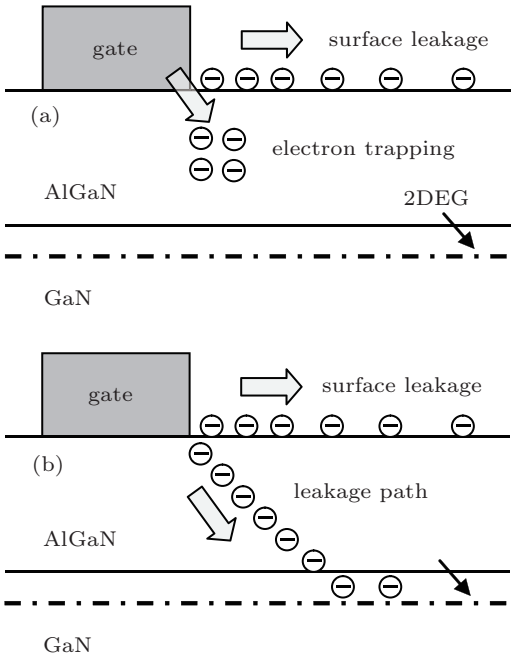


Fig. 4. Conceptual device degradation mechanism for reverse bias stress. (a) Before the "critical voltage" is reached, electrons injected into the traps in the AlGaN barrier layer result in the increase of stress current at the very beginning of each voltage step. (b) The leakage path is induced by the inverse piezoelectric effect at the "critical voltage", contributing to the permanent degradation of the device.

Since the source-to-gate distance (0.7 μm) is smaller than the drain-to-gate distance (2.5 μm) for the device used in our experiment, the leakage path should be first induced in the AlGaN layer near the source-side-edge of the gate due to the higher electric field there, which explains the sharp increase of source current beyond the "critical voltage" ($V_g = -35$ V) in Fig. 2.

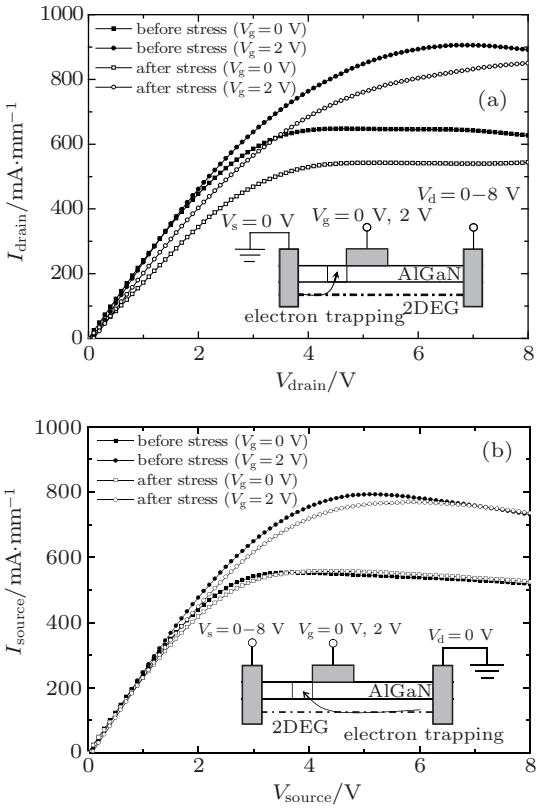


Fig. 5. Comparisons of output characteristics between before and after the step-stress experiment under different measurement schemes: (a) drain voltage V_d sweeping from 0 V to 8 V in 0.1 V/step while keeping source voltage $V_s = 0$ V and gate voltage $V_g = 0$ V /2 V, (b) source voltage V_s sweeping from 0 V to 8 V in 0.1 V/step while keeping drain voltage $V_d = 0$ V and gate voltage $V_g = 0$ V /2 V.

The output characteristics before and after the step-stress are compared in Fig. 5. Two different measurement schemes are used during the test of the output current: panel (a) drain voltage V_d sweeping from 0 V to 8 V in 0.1 V/step while keeping source voltage $V_s = 0$ V and gate voltage $V_g = 0$ V/2 V respectively, panel (b) source voltage V_s sweeping from 0 V to 8 V in 0.1 V/step while keeping drain voltage $V_d = 0$ V and gate voltage $V_g = 0$ V/2 V respectively. As can be seen, the maximum output current degrades apparently under measurement scheme (a) but degrades slightly under measurement scheme (b). This phenomenon can be explained as follows. A large number of traps may be induced in the AlGaN barrier layer near the source-side-edge of the gate during the stress experiment as shown in the inset in Fig. 5. When the channel is open and the drain electrode is positively biased, a large number of electrons coming from the source would be injected into the traps in the AlGaN barrier layer, contributing to the apparent decrease of the output current under measurement scheme

(a). But when the channel is open and the source electrode is positively biased, the electrons coming from the drain side would possess a high velocity after a long distance of acceleration and would be less easily to be trapped, which explains the slight degradation of the output current under measurement scheme (b).

4. Conclusions

In the present study, it is found that traps may be induced by the high electric field in the AlGaN barrier layer when the device is reversely biased. The electrons can be injected into the traps at the beginning of each voltage step and induce the recoverable decrease of stress current. Beyond a certain voltage, a leakage path may be generated in the AlGaN layer due to the inverse piezoelectric polarization effect, which can contribute to the sharp increase of gate leakage current and result in the permanent degradation of the device. Besides, the leakage path should be first induced under the source-side-edge of the gate electrode due to a higher electric field there. Thus changing device structures[15,16] to mitigate the electric field on the edge of the gate may improve the reliability of AlGaN/GaN HEMT.

References

[1] Tipirneni N, Koudymov A, Adivarahan V, Yang J, Simin G and Asif Khan M 2006 *IEEE Electron Dev. Lett.* **27** 716

[2] Ibbetson J P, Fini P T, Ness K D, DenBaars S P, Speck J S and Mishra U K 2000 *Appl. Phys. Lett.* **77** 250

[3] Mishra U K, Shen L, Kazior T E and Wu Y F 2008 *Proc. IEEE* **96** 287

[4] Joh J and del Alamo J A 2008 *IEEE Electron Dev. Lett.* **29** 287

[5] Chang C Y, Douglas E A, Kim J, Lu L, Lo C F, Chu B H, Cheney D J, Gila B P, Ren F, Via G D, Cullen D A, Zhou L, Smith D J, Jang S and Pearton S J 2011 *IEEE Trans. Dev. Mater. Reliab.* **11** 187

[6] Mishra U K 2012 *IEEE International Reliability Physics Symposium, IRPS* 2012, April 15–19, 2012, Anaheim, CA, USA, p. 2C.1.1

[7] Ma X H, Jiao Y, Ma P, He Q, Ma J G, Zhang K, Zhang H L, Zhang J C and Hao Y 2011 *Chin. Phys. B* **20** 127305

[8] Meneghini M, Stocco A, Bertin M, Marcon D, Chini A, Meneghesso G and Zanoni E 2012 *Appl. Phys. Lett.* **100** 033505

[9] Fu L H, Lu H, Chen D J, Zhang R, Zheng Y D, Wei K and Liu X Y 2012 *Chin. Phys. B* **21** 108503

[10] Shi L, Feng S W, Guo C S, Zhu H and Wan N 2013 *Chin. Phys. B* **22** 027201

[11] Miller E J, Yu E T, Waltereit P and Speck J S 2004 *Appl. Phys. Lett.* **84** 535

[12] Trew R J, Green D S and Shealy J B 2009 *IEEE Microwave Mag.* **10** 116

[13] Sudharsanan S and Karmalkar S 2010 *J. Appl. Phys.* **107** 064501

[14] Joh J, Xia L and del Alamo J A 2007 *IEEE International Electron Devices Meeting, IEDM'*07, December 10–12, 2007, Piscataway, NJ, USA, p. 385

[15] Kong X, Wei K, Liu G G and Liu X Y 2012 *Chin. Phys. B* **21** 128501

[16] Xie G, Tang C, Wang Tao, Guo Q, Zhang B, Sheng K and Wai T N 2013 *Chin. Phys. B* **22** 026103