A simple and accurate method for measuring program/erase speed in a memory capacitor structure*

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With the merits of a simple process and a short fabrication period, the capacitor structure provides a convenient way to evaluate memory characteristics of charge trap memory devices. However, the slow minority carrier generation in a capacitor often makes an underestimation of the program/erase speed. In this paper, illumination around a memory capacitor is proposed to enhance the generation of minority carriers so that an accurate measurement of the program/erase speed can be achieved. From the dependence of the inversion capacitance on frequency, a time constant is extracted to quantitatively characterize the formation of the inversion layer. Experimental results show that under a high enough illumination, this time constant is greatly reduced and the measured minority carrier-related program/erase speed is in agreement with the reported value in a transistor structure.

Keywords: memory capacitor, program/erase speed, minority carrier generation, illumination

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1. Introduction

Owing to the advantages of low power consumption, multi-bit storage, and potential applications in three-dimensional (3D) integration, the charge trap memory (CTM) has attracted extensive attention in both the academic and the industrial fields.[1,2] Currently, a lot of effort has been made to evaluate the CTM gate stacks with various materials and architectures.[3,4] With the merits of a simple process and a short fabrication period, the capacitor structure provides a convenient way to evaluate memory characteristics such as program/erase (P/E) speed, data retention and endurance. Different from the transistor structures in which the source and drain can provide minority carriers to the channel, the capacitor structures may have a very long formation time of the inversion layer due to the very slow thermal generation process for minority carriers.[5] During a fast program for an n-channel capacitor (or a fast erase for a p-channel one), the minority carrier generation may not be able to follow the gate bias pulse, which results in an inaccurate measurement of minority carrier-related P/E speed in the memory capacitor structure.

In this paper, we propose a simple and accurate method for measuring the P/E speed in the memory capacitor structure using light illumination. It includes the characterization of light intensity dependent formation time of the inversion layer and the comparison between the minority carrier-related P/E speed under high light illumination and literature reported values in transistor structures.

2. Effect of slow minority carrier generation time in memory capacitors

Following the conventional notation in this paper we refer to capacitors on p- and n-type Si substrates as n- and p-channel capacitors, respectively. In the inversion regime, the P/E operation of the memory capacitor depends on both the electric field in the tunneling layer and the density of minority carriers.[6] Due to the slow generation rate of minority carriers, the memory capacitor may enter into a non-equilibrium state. In such a state the voltage drops across the gate stack and the Si substrate are different from those in a thermal equilibrium state. Thus the P/E transients are also different. As an example, we calculate the voltage drop V_{ox} across the gate stack versus the substrate donor doping in a p-channel capacitor under the thermal equilibrium and the deep depletion conditions. In the calculation, it is assumed that there are no inversion carriers so that the capacitor is in the deep depletion condition (the fully non-equilibrium case).[7] The equivalent oxide thickness (EOT) of the capacitor is taken to be 15 nm, and the work function of the Al gate electrode is adopted as 4.08 eV. The gate bias is fixed at $V_g = -15$ V. Figure 1 shows the results of such a model calculation. It can be seen that under the deep depletion condition, most of the gate bias drops across

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the depletion layer in the n-type Si substrate. Particularly, V_{ox} is very small at the low substrate doping. If such a deep depletion happens in a p-channel memory capacitor during an erase operation, the device will not be erased. A high electric field in the gate stack is necessary for the erase operation. The absence of minority carriers (holes) in the channel leads to only a very small electric field in the charge trapping layer and the tunneling oxide. In the real cases, whether the capacitor enters into the fully non-equilibrium state depends on the generation rate of minority carriers[8] in the Si substrate and the dc gate bias sweep rate. So, quickly forming enough minority carriers in the channel in the inversion regime is indispensable to correctly measure the minority carrier-related program/erase speed in a memory capacitor structure.

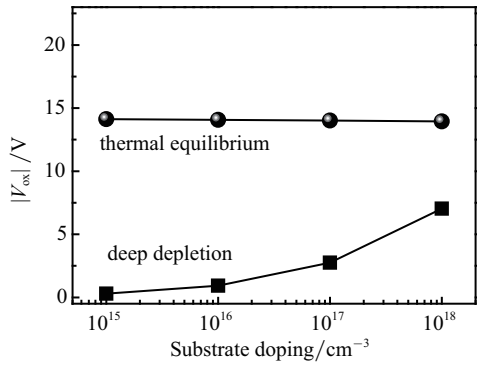


Fig. 1. Model calculated absolute values of oxide voltage V_{ox} versus the substrate acceptor doping for a p-channel capacitor (EOT = 15 nm and $V_g = 15$ V) under the thermal equilibrium and the deep depletion (fully non-thermal equilibrium) conditions.

In order to enhance the minority carrier generation rate in a memory capacitor, illumination[9,10] is employed during the P/E transient measurement. Figure 2 presents a scheme to measure erase transient characteristics for a p-channel memory capacitor under illumination. During an erase operation, a negative pulse signal is applied to the capacitor with a steady light illumination. The electron–hole pairs are generated around the capacitor. Some photo-generated holes may diffuse into the channel area beneath the Al gate pattern from the sidewall of the depletion region and respond quickly to the gate voltage pulse.

The illumination has two effects. In the first one, photo-generated minority carriers in the channel screen the electric field generated by charge in the gate electrode and make the depletion thickness in the Si substrate saturate so that most of the gate voltage drops across the gate stack. Thus, in the tunneling layer, there is a large electric field, which is very helpful for electrons to de-trap during an erase or to inject during a program. In the second one, the existence of a large number of photo-generated minority carriers can give rise to a high injection current, which is due to the fact that minority carriers themselves may participate in both program and erase processes.[6] Both effects increase the program/erase speed, so controlling and measuring the minority carrier generation rate are very important for accurate P/E speed measurement in memory capacitors. In order to simplify the problem, we focus on the minority carriers in the channel and assume that their density is uniform with only a small deviation from equilibrium. In this way, we can ignore the specific processes of generation and diffusion of minority carriers, and describe their effects using a relaxation time τ, which can be thought of as the formation time of the inversion layer. In what follows, we employ multifrequency capacitance–voltage (C–V) measurement to extract τ using a relaxation model.[11]

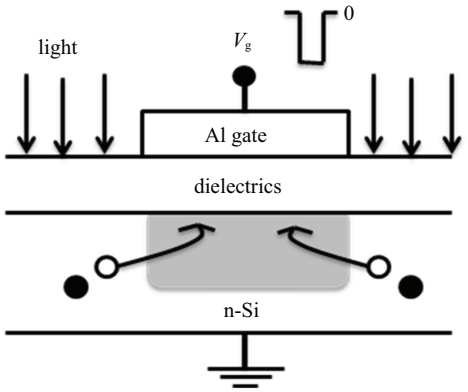


Fig. 2. Electron–hole pair generation under light illumination around a p-channel MANOS capacitor during an erase operation and subsequent hole diffusion to the channel beneath the Al gate pattern.

3. Experiment

Memory capacitors with gate stack of Al–Al_2O_3–Si_3N_4–SiO_2–Si (MANOS) structure were fabricated on n- and p-Si substrates respectively. After a standard cleaning, a 4 nm tunnel oxide (SiO_2) was thermally grown at 900 °C in dry O_2. A 7 nm Si_3N_4 film was formed on the tunneling oxide by a low-pressure chemical vapor deposition. The Al_2O_3 blocking layer was deposited on the Si_3N_4 film by atomic layer deposition using trimethylaluminum and H_2O as the precursor at a substrate temperature of 250 °C. The nominal thicknesses of Al_2O_3 for capacitors on n- and p-type Si substrates were 15 nm and 10 nm, respectively. Next, post-deposition annealing was performed at 1050 °C/60 s in N_2 ambient. After that, a 200 μm × 200 μm Al gate electrode with a thickness of 200 nm was deposited on the blocking oxide using the electron beam evaporation and patterned through a lift-off process. Then, a 200 nm Al film was deposited on the backside of the Si wafer. Finally, annealing was performed at 400 °C for 10 min in N_2 ambient to make the backside Ohmic contact.

The electrical characteristics were measured by using an Agilent Semiconductor Device Analyzer (B1500A) at room temperature. A He–Ne laser was used as the illumination light

source. A rotating attenuator was used to vary the illumination intensity. In order to make light perpendicularly incident on the memory capacitor, a small 45°-tilted reflecting mirror was used to change the light direction by 90°. The beam spot area was about 4.7 mm^2, which was much larger than the capacitor area (0.04 mm^2). The position of the beam spot was adjusted so that its center was on the Al gate electrode of the measuring memory capacitor. The calculated reflection rates of the gate stack were 31.5% for the n-channel capacitors and 30% for the p-channel ones. From these data, it is easy to obtain the area power density P_a of laser illumination absorbed in the Si substrate. In the following, P_a is used to characterize the memory property of the capacitor.

4. Results and discussion

4.1. Extracting the formation time of the inversion layer

Figures 3(a) and 3(b) show the multi-frequency C–V curves of p-channel and n-channel MANOS capacitors in the dark and under illumination with $P_a = 6$ mW/cm^2. For the p-channel capacitor in the dark, the C–V curves overlap together from 1 kHz to 1 MHz showing little inversion carrier generation, so the p-channel device may enter into deep depletion. For the n-channel MANOS capacitor in the dark, a clear change of inversion capacitance with frequency is seen. Under the illumination of $P_a = 6$ mW/cm^2, for a given frequency the inversion capacitance increases a lot for the two MANOS capacitors. It means that more minority carriers are generated under illumination. As discussed above, the formation time of the inversion layer is an important quantity for accurate P/E speed measurement, so this time is extracted for the MANOS capacitors in the dark and under varying illumination. Based on the relaxation time model, the evolution of inversion charge q_i can be written as[12]

$$\mathrm{d}q_i/\mathrm{d}t = -(q_i - q_{i0})/\tau, \tag{1}$$

where τ is the relaxation time, and q_{i0} denotes the quasiequilibrium value of q_i. As shown in the Schroder's theory of transient capacitance (C–t) test,[13,14] there are a few mechanisms for the thermal generation of the minority carriers: Si/SiO$_2$ interface generation, thermal generation inside the depletion region and from its sidewall, and thermal generation from the bottom bulk neutral region in one diffusion length of the minority carriers. In Eq. (1), the effects of all these generation mechanisms are lumped into the relaxation time τ. Using this equation and the theory of small signals, Zhu[11] has derived the following equation for the dependence of capacitance on frequency in the inversion regime:

$$C_{inv}(\omega) = C_{hf} + (C_{qe} - C_{hf})/[1 + (\omega\tau)^2]. \tag{2}$$

Here ω is the angular frequency; C_{qe} and C_{hf} are quasi-static and high-frequency capacitances, respectively. The validity of Eqs. (1) and (2) requires that the inversion charge density can follow the dc component of the gate voltage. The lowest frequency of our B1500A is 1 kHz. Thus if the measured C_{inv} (1 kHz) is near C_{qe} in our experiment, Eqs. (1) and (2) can be thought to be valid. Theoretically, C_{qe} should be almost the same as the capacitance in the strong accumulation regime. Although Eq. (1) is originally proposed for the thermal generation of minority carriers, it is still a good approximation when light is illuminated around a capacitor. In this case, the minority carriers can be thought to be generated from the sidewall of the depletion region.

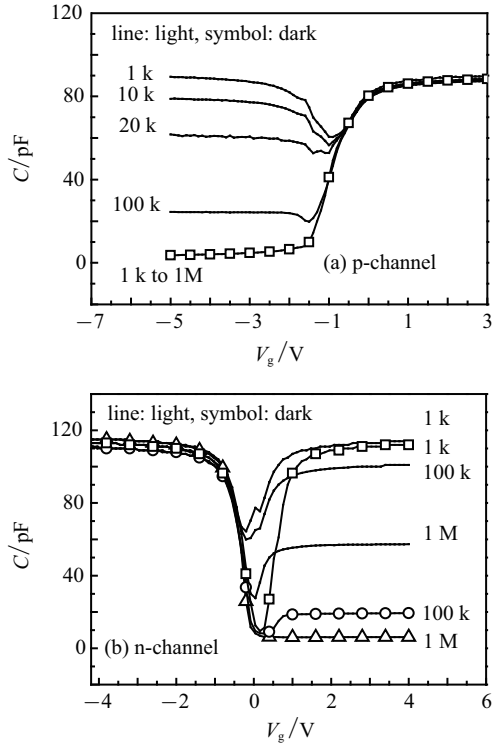


Fig. 3. Multi-frequency C–V curves for (a) p-channel and (b) n-channel MANOS capacitors in the dark and under light illumination.

Figure 4 shows the fittings of the inversion capacitance (in Fig. 3) to Eq. (2) in the dark and under illumination. For the p-channel MANOS capacitor, the τ value is estimated to be larger than 1 ms in the dark, as C_{inv} is very small even at 1 kHz. Under the illumination with $P_a = 6$ mW/cm^2, the τ value decreases to 6.58 μs. For the n-channel MANOS capacitor, the τ value is 0.76 μs under illumination, which is much smaller than 6.5 μs in the dark. Figure 5 shows the τ values for p- and n-channel devices versus the absorbed light intensity P_a. For both MANOS capacitors, τ first decreases and then becomes saturated with P_a increasing. The saturated τ value is about 0.3 μs, which is limited by the minority carrier recombination lifetime and the diffusion constant. In order to achieve an accurate P/E measurement, P_a should be large enough to make τ reach the saturation value.

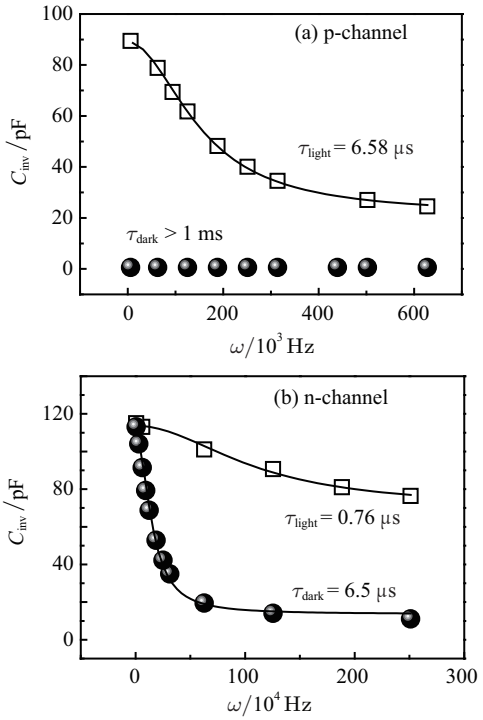


Fig. 4. Measured inversion capacitance values (symbols) versus frequency and the corresponding fittings (lines) to Eq. (2) for (a) p-channel and (b) n-channel MANOS capacitors.

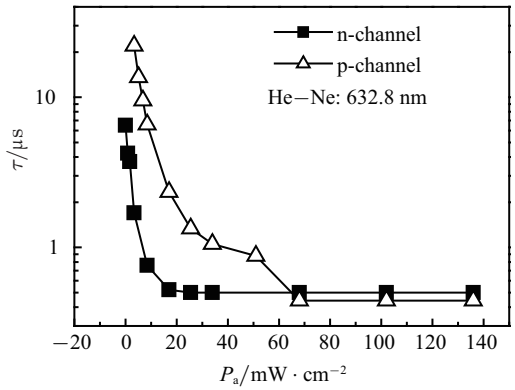


Fig. 5. Dependences of τ on the absorbed light intensity P_a for p- and n-channel MANOS capacitors.

4.2. Comparison of P/E transients in the dark and under illumination

As discussed above, τ becomes saturated at high incident intensity illumination. If this saturated τ value is much smaller than the width of the gate voltage pulse, then the measured P/E speed is considered to be accurate. In order to prove this point, the minority carrier-related P/E speeds of the two MANOS capacitors are measured in the dark and under the illumination with $P_a = 70$ mW/cm^2. The results are presented in Fig. 6. For the p-channel capacitor in the dark, it enters into the deep depletion in the inversion regime, so both the voltage drop across the gate stack and the minority carrier density in the channel are small. Due to these two facts, the p-channel MANOS capacitor cannot be erased at all.[15,16] However, under illumination, the p-channel capacitor can be easily erased. A TANOS device has the same gate dielectric stack as our MANOS structure, but it has a high work function TaN instead of the Al gate electrode.[6] Padovani *et al.*[6] have demonstrated that both electron detrapping and hole injection may happen in an erase operation in a TANOS device. In our two-terminal capacitor structure, we cannot separate the two processes from each other. However, under the light illumination, a high voltage drop across the gate stack and the existence of a large number of holes in the channel make these two processes possible. In the n-channel MANOS capacitor, a clear program is possible only for the voltage pulse longer than 0.1 ms in the dark. Under the light illumination, the program even starts for a program voltage pulse as short as 1 μs. It is due to the small saturated τ value (∼0.3 μs) under high light illumination.

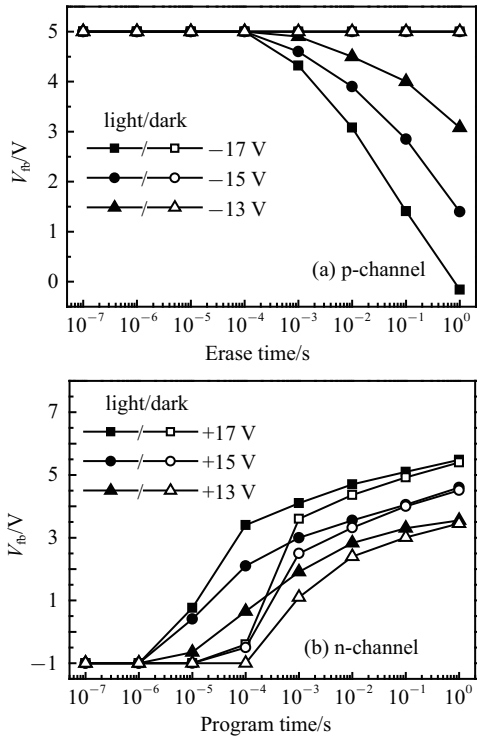


Fig. 6. (a) Erase transients for p-channel MANOS capacitor and (b) program transients for n-channel MANOS capacitor in the dark and under light illumination.

In order to examine the accuracy of the P/E speed measurement in our two-terminal MANOS capacitor (2T-CAP) under light illumination, we compare our P/E speed data under the Fowler–Nordheim (FN) injection with the literature-reported data measured from n-channel TANOS transistors (n-TANOS TR)[17] and a three-terminal (3T) p-channel TANOS capacitor (3T p-TANOS CAP).[6] In the 3T p-TANOS CAP, an n-type source contact was fabricated to provide minority carriers in the inversion regime. In Fig. 7, we plot the change of the threshold voltage for transistors or the flat-band voltage for capacitors in a certain time versus $E_{eff} = V_g$/EOT to quantify the

P/E speed. It can be seen that our P/E speed data under illumination are comparable to the literature data measured in the transistor structure. Therefore, our illuminated P/E speed data are very accurate. Some further remarks can be made on our illuminated P/E speed data. As a memory capacitor has only two terminals, only the FN injection is possible. For a memory transistor with four terminals, besides the FN injection, the injection of channel hot carriers or the band-to-band-tunneling induced hot carriers are also possible. As far as the FN injection is concerned, the carrier injection rates in a two-terminal memory capacitor and a four-terminal transistor should be almost the same provided that enough minority carriers can be formed quickly in the channel in the FN P/E processes.

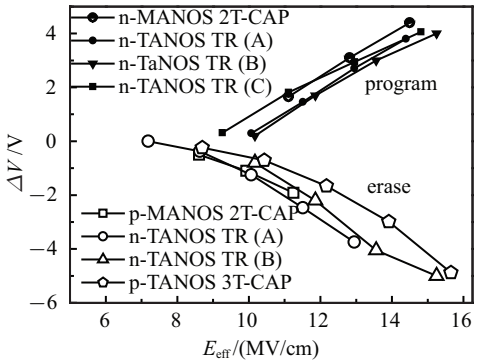


Fig. 7. Comparisons between P/E speed data in our p- and n-channel two-terminal MANOS capacitors (MANOS 2T-CAP) under illumination and those in the p-channel three-terminal TANOS capacitor (p-TANOS 3T-CAP)[6] and n-channel TANOS transistors (n-TANOS TR).[17] Here n-TANOS TR (A), n-TANOS TR (B), and n-TANOS TR (C) are the respective P/E speed data of devices A, B, and C in the reference. The program and erase times are 10^{-4} s and 10^{-2} s, respectively.

5. Conclusion

In this paper, a simple and accurate method is proposed to measure the minority carrier-related program/erase speed in a memory capacitor structure by using light illumination. The formation time of the inversion layer is extracted from the multi-frequency *C–V* measurement. It first decreases and then becomes saturated at high illumination intensity. The results show that under high enough light illumination, the minority carrier-related P/E speed in the memory capacitor increases a lot and is comparable to the literature-reported values measured in transistor structures.

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