High-power SiC MESFET using a dual p-buffer layer for an S-band power amplifier*

Deng Xiao-Chuan(邓小川)†, Sun He(孙 鹤), Rao Cheng-Yuan(饶成元), and Zhang Bo(张 波)

State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China

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A silicon carbide (SiC) based metal semiconductor field effect transistor (MESFET) is fabricated by using a standard SiC MESFET structure with the application of a dual p-buffer layer and a multi-recessed gate to the process for an S-band power amplifier. The lower doped upper-buffer layer serves to maintain the channel current, while the higher doped lower-buffer layer is used to provide excellent electron confinement in the channel layer. A 20-mm gate periphery SiC MESFET biased at a drain voltage of 85 V demonstrates a pulsed wave saturated output power of 94 W, a linear gain of 11.7 dB, and a maximum power added efficiency of 24.3% at 3.4 GHz. These results are improved compared with those of the conventional single p-buffer MESFET fabricated in this work using the same process. A radio-frequency power output greater than 4.7 W/mm is achieved, showing the potential as a high-voltage operation device for high-power solid-state amplifier applications.

Keywords: dual p-buffer layer, silicon carbide, MESFETs, electron confinement

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1. Introduction

The silicon carbide (SiC) based metal semiconductor field effect transistor (MESFET) is considered to be an excellent candidate for high power, high frequency, and high temperature applications in commercial and military communications due to its superior properties like the wide bandgap (3.26 eV), high breakdown field (3 MV/cm), large thermal conductivity (4.9 W/cm·K), and high electron saturation velocity (2×10^7 cm/s).[1–3]

The p-buffer layer is widely used in the SiC MESFET to isolate the semi-insulating substrate from the active channel.[4–6] Optimizing buffer thickness and doping is critical to realizing the control function of the buffer. However, a conventional low-doped p-buffer SiC MESFET exhibits high output conductance induced by the poor electron confinement in the channel region that enhances the probability of electron trapping in the buffer and substrate, and thus causes a leakage current and degrades the gain and output power. A high-doped p-buffer can solve the problem of the lightly-doped p-buffer but significantly reduces the maximum drain current, which results in a larger channel width and a higher doping concentration required to compensate the decreasing current. Hence the p-buffer layer needs to be carefully designed in order to provide the necessary channel isolation while not hindering the high-frequency device operation by introducing significant parasitic capacitance and drain leakage current.[7,8] However, only a few studies of p-buffer layer configuration in the SiC MESFET have been performed up to now.[9,10] Konstantinov *et al*.[11] presented a lateral epitaxial MESFET with a highly doped p-buffer layer only under the gate contact to suppress the short channel effects while still possessing a high breakdown voltage. However, the fabrication of an n-type buried region and p^+ depletion stopper layer are often difficult, which increases the processing cost.

In this paper, we report the fabrication of a high-power 4H-SiC MESFET employing a dual p-buffer layer on a high-purity semi-insulating (HPSI) substrate. The upper-buffer layer is of lower doping concentration and serves to provide a larger drain current, while the lower-buffer layer is of higher doping concentration which provides excellent electron confinement in the channel layer, resulting in improved power performance and reliability. The fabricated SiC MESFET with the dual p-buffer layer exhibits superior performance compared with the conventional single p-buffer layer device.

2. Device structure and fabrication

The proposed power MESFET in this work, as shown in Fig. 1, was fabricated on a 3-in-diameter 4H-SiC HPSI wafer. The epi stack consisted of a 0.8 μm p-type higher doped lower-buffer layer ($N_a = 5\times10^{16}$ cm^{-3}) and a 0.4 μm p-type lower doped upper-buffer layer (the peak concentration $N_a = 2\times10^{16}$ cm^{-3}), followed by a 0.35 μm n-type channel layer ($N_d = 3\times10^{17}$ cm^{-3}) and a 0.15 μm highly doped n-type cap layer ($N_d = 1.5\times10^{19}$ cm^{-3}). The doping concentration and the thickness were obtained directly from secondary ion mass spectroscopy (SIMS) analysis. The SIMS profiling, as shown in Fig. 2, was obtained from special test wafers grown prior to the wafers for the device fabrication. A

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†Corresponding author. E-mail: xcdeng@uestc.edu.cn

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multi-recessed gate was used to improve the output power density and to alleviate the trapping induced instabilities by moving the current path away from the surface of the device.[12] The details of the process has been described previously.[13] In short, the processing included third mesa etching for determining the multi-recessed gate and device isolation, Ni ohmic contacts, air bridges, and thermally grown passivation oxide layer. The gate patterning was carried out using electron beam lithography, whereas the other steps used the standard contact photolithography. The etching was conducted using inductively coupled plasma (ICP) with fluorine-based plasma. A MESFET with a gate length of 0.8 μm and a gate periphery of 20 mm was made. For comparison, 24 mm gate periphery SiC MESFETs with a 2 μm p-type single buffer layer ($N_a = 5 \times 10^{15}$ cm^{-3}) and multi-recessed gate were fabricated and characterized.

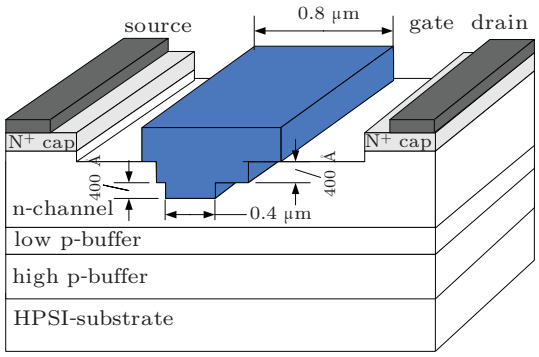


Fig. 1. (color online) Schematic cross-section of the proposed MESFET.

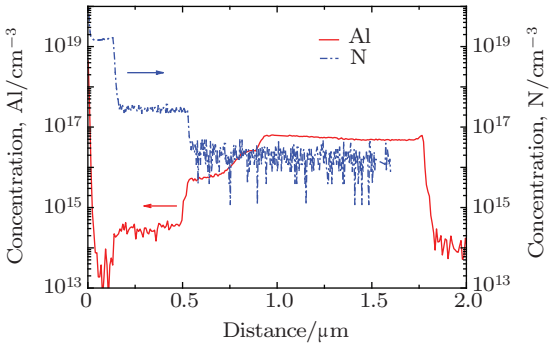


Fig. 2. (color online) SIMS measured aluminum acceptor and nitrogen donor profiles.

3. Results and discussion

The *I*–*V* characteristics of the devices are measured using a Keithley 4155 system. Figure 3 shows the drain current (I_{ds}) versus drain–source voltage (V_{ds}) measured for the dual p-buffer layer device at different values of gate bias voltage V_{gs}. The source contact is grounded, and the gate bias V_{gs} is varied from 0 V to −14 V. A saturation drain current (I_{dsat}) of 410 mA/mm and a gate-drain breakdown voltage larger than 200 V are measured for the 2×331 μm gate periphery SiC MESFET with dual p-buffer layer. The high breakdown voltage is mainly attributed to the reduced electric field peak at the bottom edge of gate toward the drain side by the extension of gate metal on the surface, which acts like a field plate resulting in a gradual field distribution. Furthermore, the higher-doped p-buffer layer suppresses the channel electron ejection that causes the buffer leakage current. Figure 4 shows the typical DC transfer characteristics of the device. The drain is biased at 25 V. The maximum extrinsic transconductance g_m is 33 mS/mm. The device pinches off completely at the gate bias of −14 V.

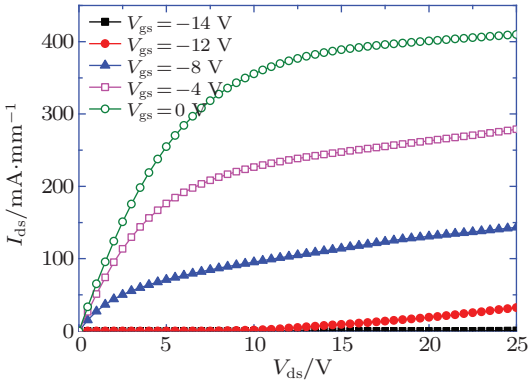


Fig. 3. (color online) Drain current versus drain voltage for 4H-SiC MESFET with dual p-buffer layer at different values of gate bias voltage V_{gs}.

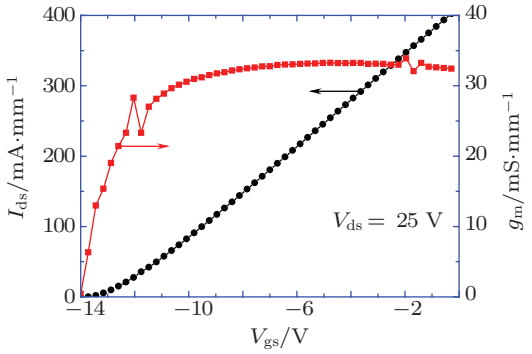


Fig. 4. (color online) DC transfer characteristics of SiC MESFET with dual p-buffer layer.

Figure 5 shows the SEM image of a 20-mm gate periphery SiC MESFET with dual p-buffer layer. The radio-frequency (RF) power testing is performed on an individually packaged 20-mm gate periphery SiC MESFET using pulsed waveform. The RF input is pulsed with 100 μs pulse width and 10% duty cycle at 3.4 GHz. The best results of peak power are shown in Fig. 6 for two different SiC MESFET devices made with the same process. The power sweeps from a dual p-buffer layer device operated at a drain bias of 80 V. Under the pulsed operation, the proposed MESFET presents a saturated output power of 94 W (4.7 W/mm), a linear gain of 11.7 dB, and a maximum power added efficiency (PAE) of 24.3%. For the

single buffer layer FET with 24-mm gate periphery, these values are 80 W (3.3 W/mm), 10.7 dB, and 25.8%, respectively. The high output power and gain are due to the fact that the dual buffer layer is used to improve the gate–drain breakdown voltage and to reduce the output conductance by confining the electron in the channel region to minimize the effects of deep level traps.

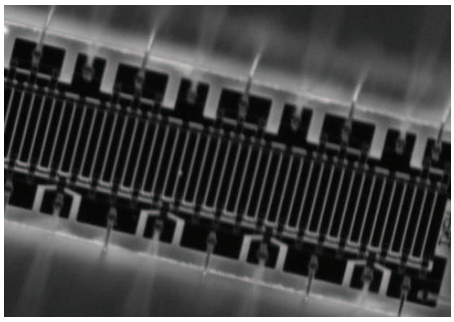


Fig. 5. SEM image of SiC MESFET with 20-mm gate periphery.

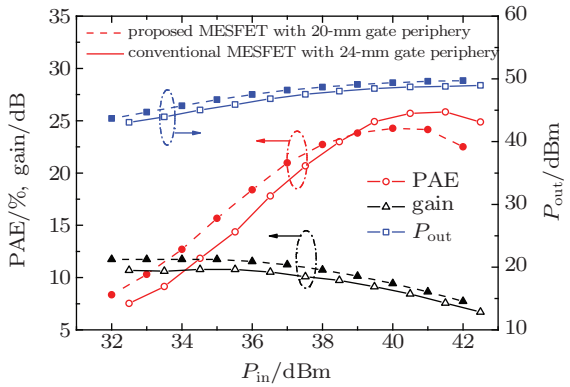


Fig. 6. (color online) The P_{out}, gain, and PAE versus P_{in} for SiC MESFETs with dual buffer layer and single buffer layer.

In order to clarify whether the channel current is confined in the channel layer, numerical device simulations are performed using Atlas from Silvaco with appropriate calibrated SiC parameters.[14,15] In addition to basic Poisson and the drift/diffusion equations, the different physical models used simultaneously in Silvaco are SRH (Shockley–Read–Hall) and Auger for generation and recombination, Analytic and Fldmob for mobility, Incomplete for incomplete ionization of dopants, and Impact Selb for impact ionization. Here the traps in the HPSI substrate are not considered. Figure 7 shows the simulated electron current density distributions under an applied drain bias of 40 V and a gate bias of −8 V for SiC MESFETs with a dual p-buffer layer (the basic parameters of the structure are determined from the SIMS measurement) and a single p-buffer layer (thickness 2 μm, doping concentration $N_a = 5 \times 10^{15}$ cm^{-3}); the same thickness and doping level in the n-type channel region are used for the two MESFETs.

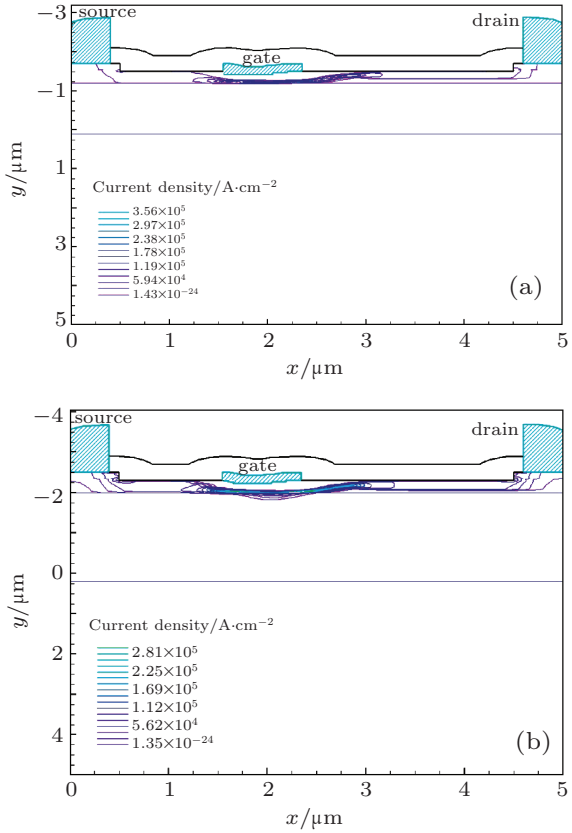


Fig. 7. (color online) Simulated drain current density distributions for SiC MESFETs with (a) dual p-buffer layer (b) conventional p-buffer layer.

From the simulation results, it is observed that channel electrons are injected into the conventional lightly doped p-buffer layer, which can be trapped and/or recombined in the buffer, thereby leading to a decreased channel current and a degraded reliability. The channel current, however, is not extended into the buffer region for the proposed MESFET. This is due to the fact that the highly doped p-buffer layer prohibits the channel electrons from reaching the deep level trap in the buffer. Therefore the dual p-buffer layer structure provides excellent electron confinement in the channel region, which results in improved power performance and reliability.

4. Conclusion

In this work, an SiC MESFET with dual p-buffer layer structure is successfully developed. Its experimental results are compared with those of the conventional p-buffer layer device fabricated using exactly the same process flow. A 20-mm gate periphery device with a dual p-buffer layer shows a pulse output power of 94 W (4.7 W/mm), a linear gain of 11.7 dB, and a maximum power added efficiency of 24.3% at 3.4 GHz. This represents a 1.4 W/mm and 1 dB improvement over the conventional device with lightly doped p-buffer layer. These improvements are explained by the excellent electron confinement in the channel region using the optimized p-buffer layer. Therefore, the 4H-SiC MESFET with dual p-

buffer layer has superior RF performances compared with similar devices based on the conventional structure.

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References

[1] Ostling M *2010 IEEE International Electron Devices Meeting,* December 6–8, 2010 San Francisco, USA, p. 1331

[2] Südow M, Andersson K, Billström N, Grahn J, Hjelmgren H, Nilsson J, Nilsson P, Ståhl J, Zirath H and Rorsman N 2006 *IEEE Trans. Microwave Theory and Techniques* **54** 4072

[3] Chen G, Qin Y, Bai S, Wu P, Li Z Y, Chen Z and Han P 2010 *Solid-State Electronics* **54** 353

[4] Sriram S, Hagleitner H, Namishia D, Alcorn T, Smith T and Pulz B 2009 *Electron Devices Letter* **30** 952

[5] Hjelmgren H, Allerstam F, Andersson K, Nilsson P and Rorsman N 2010 *IEEE Trans. Electron Devices* **50** 729

[6] Andersson K, Südow M, Nilsson P and Sveinbjörnsson E 2006 *IEEE Trans. Electron Devices Letters* **27** 573

[7] Los A V, Mazzola M S, Kajfez D, McDaniel B T, Smith C E, Kretchmer J, Rowland L B and Casady J B 2004 *Materials Science Forum* **457–460** 1193

[8] Frank G, Ravi C and Tom N 2002 *Microelectronics Reliability* **42** 1003

[9] Sankha S M and Syed S I 2004 *International Journal of High Speed Electronics and Systems* **14** 890

[10] Deng X C, Zhang B, Zhang Y R, Wang Y and Li Z J 2009 *Chin. Phys.* B **18** 3018

[11] Konstantinov A O, Harris C I and Ericsson P 2002 *Materials Science Forum* **389–393** 1375

[12] Deng X C, Li L, Zhang B, Mo J H, Wang Y, Wang Y and Li Z J 2011 *Electronics Letters* **47** 517

[13] Deng X C, Feng Z, Zhang B, Li Z J, Li L and Pan H S 2009 *Chin. Phys.* B **18** 3018

[14] Device Simulator Atlas2005 *Atlas User's Manual* Silvaco International

[15] Deng X C, Zhang B and Li Z J 2009 *Semicond. Sci. Technol.* **24** 015011