Parasitic bipolar amplification in single event transient and its temperature dependence*

Liu Zheng(刘 征)†, Chen Shu-Ming(陈书明), Chen Jian-Jun(陈建军), Qin Jun-Rui(秦军瑞), and Liu Rong-Rong(刘蓉容)

College of Computer, National University of Defense Technology, Changsha 410073, *China*

(Received 27 February 2012; revised manuscript received 26 April 2012)

Using three-dimensional technology computer-aided design (TCAD) simulation, parasitic bipolar amplification in single event transient (SET) current of single transistor and its temperature dependence are studied. We quantify the contributions of different current components in SET current pulse, and it is found that the proportion of parasitic bipolar amplification in total collected charge is about 30% in both 130-nm and 90-nm technologies. The temperature dependence of parasitic bipolar amplification and the mechanism of SET pulse are also investigated and quantified. The results show that the proportion of charge induced by parasitic bipolar increases with rising temperature, which illustrates that the parasitic bipolar amplification plays an important role in the charge collection of single transistor.

Keywords: single event transient, parasitic bipolar amplification, funnel-aided drift, temperature dependence

PACS: 94.05.Dd, 85.30.Tv, 02.60.Cb **DOI:** 10.1088/1674-1056/21/9/099401

1. Introduction

Radiation-induced soft errors have become one of the biggest reliability issues in defense and space systems. Single event effects (SEEs) in complex integrated circuits have become more serious with shrinking device size and increasing circuit frequency. It is well established that single event transient (SET) is a significant error mechanism in advanced complementary metal oxide semiconductor (CMOS) devices.[1−5]

The total charge collected is the sum of funnel-aided drift, diffusion, and bipolar amplification components in very deep sub-micro technologies.[6] Following a particle strike at the drain/well junction, numerous electron-hole pairs are generated along the ion track. Electrons can be collected quickly, and holes can only escape through the body contact or by recombination. Residual holes left in the well raise the well potential and lower the source/well potential barrier, and the source (S) injects electrons into the channel, which is controlled by the gate (G). These electrons can be amplified and collected by the drain (D), where they can add to the original particle-induced current ($I_{\rm ch}$) and cause an increased charge collection. This is the well-known parasitic bipolar amplification effect, where the source acts as the emitter (E), the bulk as the base (B) region, and the drain as the collector (C).[7] The corresponding current is $I_{\rm E}$, $I_{\rm B}$, and $I_{\rm C}$, and β is the amplification factor, as shown in Fig. 1.

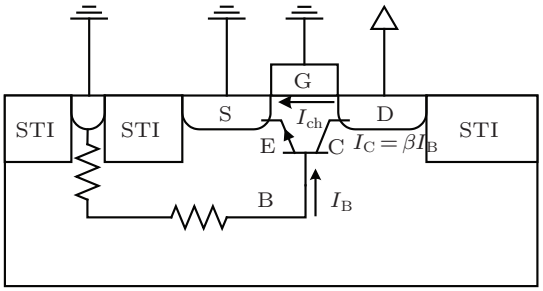


Fig. 1. Schematic of parasitic bipolar amplification.

Combinational logic soft errors are expected to be the dominant reliability issue for advanced technologies. One of the major factors affecting the soft-error rates is the single event transient.[8] As the primary mechanism of SEEs, charge collection has been the focus of research in recent years. Parasitic bipolar amplification induced by charge sharing has been studied in Refs. [9] and [10]. Three-dimensional technology computer-aided design (TCAD) models have been used in mixed-mode simulations to analyze the effect of well contacts at mitigating parasitic PNP bipolar conduction due to a direct hit ion

*Project supported by the National Natural Science Foundation of China (Grant Nos. 60836004, 61076025, and 61006070) and the Specialized Research Fund for the Doctoral Program of Higher Education of China (Grant No. 20104307120006).

†Corresponding author. E-mail: zhliu1982@hotmail.com

© 2012 Chinese Physical Society and IOP Publishing Ltd

strike.[11] A novel mechanism for upset is seen in a commercially available 0.25-μm 10-T SEE hardened static random-access memory (SRAM) cell.[12] This new mechanism involves direct drift–diffusion collection at an N-channel metal-oxide-semiconductor field-effect transistor (NMOS) transistor in conjunction with parasitic bipolar conduction in nearby P-channel metal-oxide-semiconductor field-effect transistor transistors. Ferlet-Cavrois and his coworkers experimentally showed that the drain junction of an off-state NMOS transistor collects more charge than an identical junction isolated from neighboring elements, and proved that the charge amplification effect was strong enough to invalidate usual charge collection models based only on funnel and diffusion transport.[13] Bipolar amplification effect in an inverter chain of SET is studied by three-dimensional (3D) mixed-mode simulation, which is compared with that in single NMOS. It is found that the bipolar amplification component accounts for a larger proportion in SET current pulse than in an inverter chain.[14]

This work compares different current components (including drift component, diffusion component, and parasitic bipolar amplification component) of SET pulse in detail between NMOS and PMOS in both 130-nm and 90-nm CMOS technologies. It is found that the proportion of parasitic bipolar amplification in total charge collected is about 30% in both technologies. The temperature dependence of the parasitic bipolar amplification and the mechanism of SET pulse are also investigated.

2. Simulation setup

Three-dimensional TCAD simulations are adopted in this work to calculate the SET current of NMOS/PMOS in 130-nm and 90-nm technologies. The bias conditions of single NMOS are consistent with usual biases of transistors sensitive to SEE (see Table 1). To neglect the parasitic bipolar conduction effect, we use a diode reversed biased (N-diode/P-diode)in place of the single transistor (NMOS/PMOS), in which case it only calculates $I_{\rm ch}$. It is the same as the NMOS/PMOS transistor except that the gate and source electrodes and the source doped junction are suppressed (the same setup as Ref. [14]).

In this paper, all simulations are conducted by commercial TCAD tools using the YINHE computing cluster. The size of the simulation structure is $10 \times 10 \times 10$ μm^3, as shown in Fig. 2, and the device contains about 2×10^5 grid points.

Table 1. The bias conditions of single NMOS for SET simulation. The voltage of power supply (VPS) is 1.2 V, the ground voltage (GV) is 0 V.

	Drain	Gate	Source	Substrate
NMOS@OFF	VPS	GV	GV	GV
N-diode	VPS	No	No	GV
PMOS@OFF	GV	VPS	VPS	VPS
P-diode	GV	No	No	VPS

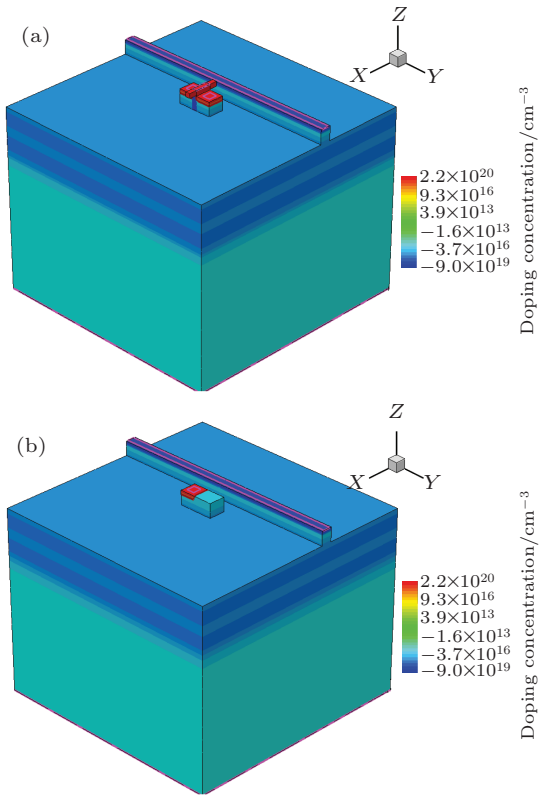


Fig. 2. (colour online) Device structures of (a) 130-nm NMOS and (b) N-diode.

For all simulations, the following physical models and parameters were used: (1) Fermi-Dirac statistics; (2) band-gap narrowing effect; (3) doping-dependent Shockley-Read-Hall (SRH) recombination and Auger recombination; (4) impacts of temperature, doping, electric filed, and carrier-carrier-scattering on the mobility. Due to no convergence induced by the complex physical temperature models, SET currents were calculated only from 260 K to 400 K in this paper; (5) incident heavy ions were modeled using a Gaussian radial profile with a characteristic 1/e radius of 0.1 μm and a Gaussian temporal profile with a characteristic decay time of 250 fs. The linear energy transfer (LET) used in all simulations is 60 MeV·cm^2/mg, and the position of incidence is the center of drain.

The process models in this work refer to 130-nm and 90-nm bulk CMOS processes of a foundry in China. To calibrate the doping profiles within the 3D device model, we used process simulation and

an inverse modeling approach.[6,15−20] The 3D device model was verified before simulations. The 3D simulation results is in good agreement with the I–V characteristics based on simulation program with integrated circuit emphasis integrated circuit emphasis (SPICE) model parameters, which are provided by the foundry. This model and method have been used and validated in recent papers of our group.[16−20]

3. Results and discussion

3.1. Comparison of NMOS in different technologies

The SET current of single NMOS under OFF bias (NMOS@OFF) is plotted in Fig. 3, together with that of N-diode. In Fig. 4, the collected charge is the integral of corresponding curve in Fig. 3.

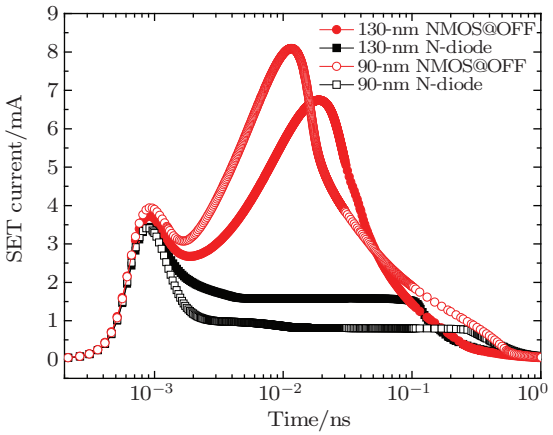


Fig. 3. (colour online) SET current pulses of NMOS@OFF and N-diode.

According to the conclusion in Ref. [14], the first peak of SET current is judged as the funnel-aided drift component, with little relation with source. As shown in Fig. 3, the peak value of bipolar amplification component in 90-nm NMOS@OFF is higher, starts earlier, and lasts longer than that in 130-nm NMOS@OFF. Therefore, in this case the charge collected is more than that in 130-nm NMOS@OFF. This is mainly due to the bipolar amplification component before 0.5 ns. After 1 ns, the charge collected by N-diode is more than that of NMOS@OFF, which is obvious in 130-nm technology. The reason is that in the case of NMOS@OFF, there is a small current I_{B} in the base of parasitic bipolar to deplete the electron–hole pairs in the substrate. On the contrary, the N-diode has a little more electron–hole pairs to collect in the following diffusion period.

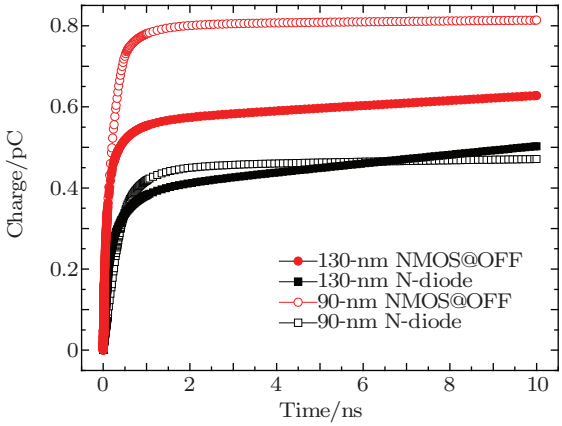


Fig. 4. (colour online) Collected charges of NMOS@OFF and N-diode.

To investigate the influence of technology scaling on the charge collection and parasitic bipolar amplification, we compare two shapes of SET current in both technologies. With decreasing device sizes, narrower channel means narrower base of parasitic bipolar transistor, which results in a larger amplification factor and increases the charge collected.

Using the logarithmic coordinate system, it is easy to find out the property of SET current shape. To explore the respective contributions of different current components in the charge collection, the SET current pulse of NMOS@OFF is divided into 3 parts, as shown in Fig. 5. The two curves firstly intersect at x_0 and the area enclosed by $I_{\mathrm{N-diode}}$ curve, $x = x_0$, and x axes is defined as Q1, which is considered as collected charge induced by the funnel-aided drift; the area Q2 is regarded as the component of parasitic bipolar amplification; the third part Q3 is regarded as the diffusion part. From the above discussions, the SET current of N-diode is mainly used to calibrate the bipolar amplification part. It has a little

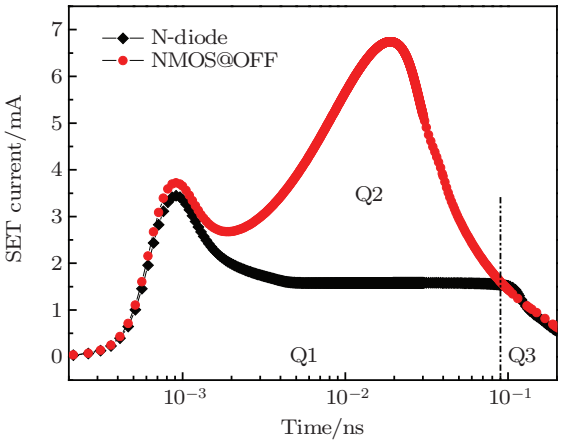


Fig. 5. (colour online) Different mechanisms of charge collection. Q1: funnel-aided drift part; Q2: bipolar amplification part; Q3: diffusion part.

difference with common NMOS@OFF in Q3 region. To evaluate the real diffusion part in common NMOS, the third part is defined by NMOS@OFF curve.

The normalization therefore makes the comparison of different components and devices of different technologies and types possible. As shown in Figs. 6 and 7, in both technologies, they almost have the same percentage of about 30%, which means that the parasitic bipolar amplification effect has the same contribution to the final total charge collected. In the process of charge collection, 90-nm NMOS@OFF has a slightly more share and a greater absolute value of collected charge induced by bipolar amplification than 130-nm NMOS@OFF. The primary difference of the two figures is the proportions of funnel-aided drift and diffusion, which is mainly due to the different time points when $I_{\mathrm{N-diode}} = I_{\mathrm{NMOS@OFF}}$. As discussed above, the bipolar amplification effect in 90-nm NMOS@OFF lasts a longer time than 130-nm NMOS@OFF (0.09 ns for 130 nm and 0.5 ns for 90 nm). All these results indicate that all the mechanisms of charge collection interact more with each other in the smaller feature size.

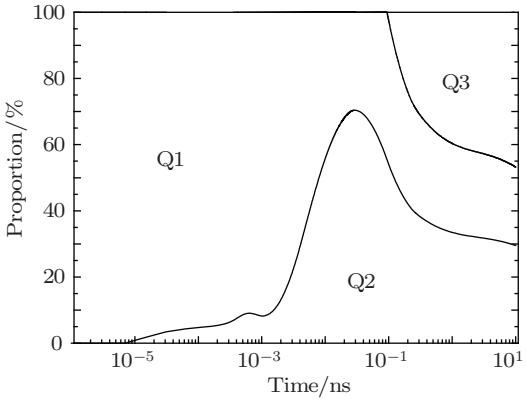


Fig. 6. Proportions of different collected charges in 130-nm NMOS.

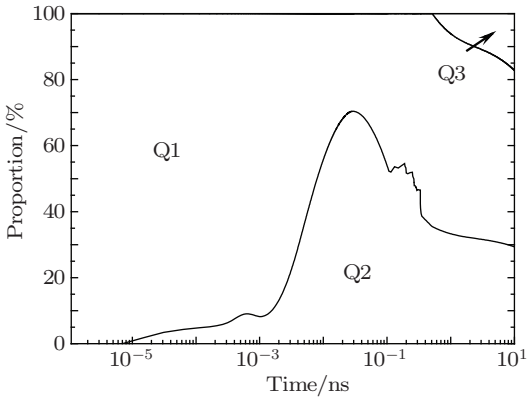


Fig. 7. Proportions of different collected charges in 90-nm NMOS.

3.2. Comparison of the bipolar amplification current in PMOS and NMOS

As shown in Figs. 8 and 9, the SET current of PMOS almost has a symmetrical shape and collects less charge than that of NMOS because the N-well of PMOS cuts off the path of charge collection. A portion of electron–hole pairs is blocked by the N-well doping, which influences the collection of parasitic bipolar amplification and funnel-aided drift. As a result, the collected charge of PMOS is about 0.1 pC, which is less than that of NMOS before 0.5 ns.

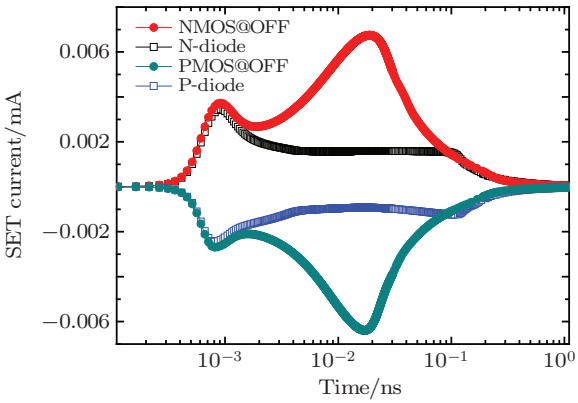


Fig. 8. (colour online) SET currents of 130-nm NMOS/PMOS.

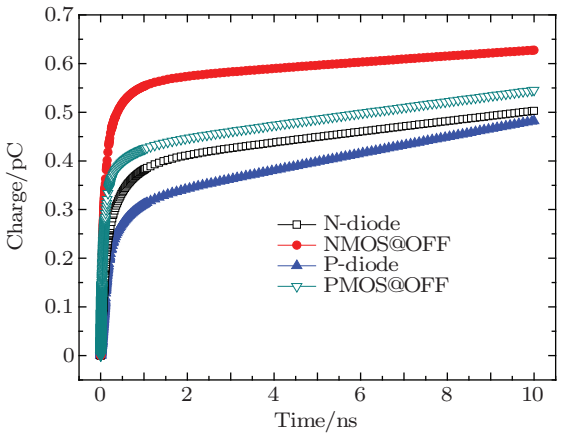


Fig. 9. (colour online) Collected charge of 130-nm NMOS/PMOS.

By comparing contributions of components in 130-nm NMOS and PMOS, we find that at the beginning ($< 10^{-5}$ ns) and the peak of charge collection, the bipolar contribution of PMOS (80%) is more significant than that of NMOS (70%). Though in the end of the charge collection (10 ns), they have similar proportion (30%), we can reach a conclusion that the parasitic bipolar amplification of PMOS plays a more

significant role than that of NMOS, which is in good agreement with Ref. [6].

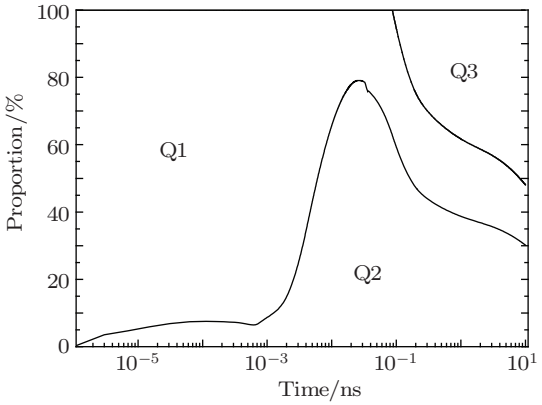


Fig. 10. Proportions of different collected charges in 130-nm PMOS.

4. Temperature dependence of the parasitic bipolar amplification

As shown in Fig. 11, areas Q1 and Q2 show different trends with increasing temperature in the range from 260 to 400 K, the funnel-aided drift (bipolar amplification) is inversely (proportional) to the temperature. Therefore, in the range from 260 to 400 K, the proportion of Q2 rises from 48.4% to 67.735%, which shows that the temperature is of great significance for the bipolar amplification effects. This is consistent with the conclusion in Ref. [16].

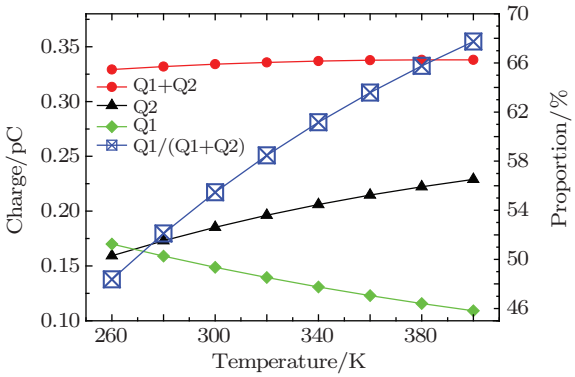


Fig. 11. (colour online) Temperature dependence of different collected charges in 130-nm NMOS.

The drift collection depends on the carrier velocity which is a complex function of mobility and electric field strength. The carrier mobility decreases with increasing temperature, resulting in less charge collected by drift. The electron mobility decreases with rising temperature. When temperature increases from 260 to 400 K, the mobility decreases from 350 to 149.5 $cm^2/V{\cdot}s$.[16] The enhancement of bipolar amplification with increasing temperature can be explained as follows. The resistance between the body contact and the bulk under the gate increases with increasing temperature, resulting in a higher well potential and corresponding larger bipolar amplification.

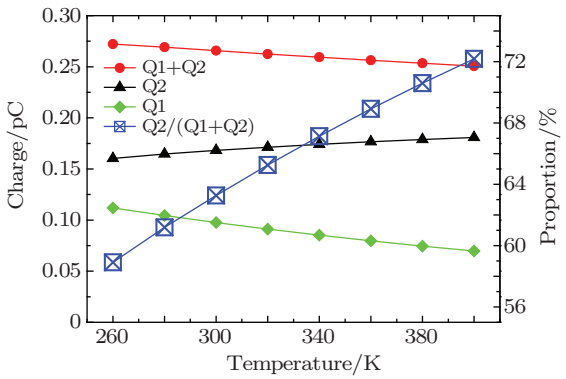


Fig. 12. (colour online) Temperature dependence of different collected charges in 130-nm PMOS.

Similar conclusion is applicable for the 130-nm PMOS. The only difference with the NMOS is the decreased sum of Q1 and Q2 due to reduced drift collection. As shown in Fig. 12, the Q2 portion increases from 58.912% to 72.178% in the range from 260 to 400 K. The increased value is 13.275%, which is less than that for NMOS (19.335%). This supports the conclusion that the temperature influence on the bipolar effect of PMOS is less than that of NMOS.

5. Conclusion

Parasitic bipolar amplification in SET current of single NMOS/PMOS and its temperature dependence have been analyzed. Contributions of different current components in the SET current pulse are concluded and quantified. It is found that the parasitic bipolar amplification proportion in total charge collected is about 30% in both 130-nm and 90-nm technologies. Moreover, the temperature dependence of the parasitic bipolar amplification and its mechanism are also studied and quantified. The results indicate that the proportion of charges induced by parasitic bipolar increases with rising temperature, which shows that the parasitic bipolar amplification plays an important role in the charge collection of single transistor.

In this paper, different components and mechanisms (funnel-aided drift, parasitic bipolar amplification, diffusion) of the SET current pulse have been

studied, which are very helpful to derive the accurate analytical model of SET in deep-submicron CMOS circuit.

References

[1] Benedetto J M, Eaton P H and Mavis D G 2006 *IEEE Trans. Nucl. Sci.* **53** 3462

[2] He C H, Geng B, Yang H L, Cheng Z H, Wang Y P and Li G Z 2003 *Acta Phys. Sin.* **52** 180 (in Chinese)

[3] He C H, Geng B, He B P, Yao Y J, Li Y H, Peng H L, Lin D S, Zhou H and Chen Y S 2004 *Acta Phys. Sin.* **53** 194 (in Chinese)

[4] Zhang Q X, Hou M D, Liu J, Wang Z G, Jin Y F, Zhu Z Y and Sun Y M 2004 *Acta Phys. Sin.* **53** 566 (in Chinese)

[5] Li H 2006 *Acta Phys. Sin.* **55** 3540 (in Chinese)

[6] Amusan O A, Witulski A F, Massengill L W, Bhuva B L, Fleming P R, Alles M L, Sternberg A L, Black J D and Schrimpf R D 2006 *IEEE Trans. Nucl. Sci.* **53** 3253

[7] Dodd P E and Massengill L W 2003 *IEEE Trans. Nucl. Sci.* **50** 583

[8] Gadlage M J, Ahlbin J R, Narasimham B, Ramachandran V, Dinkins C A, Pate N D, Bhuva B L, Schrimpf R D, Massengill L W, Shuler R L and McMorrow D 2010 *IEEE Tran. Device Mater. Rel.* **10** 157

[9] Amusan O A, Massengill L W, Baze M P, Bhuva B L, Witulski A F, Black J D, Balasubramanian A, Casey M C, Black D A, Ahlbin J R, Reed R A and McCurdy M W 2008 *Proceeding of the 46th Annual IEEE International Reliability Physics Symposium* April 27-May 1, 2008 Phoenix, USA, p. 468

[10] Wissel L, Oldiges P and Guo D 2010 *IEEE Trans. Nucl. Sci.* **57** 3234

[11] Olson B D, Amusan O A, Dasgupta S, Massengill L W, Witulski A F, Bhuva B L, Alles M L, Warren K M and Ball D R 2007 *IEEE. Trans. Nucl. Sci.* **54** 894

[12] Olson B D, Ball D R, Warren K M, Massengill L W, Haddad N F, Doyle S E and McMorrow D 2005 *IEEE Trans. Nucl. Sci.* **52** 2132

[13] Ferlet-Cavrois V, Vizkelethy G, Paillet P, Torres A, Schwank J R, Shaneyfelt M R, Baggio J, du Port de Pontcharra J and Tosti L 2004 *IEEE Trans. Nucl. Sci.* **51** 3255

[14] Liu Z, Chen S M, Liang B, Liu B W and Zhao Z Y 2009 *Acta Phys. Sin.* **59** 649 (in Chinese)

[15] Turowski M, Raman A and Jablonski G 2007 *14th International Conference on Mixed Design of Integrated Circuits and Systems* June 21–23, 2007 Ciechocinek, Poland, p. 433

[16] Chen S M, Liang B, Liu B W and Liu Z 2008 *IEEE Trans. Nucl. Sci.* **55** 2914

[17] Chen S M and Chen J J 2012 *Chin. Phys.* B **21** 016104

[18] Chen J J, Chen S M, Liang B and Deng K F 2012 *Chin. Phys.* B **21** 016103

[19] Chen J J, Chen S M, Liang B, Liu B W, Chi Y Q, Qin J R and He Y B 2011 *Acta Phys. Sin.* **60** 086107 (in Chinese)

[20] Qin J R, Chen S M, Liang B and Liu B W 2012 *Chin. Phys.* B **21** 029401