SPICE modeling of memristors with multilevel resistance states*

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With CMOS technologies approaching the scaling ceiling, novel memory technologies have thrived in recent years, among which the memristor is a rather promising candidate for future resistive memory (RRAM). Memristor's potential to store multiple bits of information as different resistance levels allows its application in multilevel cell (MCL) technology, which can significantly increase the memory capacity. However, most existing memristor models are built for binary or continuous memristance switching. In this paper, we propose the simulation program with integrated circuits emphasis (SPICE) modeling of charge-controlled and flux-controlled memristors with multilevel resistance states based on the memristance versus state map. In our model, the memristance switches abruptly between neighboring resistance states. The proposed model allows users to easily set the number of the resistance levels as parameters, and provides the predicability of resistance switching time if the input current/voltage waveform is given. The functionality of our models has been validated in HSPICE. The models can be used in multilevel RRAM modeling as well as in artificial neural network simulations.

Keywords: memristor, multilevel cell, SPICE model

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1. Introduction

Since Moore's law will cease to exist in the near future as CMOS technologies are approaching their scaling limits, many novel materials and architectures with distinct memory mechanisms have recently been proposed by the memory industry for the purpose of continuing Moore's law, such as phase-change memory (PCRAM), ferroelectric memory (FeRAM), magnetic memory (MRAM), molecular memory, and carbon nanotube-based memory.[1]

More recently, Williams *et al.* from HP[2] have materialized the memristor, which was postulated by Chua as the fourth basic element of electrical circuits in 1971 and had remained its theoretical existence henceforth.[3] The memristor has demonstrated the non-volatile resistance switching property. Its improvable high endurance, long retention time, high off/on resistance ratios, and fast programming speeds[4,5] distinguish itself as a rather promising candidate for building future resistive random access memory (RRAM).[6]

Another great advantage of the memristor is its potential to store multiple bits of information as different resistance levels,[3,7] which is known as the multilevel cell (MCL) technology.[8] The MCL functionality is a convenient yet crucial way to increase the memory capacity, and thus enhances the cost per GByte competitiveness of the technology. For example, the commercial available MLC NAND memories[8] and PCRAM memories[9] can store up to four states per cell.

According to Chua, the memristor with the continuative flux–charge relation has the potential to keep as many resistance stages as the periphery circuit can detect. However, in the real case, it is difficult to control the memristor to reach an anticipated resistance level due to the nonlinear flux–charge relationship and the vague understanding of the memristance (to avoid clutter, throughout the paper, we will use memristance and resistance interchangeably) change mechanism. Kim *et al.* proposed a reference resis-

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tance array and a feedback loop to achieve the accurate memristance programming;[10] Merkel *et al.* proposed a multilevel memristance rating metric and the corresponding memory architecture.[11] Both methods handle the multilevel programming problem by imposing the external CMOS circuits, which incur large periphery CMOS circuits.

Actually, there exist a kind of memristors with instinct multilevel resistance features, the resistance of which switches abruptly rather than continuously between neighboring resistance levels. Many memristors with the metal/oxide/metal structure have been found to exhibit bipolar multilevel resistance switching characteristics. For example, Yang *et al.* developed a Cu/TaO_x/Pt structured memristor with three nonvolatile resistance states;[12] Wang *et al.* reported a multilevel memristor in a Ti/Cu_xO/Pt structure;[13] Chang *et al.* investigated the multilevel resistance switching characteristics in a thin FeO_x film;[14] Wu *et al.* demonstrated a low-power and highly reliable multilevel operation in a ZrO_2 RRAM.[15] Moreover, Lu *et al.* even developed a memristor with ten resistance levels.[16]

As the multilevel memristor attracts growing attention, a practical circuit multilevel memristor model is greatly demanded for studying more complicated memory structures and applications, since physical memristor devices are still limited. However, most existing memristor models are built upon specific materials and switching mechanisms with binary ($R_{\rm on}/R_{\rm off}$) and continuous resistance switching.[17–23] Many model researches still focus on the improvement of the window function or the border constraint for the existing models,[24] or use mathematical models not suitable for circuit level simulation.[25,26] The models in Refs. [27] and [28] are based on the charge–flux constitutive relationships but not designed for multilevel memristors. Although Rozenberg *et al.* presented a theoretical model for the nonvolatile memory with multilevel switching,[29] their model is just a phenomenological model obtained with numerical simulations, which cannot be applied in circuit simulations. The only simulation program with integrated circuits emphasis (SPICE) model, which claimed the possible use for modeling multilevel RRAM, is the one proposed by Lee *et al.*[30] However, their model is mainly intended for single-bit unipolar RRAM rather than for bipolar multilevel memristors; and moreover, it is just a phenomenological model built by voltage-controlled resistors.

In this paper, we present SPICE models for charge-controlled and flux-controlled bipolar multilevel memristors, which can be applied in circuit simulations. The memristance versus state map proposed by Chua[31,32] is adopted to build the models. Since the memristance versus state map abstracts the fundamental characteristics of the memristor, our models can be widely applied to all kinds of multilevel memristors, rather than limited to a specific memristor with particular material or physical mechanism. In the proposed models, the memristance switches abruptly rather than continuously between neighboring resistance levels, which can be easily set as model parameters abstracted from the V–I curve of any actual memristor exhibting multilevel resistance switching phenomenon. Moreover, the resistance states in the models can be precisely modulated by the input current/voltage, and the resistance switching time between memristance levels can be predicted given the waveform of the stimulating voltage/current, which is hardly possible in the previous memristor models. We have simulated the SPICE models in HSPICE for demonstration of their functionalities. The proposed model can be used to model memristor-based RRAM MLCs as well as synaptic weights in artificial neural networks.[33] As far as we know, this is the first SPICE models proposed for charge-controlled and flux-controlled bipolar multilevel memristors.

The rest of the paper is organized as follows. In Section 2, we discuss the memristance versus state map of multilevel memristors, which is the theoretical basis for building the SPICE models. Section 3 presents the SPICE circuit structures for the charge- and the flux-controlled memristor models. Section 4 presents the SPICE simulation results of the models in HSPICE. In Section 5, we discuss the benefits and the shortcomings of the proposed models. Section 6 concludes this paper.

2. Memristance versus state map of multilevel memristors

Ideally, the memristor is a device that does not depend on any particular material or physical mechanism, whose characteristics are solely determined by its flux–charge constitutive relation or memristance versus state map.[32] However, in the real case, the state parameter of a practical memristor involves more than flux and charge. For example, the HP memristor

is a memristive system rather than a memristor.[2,7] For simplicity, we restrict our discussion to pure memristors, namely, charge-/flux-controlled time invariant memristors with charge/flux as the exclusive state variable. It is worth mentioning that in the proposed models, a current-/flux-controlled memristor is equivalent to a current-/voltage-controlled memristor, since the charge/flux is the time integral of the current/voltage. With the guidance of the memristance versus state map, we can tune the memristor's resistance continuously. Take the charge-controlled memristor shown in Fig. 1 for example, suppose the original resistance of the memristor is R_0 at state $q = q_0$, to change the resistance of the memristor to R_1 at state $q = q_1$, we only need to apply a current pulse $i(t)$ whose time integration is equal to the charge increment $\Delta q = (q_1 - q_0)$. The charge increment can be calculated from the memristance versus charge map.

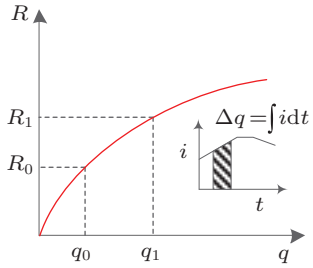


Fig. 1. (colour online) Memristance versus charge map of the memristor used to navigate its resistance tuning. The inset shows the time integration of the control current pulse.

Therefore, it is crucial to derive the memristance versus state map for the multilevel memristor. From Refs. [31] and [32], we know that the memristance versus state map for a binary charge-controlled memristor is

$$R_{\mathrm{M}}(q) = R_{\mathrm{on}} + 0.5(R_{\mathrm{off}} - R_{\mathrm{on}}) \times [\mathrm{sgn}(q + B) - \mathrm{sgn}(q - B)], \quad (1)$$

where R_{on} and R_{off} are the minimum and the maximum resistances of the memristor, respectively, B and $-B$ are the right and the left charge breakpoints for resistance switching, respectively, and sgn is the sign function. Equation (1) is shown in Fig. 2(a) by the solid line. It can be told from the figure that the resistance change of the memristor is only related to the amount of charge q passing through the memristor, regardless of the way the charge (the current) is applied to the memristor. In other words, no matter which current source is used, the memristance will change as long as the charge, i.e., integral of current, reaches the charge breakpoint in Fig. 2(a).

The dotted line in Fig. 2(a) shows the flux–charge constitutive relation of the memristor, which is a piecewise-linear curve consisting of 3 segments, with the slopes of the middle and the outer segments equaling to R_{off} and R_{on}, respectively. The equation for the φ–q constitutive relation is

$$\varphi_{\mathrm{M}}(q) = R_{\mathrm{off}} + 0.5(R_{\mathrm{on}} - R_{\mathrm{off}}) \times [|q + B| - |q - B|]. \quad (2)$$

In fact, equations (1) and (2) are equivalent, since equation (1) can be obtained by differentiating Eq. (2) with respect to q. Therefore, as long as one of the equations is known, the other can be deduced.

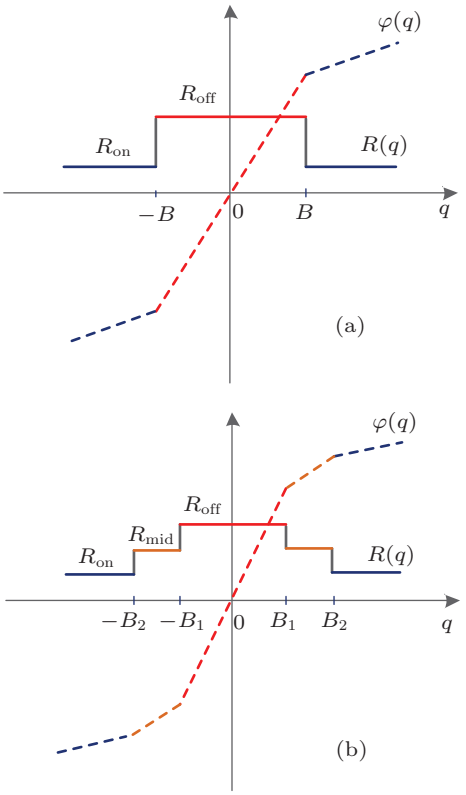


Fig. 2. (colour online) Memristance versus charge maps (solid lines) of (a) the binary[32,32] and (b) the ternary memritors, the dotted lines shows the corresponding piecewise-linear φ–q constitutive relationships.

To extend the binary model to the multilevel model, the memristance versus charge map should incorporate more resistance levels. As shown in Fig. 2(b), there are three resistance levels with resistances R_{on}, R_{mid}, and R_{off} separated by charge breaking points B_1 and B_2. The equation for the trinary memristance versus charge map is

$$R_{\mathrm{M}}(q) = R_{\mathrm{off}} + 0.5(R_{\mathrm{tmp}}(q) - R_{\mathrm{off}}) \times [\mathrm{sgn}(q + B_1) - \mathrm{sgn}(q - B_1)], \quad (3)$$

where

$$R_{\rm tmp}(q) = R_{\rm mid} + 0.5(R_{\rm on} - R_{\rm mid}) \times [\mathrm{sgn}(q + B_2) - \mathrm{sgn}(q - B_2)]. \quad (4)$$

To derive a general equation for the memristance versus charge map of multilevel memristors, we abstract a general function from Eq. (1)

$$f(X, Y, Z, q) = Y + 0.5(X - Y) \times [\mathrm{sgn}(q + Z) - \mathrm{sgn}(q - Z)]. \quad (5)$$

Then the equation for the memristance versus charge map of binary memristors, namely, Eq. (1), can be rewritten as

$$R_{\rm M}(q) = f(R_{\rm on}, R_{\rm off}, B, q). \quad (6)$$

And that of ternary memristors, namely, Eqs. (2) and (3), can be rewritten as

$$R_{\rm M}(q) = f(f(R_{\rm on}, R_{\rm mid}, B_2, q), R_{\rm off}, B_1, q). \quad (7)$$

In the same way, we can derive the equation for the memristance versus charge map of n-level memristors. Generally, the equation can be written as

$$R_{\rm M}(q) = f(f(\cdots f(R_n, R_{n-1}, B_{n-1}, q), \ldots, R_2, B_2, q), R_1, B_1, q), \quad (8)$$

where $(R_{\rm off} =)\ R_1 > R_2 > \cdots > R_{n-1} > R_n\ (= R_{\rm on})$ are the memristances for the n levels, and $B_1 < B_2 < \cdots < B_{n-1}$ are the $n-1$ charge breaking points.

Similarly, the equation for the n-level memductance versus flux map can be derived as

$$G_{\rm M}(\varphi) = f(f(\cdots f(G_n, G_{n-1}, F_{n-1}, \varphi), \ldots, G_2, F_2, \varphi), G_1, F_1, \varphi), \quad (9)$$

where $(G_{\rm off} =)\ G_1 < G_2 < \cdots < G_{n-1} < G_n\ (= G_{\rm on})$ are the memductances for the n levels, and $F_1 < F_2 < \cdots < F_{n-1}$ are the $n-1$ flux breaking points.

2.1. SPICE models

Based on the analysis above, we use the SPICE circuit to build the behavior models for charge-controlled and flux-controlled memristors. The circuit structures in the SPICE models are shown in Fig. 3.

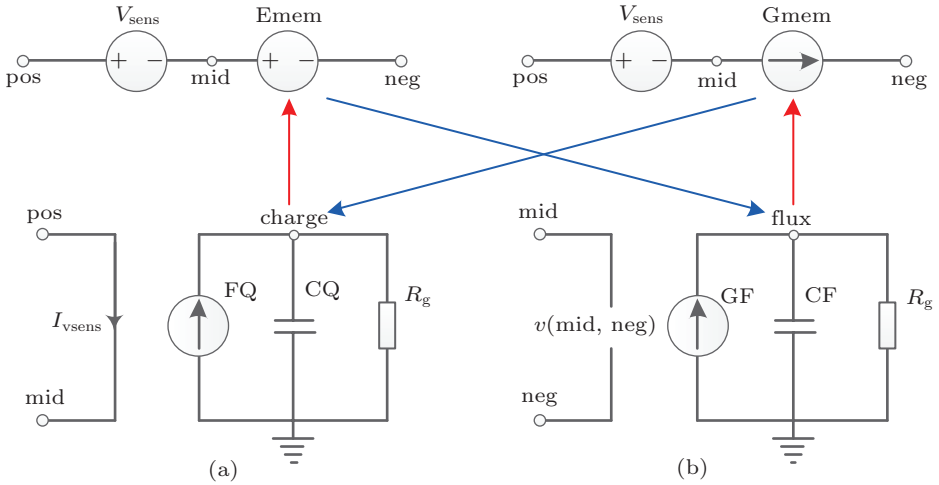


Fig. 3. (colour online) Structures of the SPICE models for (a) charge-controlled and (b) flux-controlled memristors.

2.1.1. Charge-controlled model

In the charge-controlled model, the memristance $R_{\rm M}(q)$ is dependent on input charge q. The model can be expressed by the following equations:

$$v_{\rm M} = R_{\rm M}(q) i_{\rm M}, \quad (10)$$

$$q = \int_0^t i_{\rm M} {\rm d}t, \quad (11)$$

where equation (9) is the resistive port equation, equation (10) is the state equation. It can be seen from the upper part of Fig. 3(a) that the port equation is realized by using a voltage-controlled voltage source Ememe and an independent voltage source $V_{\rm sen}$ serially connected between nodes pos and neg. Voltage source $V_{\rm sen}$ with output voltage 0 V is used to sense the applied current $i_{\rm M}$ ($i_{\rm sens}$) through the memristor, and voltage source Ememe is used to model the voltage drop $v_{\rm M}$ across the memristor, namely, $R_{\rm M}(q)$ multiplied by $i_{\rm M}$. The state equation is realized by feeding the measured current into the capacitor CQ via the

current controlled current source FQ, as shown in the low part of Fig. 3(a). The capacitor voltage $V_{\rm charge}$ is then equal to q, which is used by voltage source Emem to determine $R_{\rm M}(q)$, as shown by the red arrow in Fig. 3(a). A large resistor $R_{\rm g}$ is placed in parallel with the capacitor CQ to satisfy the SPICE convergence criteria. Note that the blue arrow in Fig. 3(a) points to the sub-circuit in the lower part of Fig. 3(b), which is used to calculate the flux through the memristor.

2.1.2. Flux-controlled model

In the flux-controlled model, the memristance $G_{\rm M}(\varphi)$ is dependent on the input flux φ. The model can be expressed by the following equations:

$$i_{\rm M} = G_{\rm M}(\varphi)v_{\rm M}, \tag{12}$$

$$\varphi = \int_0^t v_{\rm M}{\rm d}t, \tag{13}$$

where equation (11) is the conductive port equation, and equation (12) is the state equation. The conductive port equation for the flux-controlled model is realized by a voltage-controlled current source Gmem and an independent voltage source $V_{\rm sen}$ serially connected between nodes pos and neg, as shown in the upper part of Fig. 3(b). Voltage source $V_{\rm sen}$ with output voltage 0 V is also used to sense the current $i_{\rm M}$ through the memristor, and current source Gmem is used to model the current $i_{\rm M}$ through the memristor, namely, $G_{\rm M}(q)$ multiplied by $v_{\rm M}$. The state equation is realized by the lower part of Fig. 3(b). The applied voltage $v_{\rm M}$ ($v({\rm mid}, {\rm neg})$) is transferred into current by another voltage-controlled current source GF. The current is fed into capacitor CF. The capacitor voltage $V_{\rm flux}$ is then equal to the flux φ, which is used by current source Gmem to determine $G_{\rm M}(\varphi)$, as shown by the red arrow in Fig. 3(b). A large resistor $R_{\rm g}$ is also placed in parallel with capacitor CF to satisfy the SPICE convergence criteria. The charge here is calculated by using the sub-circuit in the lower part of Fig. 3(a) pointed by the blue arrow starting from Fig. 3(b).

3. Demonstrations of HSPICE analyses

To verify the aforementioned SPICE models, we do circuit analysis in HSPICE. The number of levels chosen for analysis is 4, and the memristance range from 100 Ω to 160 kΩ is chosen from the HP publication.[2] The memristance range is divided into 4 levels, 100 Ω, 541 Ω, 2947 Ω, and 16000 Ω, a geometric sequence rather than an arithmetic sequence for a better graph presentation. The memristance versus state maps for the four-level charge- and flux-controlled models respectively are

$$\begin{aligned} R_{\rm M}(q) = {} & f(R_{\rm on}, f(R_{\rm mid1}, f(R_{\rm mid2}, R_{\rm off}, \\ & B_3, q), B_2, q), B_1, q), \end{aligned} \tag{14}$$

$$\begin{aligned} G_{\rm M}(\varphi) = {} & f(G_{\rm on}, f(G_{\rm mid1}, f(G_{\rm mid2}, G_{\rm off}, \\ & F_3, \varphi), F_2, \varphi), F_1, \varphi). \end{aligned} \tag{15}$$

In the charge-controlled model, the breaking points are chosen to be 2×10^{-4} C, 4×10^{-4} C, and 6×10^{-4} C for B_1, B_2, and B_3, respectively; while in the flux-controlled model, the breaking points are chosen to be 2 W, 4 W, and 6 W for F_1, F_2, and F_3, respectively.

The simulation results for the charge-controlled and the flux-controlled models are shown in Figs. 4(a), 4(c) and 4(b), 4(d), respectively. Figure 4(a) shows the $R_{\rm M}(q)$ and the $G_{\rm M}(\varphi)$ curves. From the $R_{\rm M}(q)$ curve, we can see that there are four resistance levels, and the resistance of the memristor transits towards downstairs when the charge is building up, and vice versa. The $R_{\rm M}(q)$ curve coincides with the memristance versus charge map for the four-level memristor, which means that the proposed SPICE model is valid.

Notice that the resistance transition will occur as long as the charge passes any charge breaking point, no matter how the charge is accumulated. That is to say, the resistance transition only depends on the integration of the current, regardless of the waveform of the input current. So for a given regular input current, the precise resistance transition time can be calculated. For example, if the applied current is $i = A\sin(\omega t)$, where $A = 1$ mA and $\omega = 1$ s^{-1}, then $q = (1 - \cos t) \times 10^{-3}$ (C), the time needed for the three resistance switchings can be calculated to be 643.5 ms, 927.3 ms, and 1159.3 ms, which are in accordance with the simulation results. The predictability of the resistance switching time is a distinct feature of our model compared with the existing models whose resistance switching time is hardly predictable. The corresponding $\varphi(q)$ curve consists of four segments, and the slope of each segment equals to the resistance of the corresponding resistance level, which coincides with the theoretical analysis.

In Fig. 4(c), we show the pinched voltage–current (V–I) hysteresis loop, which is the fingerprint of the

memristor. To produce the hysteresis loop, a periodic input current should be applied to the model. From the V–I curve, we can also see that the resistance goes through four stages as the applied current sweeps to either end.

The simulation results for the flux-controlled model are similar to those for the charge-controlled model, as shown in Figs. 4(b) and 4(d). The state is presented by resistance rather than by conductance, since the memristance is more obvious for graphical perception. From the results, we can see that the flux-controlled SPICE model is also correct. To sum up, the HSPICE analysis results validate that the proposed multilevel charge-controlled and flux-controlled SPICE models function correctly.

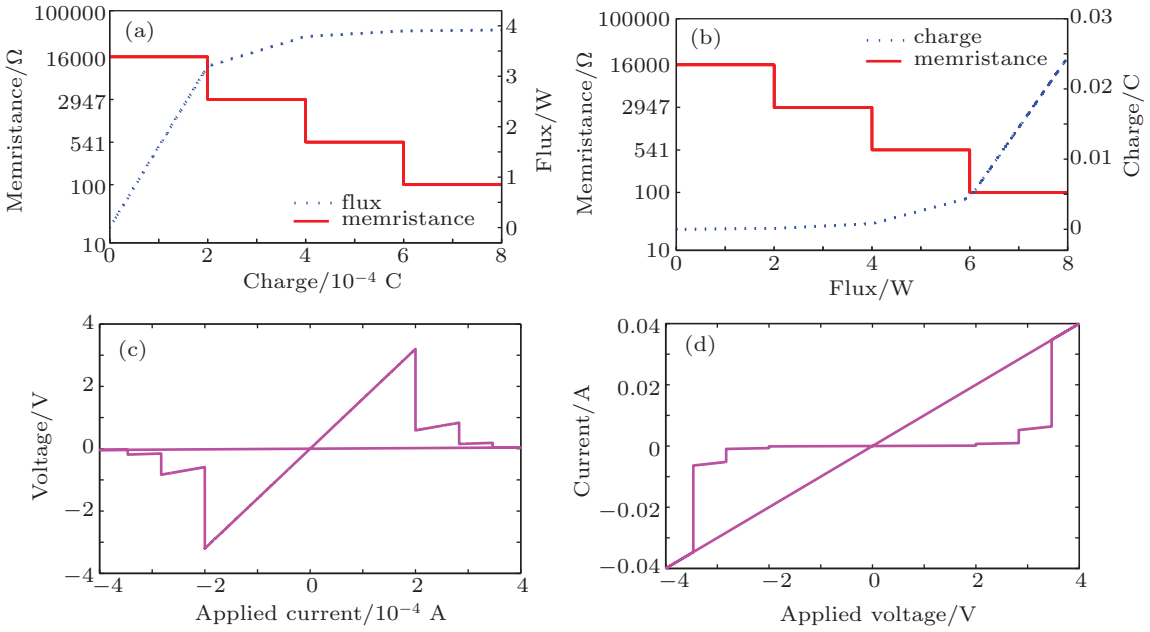


Fig. 4. (colour online) Simulation results for the charge-controlled ((a) $R_{\rm M}(q)$ and $\varphi(q)$, (c) V–I hysteresis loop) and the flux-controlled ((b) $R_{\rm M}(\varphi)$ and $q(\varphi)$, (d) I–V hysteresis loop) SPICE models.

4. Discussion

We believe that the multilevel resistance switching is a common characteristic of some kinds of memristors, rather than an isolated instance. Therefore, our models are proposed based on the memristance versus state map, which is the fundamental characteristic of memristors. This approach makes the models applicable to all multilevel memristors, rather than limited to any specific memristor. Moreover, the proposed models are not attainable through a simple extension or combination of existing models, which do not provide the ability to set multiple resistance levels and values as the parameters.

Although built regardless of materials and physical mechanisms, our models reinforce the conducting filament forming/rupturing theory, which assumes that the resistance switching of these materials is primarily due to the repeated formation and rupture of the nanoscale conducting filaments (CFs) at a localized position,[34,35] and the formation and rupture is caused by the external voltage/current bias. In our models, the accumulating/diminishing process of charge (flux) is equivalent to the formation/rupture process of CFs, which also accounts for the delayed switching phenomenon. In the proposed models, the charge/flux is accumulated linearly, corresponding to the linear formation of CFs. However, we can modify the charge/flux integrating equation in Eqs. (10) and (11) to take more factors of the CF formation mechanism into consideration.

In our models, however, the memristance will be pushed to either limits eventually if the applied positive current or voltage sustains long enough, regardless of how small the current or voltage is. This discrepancy with some voltage/current threshold memristor models is caused by the charge/flux thresholds (breakpoints in Fig. 2) adopted in our model, which actually explains the phenomenon that a large voltage bias always makes the switching event faster than a small

one. Another benefit of adopting charge or flux as the threshold is that the resistance switching time is calculable if we know the wave form of the applied current or voltage. The prerequisite of applying the models is obtaining the memristance versus state map of the memristor, which can be established theoretically for an ideal multilevel memristor or extracted from the I–V curve of a real memristor device. Moreover, our models enable the resistance levels to be grouped to form new resistance levels. For example, the four-level memristor with four charge/flux breaking points modeled in the previous section can be grouped into a two-level memristor if we set only one charge/flux breaking point. The models can be easily implemented in circuit simulation tools, such as SPICE and Verilog-A.

5. Conclusion

In this work, we have proposed the multilevel charge-controlled and flux-controlled memristor models based on the memristance versus state map of the memristor for the first time. Though developed regardless of materials and physical mechanisms, the proposed models can well support the conducting filament forming/rupturing theory, which tries to explain the resistance switching of memristors. Our model allows users to set the number of the resistance levels easily, and provides the predicability of resistance switching time for a given input current/voltage waveform. Additionally, when the model is used in simulating multilevel RRAM architecture, the number of memory levels presented by each memristor can be reconfigured by grouping resistance levels based on the needs of applications.

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