A novel sensitivity model for short nets*

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For modern processes at deep sub-micron technology node, yield design, especially the yield design at the stage of layout design is an important way to deal with the problem about manufacturability and yield. In order to reduce the yield loss caused by redundancy material defect, choice of nets to be optimized at first is an important step in the process of layout optimization. This paper provides a new sensitivity model for short net, which is net-based and reflects the size of the critical area between a single net and the nets around it. Since this model is based on a single net and includes the information of surrounding nets, the critical area between the single net and surrounding nets can be reduced at the same time. In this way, the efficiency of layout optimization becomes higher. According to experimental observations, this sensitivity model can be used to choose the position for optimization. Compared with the chip-area-based and basic-layout-based sensitivity models, our sensitivity model not only has higher efficiency, but also hold true for choosing the net to be optimized at first.

Keywords: redundancy material defect, layout optimization, critical area, short sensitivity

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1. Introduction

With the development of semiconductor industry, especially wide applications for nanometer nodes, design for manufacturability (DFM) has become more important than ever before in very large scale integration (VLSI) design.[1−4] The predicted yield of integrated circuit (IC) designed completely according to the standard rules cannot be achieved due to manufactural limitations including increasing densities of devices and interconnects due to sub-wavelength lithography, the yield loss resulting from fabrication defects,[5−9] the topography variations due to mechanically chemical polishing,[10−12] and so on.[13−16] As the main physical design step, routing contains the most accurate and richest manufacture information. Thus, layout optimization, which is an effective DFM method in routing step to take into account the lithography defects, arbitrary defects, and variation defects,[6,17−24] turns out to be a hot theme in academic and industrial research.

Considering the random defects, the practical method in yield design is the optimization in layout design step according to defects messages.[6,25−28] Experimental results have shown that the real defects have non-regular shapes in manufacture process[9,29−32] and have a certain spatial distribution.[20,33,34] In order to describe the yield issue, researchers introduced the definition of layout critical area and its extraction methods.[35−38] The layout critical area, as the bridge between design and manufacture, can improve the yield by reducing itself.

Changing the layout is the main method we adopt to reduce the layout critical area. How to choose and alter the layout positions has become a hot topic, which is vital to increase the accuracy of layout optimization. The layout sensitivity which reflects the failure probability provides abundant information to select the optimized positions. In Ref. [13], although the defect-diameter distribution is considered, a sensitivity model for short critical area in unit chip was still studied. The successive optimization method of critical area between networks is inefficient. Moreover, the layout sensitivity model based on layout message in Ref. [39] does not consider the real defects and network shapes. We have proposed in Ref. [41] an open NSO–network sensitivity model, which extracts the optimal positions, and found that single-network sen-

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sitivity model enable us to choose the optimal positions more intuitively and accurately. A new NSO sensitivity model for short net is further studied.

Nowadays, there are not enough indepth studies on net short sensitivity (NSS), which can reflect the short-circuit sensitivity of a single network and effectively optimize large-scale layouts when considering the real defects and network shapes. In this work, we propose a novel NSS method to achieve the layout optimization. The NSS shows high efficiency and accuracy in optimization process.

This paper is organized as follows. Section 2 provides two existing advanced sensitivity models for short nets, and analyzes the pros and cons. In Section 3, we briefly explain the interrelated concepts about layouts and defects,[38] and present our NSS method. Section 4 illustrates the NSS method and analyzes the performance, followed by conclusion in Section 5.

2. Existing sensitivity model for short nets

There are mainly two kinds of sensitivity models for short nets: one is based on the basic information of layouts, and the other is based on the value of critical area in a chip per unit. The features of the two models are analyzed in detail below.

2.1. Sensitivity model for short nets based on the basic information of layouts

A sensitivity model for short nets based on the basic information of layouts was proposed in Ref. [39], in which the defects approximate the circular ones, and the nets are similar to the rule rectangle. The maximal size of defects of m channels in the model is given as follows:

$$r = m(w+s) - w - \varepsilon, \tag{1}$$

where w is the width, s is the distance between nets, and ε is included to make sure that exact channels can contribute to an open defect. The sensitivity model for short nets is expressed by

$$S_{\text{short}} = 1 - \left[1 + \left(\frac{r-s}{w+s}\right) d\right] (1-d)^{(r-s)/(w+s)}, \tag{2}$$

where the channel density d determines the probability of the filled random access. The channel density d can be derived from the metal density D

$$D = d\frac{w}{w+s}. \tag{3}$$

Because we only consider the basic information of layouts, the sensitivity model for short nets, which reflects the short circuit failure probability, can play the role of assessing DFM due to the ease of calculation. However, there are some limitations of the model as follows:

1) The outline of the defects cannot be accurately reflected with the defects assumed to be circular ones.

2) It is necessary to obtain the distances in nets in the algorithm. For this purpose, the net is approximated to be the standard rectangular, but it is inaccurate in the description of irregular nets.

e) The channel density is required to be calculated first, which is always inaccurate because of the approximation of rectangular.

2.2. Sensitivity model for short nets based on the critical area value in a chip per unit

A sensitivity model for short nets based on the value of critical area (CA) in a chip per unit is given in Ref. [13], where the distribution of different sizes of particles is taken into account, and the probability of short circuit occurring within each couple of nets is obtained. The first step is to calculate the critical area A_{ij}^{s} between the visible nets in the model

$$A_{ij}^{\text{s}} = \begin{cases} 0, & 0 \le x \le s_{ij}, \\ l_{ij}(x - s_{ij}), & s_{ij} \le x \le 2s_{ij} + W_{\min}, \\ l_{ij}(s_{ij} + W_{\min}), & 2s_{ij} + W_{\min} \le x \le \infty, \end{cases} \tag{4}$$

where x is the size of defect particles, l_{ij} is the overlap length between nets W_i and W_j, s_{ij} is the area of the blank space, and $W_{\min}$ is the smaller area of the two nets. Thus, the probability of failure due to short defects caused by the random defect between nets W_i and W_j is obtained as follows:

$$\begin{aligned} p_{ij}^{\text{s}} &= \int_{x_{\min}}^{\infty} F(x) \frac{A_{ij}^{\text{s}}(x)}{A_{\text{chip}}} \mathrm{d}x \\ &= \frac{k l_{ij}}{2A_{\text{chip}}} \left(\frac{k l_{ij} + W_{\min}}{2s_{ij}^2} + W_{\min} s_{ij} \right), \end{aligned} \tag{5}$$

where A_{chip} is the total chip area.

The short critical area is obtained in the sensitivity model. In addition, the probability for short circuit occurring within each pair of nets is reflected with the distribution of defect size considered, which

can serve as the basis for optimizing layouts. However, it cannot reflect the spatial distribution of defect, because the model is based on the value of critical areas in a chip per unit, and it is an approximation that the distribution of nets on the layout is uniform. For a large number of net, the successive optimization for critical area between every pair of nets, the efficiency of optimization will become lower in VLSI.

To find the shortcomings of the above two sensitivity models, we propose a novel short-circuit sensitivity model based on a single net, which can reflect the probability of short circuits occurring between a single net and other surrounding nets, and take the real situations of defects and nets, as well as the size and spatial distribution of defects into account. The layout optimization's efficiency is improved.

3. Basic concept and NSS model

The outlines of real defects are irregular in the manufacturing process, which is more accurate than the equivalent circular models in the calculation of critical areas. Therefore we discuss the short-circuit sensitivity model based on the outlines of random defects.

3.1. Basic concept

In the NSS model, a layout consists of a two-dimensional matrix that can be represented by $\boldsymbol{L}_{N_1\times N_2}$, where $L[i,j]=0,1,\ (0\le i\le D_1, 0\le j\le N_2)$. The transform rule of routing on a layout is as follows: if the routing passes the grid point (i,j), then the value on this grid point in layout $L[i,j]=1$, otherwise, $L[i,j]=0$. The routing on layout is made of the sets $L[i,j]=1$. Similarly, the defects can be expressed by a two-dimensional matrix $\boldsymbol{D}_{D_1\times D_2}$, where $D[i,j]=0,1,\ (0\le i\le D_1, 0\le j\le D_2)$. The transform rule of defects in matrix is as follows: if the defects overlap with the grid position (i,j), then the value on this gird position $D[i,j]=1$, otherwise, $D[i,j]=0$, where the grid unit is the same as that of the layout. The real defects are composed of the sets $D[i,j]=1$. For a random defect $D\ (X_{\rm c},Y_{\rm c})$, its core is $(X_{\rm c},\ Y_{\rm c})$, and $X_{\rm c}=M_x/A_{\rm d}$, $Y_{\rm c}=M_y/A_{\rm d}$, where M_x and M_y are respectively the first-moment matrix of x and y axis, and $A_{\rm d}$ is the area of defects.

3.2. NSS model

Redundancy defect, resulting from dust particles in topography process, is referred to be the loss of topography layout and local line over erosion. It may cause the short fault. Figure 1(a) is the original layout, the red area in Fig. 1(b) is the defect in the manufacturing process, and figure 1(c) shows the short fault caused by the redundancy material defect existing on the layout.

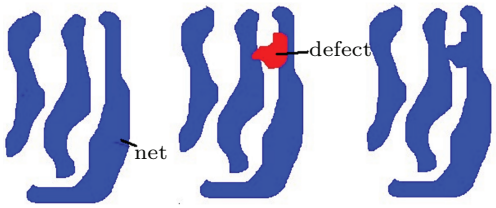


Fig. 1. Short fault caused by redundancy. (a) Original layout, (b) redundancy defect, and (c) short fault.

Definition 1 For an arbitrary shape net $N_1(i_1,j_1)$ with n_1 rows and m_1 columns $(i_1=1,2,...,n_1,\ j_1=1,2,...,m_1)$, and a net $N_2(i_2,j_2)$ with n_2 rows and m_2 columns of an arbitrary shape $(i_2=1,2,...,n_2,\ j_2=1,2,...,m_2)$, the short critical area is the region of defect centers connected in these two nets. As shown in Fig. 2, for given N_1, N_2, and $d(X_{\rm c},Y_{\rm c})$, the short critical area is $A_s(X_{\rm c},Y_{\rm c},N_1,N_2)$, which is caused by $d(X_{\rm c},Y_{\rm c})$ between nets N_1 and N_2.

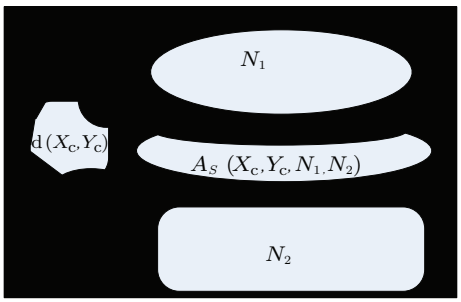


Fig. 2. Short critical area caused by redundancy defect.

Definition 2 For a special layout layer, let N^m be the set of nets in the layer, M be the number of nets, and N_i^m be the random net, where $1\le i\le M$ and $N_i^m\in N^m$. Then, the short critical area formed by the random defect $D(X_{\rm c},\ Y_{\rm c})$ in nets N_i^m and N_j^m is written by

$$A^{\rm c}(D(X_{\rm c},\ Y_{\rm c}),N_i^m,N_j^m)=\begin{cases}(A_{\rm sd}(D(X_{\rm c},\ Y_{\rm c}),N_i^m,N_j^m)-S_i-S_j)\cup N_i,\ S_i\neq 0, S-j\neq 0,\\ A_{\rm sd}(D(X_{\rm c},\ Y_{\rm c}),N_i^m,N_j^m), \qquad\qquad \text{otherwise},\end{cases} \tag{6}$$

where $A_{\rm sd}(D(X_{\rm c},\ Y_{\rm c}),N_i^m,N_j^m)$ is the intersection of sets of expanding nets N_i^m and N_j^m with the defect $D(X_{\rm c},\ Y_{\rm c})$ being the expansion element. The S_i is the intersection of $A_{\rm sd}(D(X_{\rm c},\ Y_{\rm c}),N_i^m,N_j^m)$ and N_i^m. The S_j is the intersection of $A_{\rm sd}(D(X_{\rm c},\ Y_{\rm c}),N_i^m,N_j^m)$ and N_j^m. The N_i is the area of N_i^m.

The short critical area C_i of net N_i^m resulting from the set of defect centers is expressed as

$$C_i=\sum_{j=1,j\neq i}^{M}A^{\rm c}(D(X_{\rm c},\ Y_{\rm c}),N_i^m,N_j^m). \tag{7}$$

Thus, the net sensitivity for short nets about a single net is defined as

$$\begin{aligned}N_i^{SS}&=\frac{c_i}{S(DN_i^m)}\\&=\frac{\sum\limits_{j=1,j\neq i}^{M}A^{\rm c}(D(X_{\rm c},\ Y_{\rm c}),N_i^m,N_j^m)}{S(DN_i^m)},\end{aligned} \tag{8}$$

where $S(DN_i^m)$ is the expansion area of N_i^m net in the mathematical morphology, which is associated with the size of defects and the area of nets.

In the calculation of short critical area, it is easily found that the short critical area must be a part of nets expanded in mathematical morphology. If the defect occurs on the expanded net, it will affect the net. However, it will lead to the short fault, depending on whether the defect is located within the short critical area or not. Hence, in order to reflect the short probability of a single net impacted by the defect, the above NSS expression is proposed. The NSS model meets the requirement that choosing the net with a high probability of failure to be firstly optimized can significantly improve yield, which can be used as the basis for the choice of candidate nets.

Let $N^{\rm S}$ be the set of expanded nets in the layer, S be the net number, $N_i^{\rm S}$ be any one expanded net ($1\leq i\leq S$), and $N_i^S\in N^S$. The $P^{\rm s}(X_{\rm c},\ Y_{\rm c})$ is the probability resulting from the defect $D(X_{\rm c},\ Y_{\rm c})$ on $N_i^{\rm S}$. Furthermore, the F is the set of defects on the layer. The $D(X_{\rm c},\ Y_{\rm c})$ is a defect with random shape, and $P(X_{\rm c},\ Y_{\rm c})$ is the probability that the defect $D(X_{\rm c},\ Y_{\rm c})$ occurs, and $D(X_{\rm c},\ Y_{\rm c})\in F$. Thus, the net sensitivity for short nets showing the size and spatial distribution of defects is defined as

$$N_i^{\rm p}=\sum_{D(X_{\rm c},Y_{\rm c})\in F}(N_i^{\rm SS}P(X_{\rm c},Y_{\rm c}))P^{\rm S}(X_{\rm c},Y_{\rm c}). \tag{9}$$

This formula reflects the size and spatial distribution of defects in the deep sub-micron technology node, which can serve as an important basis for selecting nets to be optimized in 90-nm, 65-nm, and even smaller technology nodes.

4. NSS application

The NSS model can be used in the highly active layout optimization. We take the local layout of mini universal serial bus (MUSB) for example. The features of the NSS model for layout optimization will be also given.

4.1. NSS optimization method

We input the local layout of MUSB and convert it into binary image. The binary image is shown in Fig. 3(a). The particle size of the defect is 14×8. Then, according to the mathematical morphology method, we extract the short critical area of the layout, which is shown in Fig. 3(b). In the image, net is blue and short critical area is green.

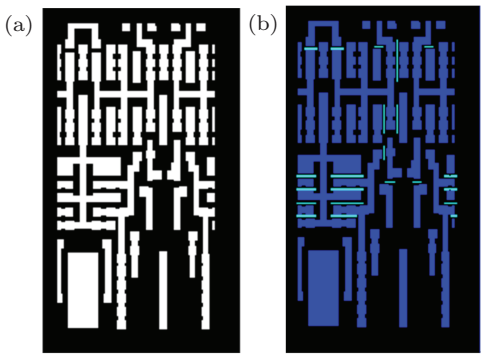


Fig. 3. (colour online) (a) Local layout of MUSB, and (b) its short critical area.

Using Eqs. (7) and (8), we obtain the NSS listed in Table 1. The first column in Table 1 is the net number, and the second is the short critical area of the single net. The NSS is listed in the third column. The NSS that is zero or too small is not listed. We can observe the NSS more clearly in Fig. 4.

Table 1. The NSS of nets.

Nets	C_i/μ^2	NSS
3	130.0	0.0232
5	1722.5	0.0867
9	130.0	0.0337
12	32.0	0.0017
21	39.1	0.0154
27	37.1	0.0143
29	38.0	0.0029
33	344.8	0.0307

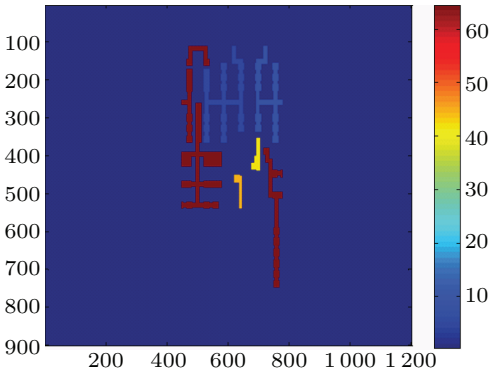


Fig. 4. (colour online) Distribution map of NSS.

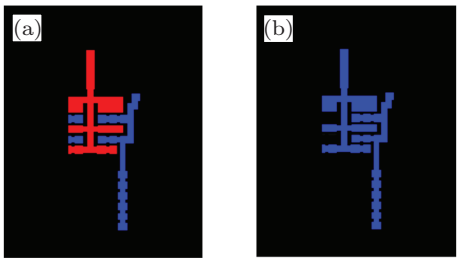


Fig. 5. Correlative nets of NSS optimization method and of existing optimization method. (a) Maximal NSS net and the correlative nets. (b) Nets with maximal short critical area.

There are some differences between NSS optimization method and existing optimization method. In Fig. 5(a), the net that has the maximum NSS and the nets that have short critical area with the maximum net are shown. In Fig. 5(b), there are two nets. The short critical area between the two nets is the largest according to Ref. [13]. From Fig. 5, it is easy to see that the first optimized net and the correlative nets can be chose at the same time when using NSS model to optimize layout. Therefore, the short critical areas between the first optimized net and the correlative nets can be reduced simultaneously. Compared with the existing optimization methods that just reduce the maximal critical area at the first optimization, the NSS optimization method is efficient.

Let us use the NSS as the the basis for selecting the optimization location. From Table 1, net 5 is the net with maximal NSS. Hence, net 5 is the first optimized net. Without changing the circuit performance and effecting the interconnection with the other layers, the wiring of net 5 is changed to reduce its short critical area. The layout after the first optimization is shown in Fig. 6(a). Let us use the same defect-size distribution to extract the short critical area of the optimized layout. Figure 6(b) is the short critical area after the first time optimization. The short critical area is significantly reduced.

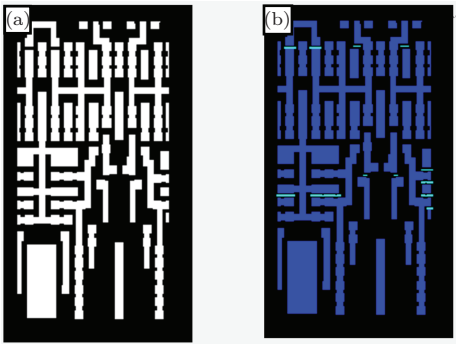


Fig. 6. (colour online) (a) Layout and (b) the short critical area after the first optimization.

In terms of Eqs. (7) and (8), we obtain the NSS after the first optimization (see Table 2) The short critical area of net 5 is 420.8 μ^2. It is reduced by 1301.7 μ^2. The NSS of net 5 is reduced to 0.0212. The net 9 has the maximal NSS, namely 0.0337. Repeat these steps until the layout cannot be optimized. It is showed that the extraction of NSS can help choose the optimization location.

Table 2. NSS after the first optimization.

Nets	C_i/μ^2	NSS
3	130.0	0.0232
5	420.8	0.0212
9	130.0	0.0337
12	32.0	0.0017
21	39.1	0.0154
27	37.1	0.0143
29	38.0	0.0029
33	344.8	0.0307

In the actual manufacturing process, distributions of different particlesize defects are different. Figure 7

shows the particlesize distribution of MUSB layout in the manufacturing process.

Taking into account the size distribution of defects on the map issue, in the calculation of short sensitivity, defects of different sizes and probabilities should be analyzed. In Fig. 7, the defect size is mainly in the range from 11×8 to 15×8. Therefore, the particle sizes of the defects were selected in this range to obtain NSS and then reflect the specific probability distribution. The results are shown in Table 3. All columns of Table 3 are the NSS values of different particle-size distributions except the last one. The last column is the value of NSS calculated based on Eq. (9) with the particlesize distribution considered, in which the spatial distribution $P^{\mathrm{s}}(X_{\mathrm{c}},\ Y_{\mathrm{c}}) = 1$. The sensitivity of net 5 is the highest, and the net 5 is selected as the first optimized net.

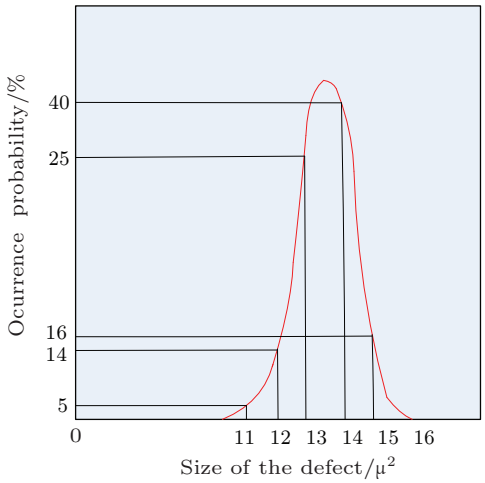


Fig. 7. (colour online) Defect's particlesize distribution of MUSB layout.

Table 3. NSS considering of the size distribution.

Nets	11×8	12×8	13×8	14×8	15×8	NSS
3	0.0096	0.0142	0.0188	0.0232	0.0276	0.0194
5	0.0263	0.0468	0.0670	0.0867	0.1057	0.0750
9	0.0144	0.0211	0.0275	0.0337	0.0396	0.0297
12	0.0000	0.0000	0.0008	0.0017	0.0025	0.0013
13	0.0000	0.0000	0.0000	0.0000	0.0019	0.0003
21	0.0000	0.0040	0.0080	0.0154	0.0226	0.0105
27	0.0000	0.0036	0.0070	0.0143	0.0214	0.0114
29	0.0000	0.0000	0.0014	0.0029	0.0042	0.0022
32	0.0000	0.0000	0.0000	0.0000	0.0105	0.0017
33	0.0084	0.0155	0.0231	0.0307	0.0382	0.0278

In order to test the feasibility of NSS optimization method, we use the optimization method to analyze a set of layouts. The results are shown in Table 4. The functions of NSS in different layouts have been realized, which fully validates that the NSS method can select the layout optimization location.

Table 4. Results of NSS for some layouts.

Layout	Size distribution/μ	Maximal net	Maximal NSS
Sample 1	12×12	7	0.0645
Sample 2	35×35	3	0.314
Sample 3	20×20	22	0.0409

4.2. Performance analysis

In order to analyze the performance of this optimization method more intuitively, the optimization method in this paper is compared with previous optimization methods used in Refs. [13] and [39]. Our optimization method based on NSS sensitivity has the following advantages: i) NSS can reflect the true shape of the defects and nets, and size and spatial distributions of the defects, which supports a wider and more accurate optimization; ii) sensitivity calculations take into account the probability that a single net becomes short with other nets all around it. The short critical areas between the first optimized net and the nets around it can be reduced simultaneously. The steps of layout optimization has been reduced and the efficiency of layout optimization has been improved.

In the optimization method, the calculation of NSS is related to the short critical areas of random shape defects, random shape layouts, and the calculation of net expansion areas. It is worth mentioning

that the rate of extracting NSS can be further improved. With the rapid development of the computer systems, divide and conquer strategy for parallel computing can be used to reduce the optimization time. In addition, with the permission of hardware investment, distributed computation can be used to further reduce the optimization time. Therefore, the optimization method proposed in this paper will offer a good application prospect.

5. Conclusion

In the process of the calculation of short critical area, it is easily found that the short critical area must be a part of nets expanded in mathematical morphology. However, if the defect occurs on the expanded net, it will affect the net and lead to the short fault, depending on whether the defect is located within the short critical area or not. Hence, in order to reflect the short probability of a single net impacted by the defect, the NSS expression is proposed. The NSS model meets the requirement that choosing the net with a high probability of failure to be firstly optimized can significantly improve yield, which can be used as the basis for the choice of nets to be optimized.

The next study will be devoted to the practical application of the model in VLSI, parallel implementation of the algorithm, automatical selection of nets, and impact on the circuit with re-wiring nets.

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