Microwave damage susceptibility trend of bipolar transistor as a function of frequency*

Ma Zhen-Yang(马振洋)†, Chai Chang-Chun(柴常春), Ren Xing-Rong(任兴荣), Yang Yin-Tang(杨银堂), Chen Bin(陈 斌), Song Kun(宋 坤), and Zhao Ying-Bo(赵颖博)

School of Microelectronics, Xidian University, Key Lab of Ministry of Education for Wide Band-Gap Semiconductor Materials and Devices, Xi'an 710071, *China*

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We conduct a theoretical study of the damage susceptibility trend of a typical bipolar transistor induced by high-power microwave (HPM) as a function of frequency. The dependences of the burnout time and the damage power on the signal frequency are obtained. Studies of the internal damage process and the mechanism of the device are carried out from the variation analysis of the distribution of the electric field, current density, and temperature. The investigation shows that the burnout time linearly depends on the signal frequency. The current density and the electric field at the damage position decrease with increasing frequency. Meanwhile, the temperature elevation occurs in the area between the p–n junction and the n–n^+ interface due to the increase of the electric field. Adopting the data analysis software, the relationship between the damage power and the frequency is obtained. Moreover, the thickness of the substrate has a significant effect on the burnout time.

Keywords: bipolar transistor, high-power microwave, frequency

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1. Introduction

Currently, one of the greatest concerns is the effect of electromagnetic interference on electronic systems due to high-power microwaves (HPMs).[1−8] Such HPMs introduce noise or signals into electronic systems, and could cause a temporary system malfunction, a component degradation, and even a permanent physical damage at high levels of irradiation. The microwave susceptibility of an electronic system has been widely investigated. The HPM injection experiments with a series of electronic components such as transistor–transistor logic, CMOS digital circuits, and analog device have shown that the susceptibility level decreases rapidly with increasing frequency.[9] The susceptibility level for several personal computers (PCs) with different specifications has been assessed.[10] The relationship between the severe upset threshold and the frequency was found to fit the same overall trend, and a linear trend indicated that the peak field strength make the PC upset increase rapidly with the frequency. An experimental study of the effects of the HPMs from 800 MHz to 4 GHz on CMOS inverters also indicate that the electromagnetic susceptibility decreases significantly with the radio frequency due to several circuit capacity bypass function.[11] All the experimental investigations indicate that the study of microwave susceptibility trend as a function of frequency is a profound task. However, few theoretical studies have been made on the HPM susceptibility trend. Specifically, there is a particular lack of device failure levels, while studies on the device level effects are required in order to better understand these electronic systems and the interference mechanism.

In a previous paper we established a two-dimensional (2D) electro-thermal model of a typical bipolar transistor and studied the damage effect and the mechanism of the device caused by microwaves, which was validated by comparing with relevant experimental data.[12] Nevertheless, only single-frequency signals at 1 GHz were studied, which cannot reflect the frequency susceptibility trend of the device. In the present paper, the dependences of the burnout time and the damage power on the signal frequency are explored numerically. The internal damage mechanism is studied through the variation analysis of the distributions of electric field, current density, and

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†Corresponding author. E-mail: zyma@mail.xidian.edu.cn

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temperature. Meanwhile, the influence of the device substrate on the damage process is studied.

2. Structure and model

2.1. Device structure

The schematic diagram of the analyzed silicon n^+–p–n–n^+ epitaxial planar transistor is given in Fig. 1(a), and only half of the transistor is analyzed due to the geometrical symmetry. The transistor in our simulation consists of a 200-μm-thick n^+-type collector substrate and a 2-μm-thick n-type epitaxial layer. Here, B, C, and E stand for its base, collector, and emitter contacts, respectively. The N^+ denotes the heavily doped region of the n-type silicon, N and P the n- and p-type silicon regions. The doping profile of the transistor is given in Fig. 1(b). The thermal electrode is specified at the bottom of the transistor where the lattice temperature remains at 300 K. The upper surface and the sidewall boundaries are thermally insulated from the environment.

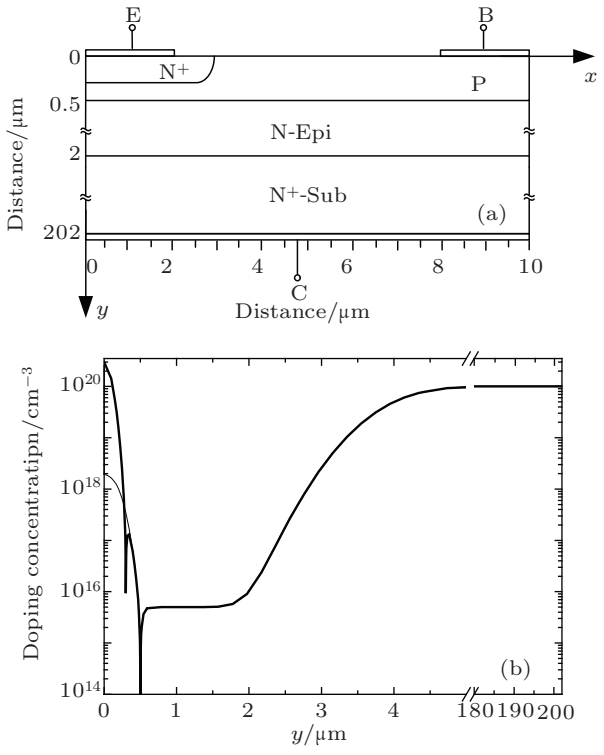


Fig. 1. (a) Device structure of an n^+–p–n–n^+ transistor; (b) doping profile of the device.

2.2. Signal source model

The HPM energy is coupled with the internal components of the electronic system through two generic paths, i.e., front-door coupling and back-door coupling, which could induce high-amplitude current pluses and high-amplitude voltage pluses on the device pinouts. In order to calculate the induced electromotive force on the device pinouts, an ideal situation is selected, assuming that the HPM is sinusoidal uniform plane wave (SUPW). The electric-field intensity is written as

$$E_{\rm in} = E_0 \sin(2\pi f t + \varphi_0), \tag{1}$$

where E_0 is the maximum of the electric field, f the frequency, and φ_0 the initial phase.

Using Maxwell's equations, we have

$$\boldsymbol{B} = \mu \boldsymbol{H}, \tag{2}$$

$$E_{\rm T} = \eta H_{\rm T}, \tag{3}$$

$$\Phi = \iint_s \boldsymbol{B} \cdot {\rm d}\boldsymbol{s}, \tag{4}$$

$$\varepsilon = -\frac{{\rm d}\Phi}{{\rm d}t} = -\iint_s \frac{{\rm d}\boldsymbol{B}}{{\rm d}t} \cdot {\rm d}\boldsymbol{s}, \tag{5}$$

where $\boldsymbol{B}$ and $\boldsymbol{H}$ are the electric field vector and magnetic field vector, respectively, μ is the permeability, η is the wave impedance, Φ is the magnetic flux, s is the area of the surface, and ε is the induced electromotive force. The induced electromotive force can be derived by Eqs. (1)–(5) as

$$\varepsilon = -\frac{{\rm d}\Phi}{{\rm d}t} = -2\pi f \mu E_0 \frac{s}{\eta} \cos(2\pi f t + \varphi_0). \tag{6}$$

The above expression indicates that there is a remarkable similarity between the waveform of the induced electromotive force and that of the radiation signal except the signal phase. Therefore, we take a simplified signal model into consideration, and the sinusoidal voltage signals with an initial phase of 0 are adopted as the injected signals in our simulation.

3. Results and discussion

3.1. Variation of burnout time with frequency

The simulation circuit is illustrated in Fig. 2, where the transistor is in the active mode of operation. Using the 2D device simulator ISE-TCAD, we take the device lattice temperature reaching the melting point of silicon at 1688 K as the burnout criteria. The frequency range selected in our simulation is between 300 MHz and 10 GHz, which is of most interest for HPM effects.[7,8] The sinusoidal voltage signals with an amplitude of 40 V are injected directly to the collector terminal until the transistor burns out. The

dependence of the signal frequency on the burnout time is illustrated in Fig. 3. It indicates that the device burnout time increases with the signal frequency. The burnout time at the frequency of 10 GHz is almost two times longer than that at the frequency of 300 MHz.

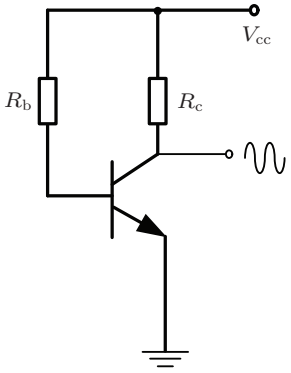


Fig. 2. Schematic diagram of the circuit.

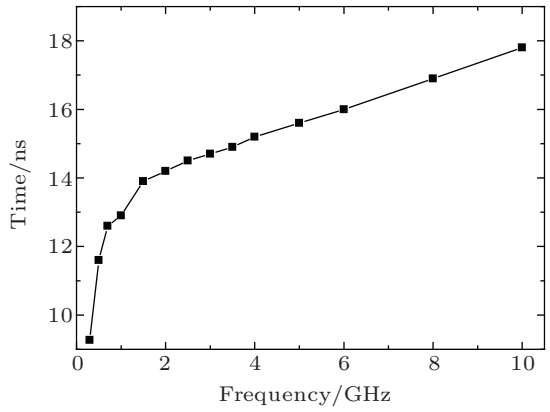


Fig. 3. Device burnout time versus frequency.

3.1.1. Variation of electric field with frequency

In the previous work, we have known that temperature elevation occurs mostly in the negative half period, and the base–emitter (B–E) junction is susceptible to damage when the signals are injected from the collector.[12] Therefore, we focus on the negative half period in the following sections. Figure 4 shows the variation of the electric field along the line $x = 2$ μm at the moment of the valley voltage ($U = -U_0$) for different signal frequencies. It is clear that with the increase of the signal frequency, the maximum value of the electric field at the B–E junction decreases. However, the electric field in the area between the p–n junction and the n–n^+ interface increases gradually. In the negative half period, when the injected absolute voltage is high enough, the emitter junction is reversely biased and the collector junction is forward biased. The potential drop mostly falls on the B–E junction, where the electric field is the highest. As we can see from Fig. 4, the distribution of the electric field fits the similar situation at the low signal frequency. However, when the signal frequency increases (see Fig. 4), another peak field occurs between the p–n junction and the n–n^+ interface, and the field at the B–E junction decreases.

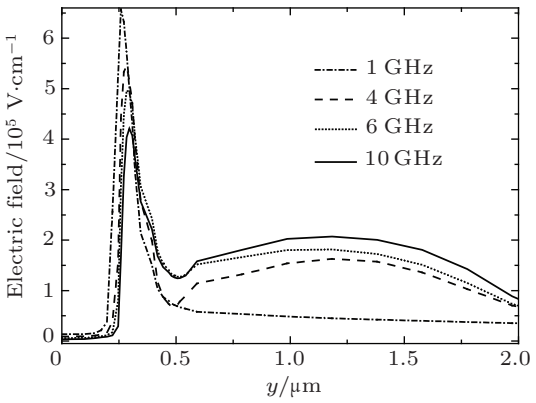


Fig. 4. Electric-field distribution of the device along the line $x = 2$ μm.

Figure 5 depicts the time evolution of the electric field (from 150 ps to 185 ps) at the frequency of 10 GHz. The study in Ref. [12] have shown that the phenomenon of base widening occurs in the positive half period, and the peak field shifts from the collector junction to the n–n^+ interface due to the high-amplitude collector current. Figure 5(a) shows the variation of the electric field at the initial time of the negative half period, which indicates that the peak of electric field at the n–n^+ interface still exists. Under the injection of microwaves, the electric field in the collector space charge region is influenced mainly by the collector current.[13] When the injected signal frequency is low, the space charges there have adequate time to flow to each electrode, and the peak field at the n–n^+ interface begins to decay when the injected voltage decreases. However, the time needed for the carriers to drift decreases with increasing frequency, and the electric field at the n–n^+ interface exists even in the negative half period. As depicted in Fig. 5(b), the electric field at the n–n^+ interface tends to drift toward the emitter region, and the electric-field strength decreases. Meanwhile, the electric-field peak strength at the B–E junction increases. At $t = 185$ ps, the electric field in the collector region essentially disappears (see Fig. 5(c)).

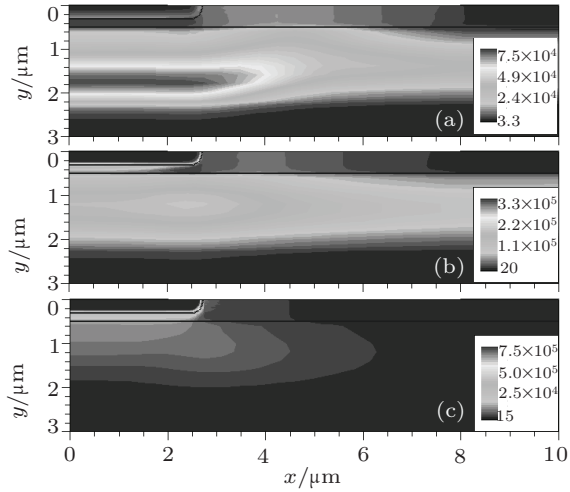


Fig. 5. Electric-field distribution of the device at (a) 150 ps, (b) 175 ps, and (c) 185 ps.

Figure 6 sketches the dependence of the potential drops across the B–E junction and the epitaxial layer on the signal frequency at the moment of the valley value in negative half period. It is seen that the potential drop across the epitaxial layer increases with the signal frequency. By contrast, the potential drop across the B–E junction decreases. Though the collector substrate offers very little resistance, the injected current is high enough so that the potential drop across the substrate cannot be negligible. The higher the collector current is, the higher the potential drop across the substrate, and the lower the potential drop across the epitaxial layer. However, the electric field in the space charge region increases with the signal frequency, and the increase of the potential drop across the n-type region will lead to the decrease of the potential drop across the B–E junction, which is also indicated in Fig. 4.

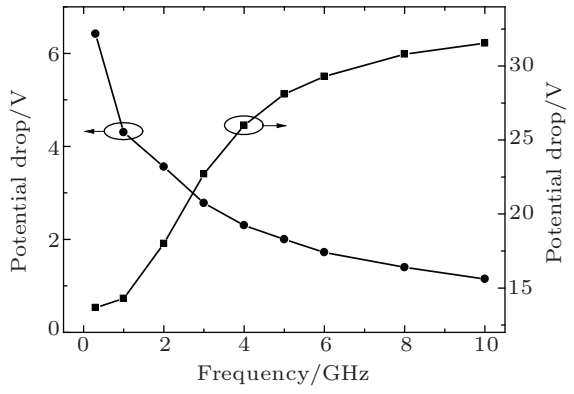


Fig. 6. Potential drops across the B–E junction (•) and the epitaxial layer (■).

3.1.2. Variation of current density with frequency

The rising time and the fall time of the injected voltage decrease gradually when the signal frequency varies from 300 MHz to 10 GHz. The displacement current, which is in direct proportion to the change rate of the injecting voltage, must increase simultaneously. As clearly showed in Fig. 7, the displacement current increases rapidly with the signal frequency, which is consistent with the discussion above. The displacement current at the frequency of 10 GHz is two hundred times larger than that at the frequency of 300 MHz. Figure 7 shows that the percentage of the displacement current in the total current increases gradually with the signal frequency. However, the percentage is very low, only 0.015 at the frequency of 10 GHz, which can be neglected as compared with the total current. Therefore, the displacement current contributes a little to the heat production, and the burnout time is rarely affected.

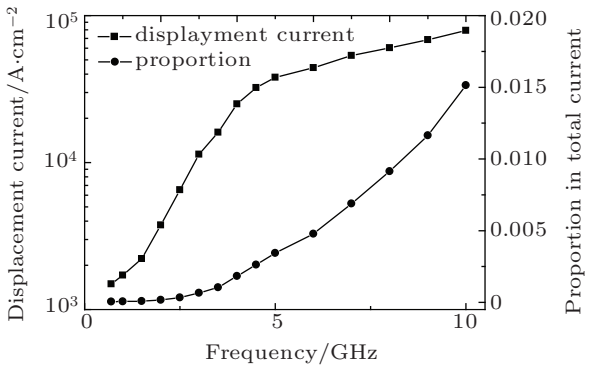


Fig. 7. Displacement current and its proportion in the total current as functions of frequency.

Figure 8 indicates that the maximum current density along the line $y = 0.1$ μm at the moment of the valley value in negative half period drops gradually with the signal frequency. At the frequency of 1 GHz, the current density at the damage position is about 1.58×10^8 A/cm^2, which is about five times larger than that at the frequency of 10 GHz.

During the injection of high-amplitude voltage signals, the presence of high-intensity electric field will have significant effect on the carrier drift velocity, and it is no longer proportional to the electric field strength. The physical model for describing this effect in our simulations is the Canali model.[14] The velocity saturation model is given by

$$v_{\rm sat} = v_{\rm sat,0}\left(\frac{T_0}{T}\right)^a,$$

where $v_{\mathrm{sat},0} = 1.07 \times 10^7$ (8.37×10^6) cm/s for the electrons (holes), and $a = 0.87$ (0.52) for the electrons (holes). In the positive half period, when the injected voltage is high enough, the avalanche breakdown occurs at the p–n junction and the n–n^+ interface. Limited by the velocity saturation and the flowing time of carriers, the avalanche carriers could not flow to the B–E junction adequately. The higher the signal frequency is, the shorter time the avalanche carriers take to flow. The similar case also exists in the negative half period. At the same time, the carrier saturation velocity will decrease with the increase of the internal accumulation temperature, which will aggravate this phenomenon. Furthermore, the potential drop across the B–E junction decreases with frequency (see Fig. 6), and the avalanche carriers reduce drastically. In short, the current density through the damage position becomes less with increasing frequency.

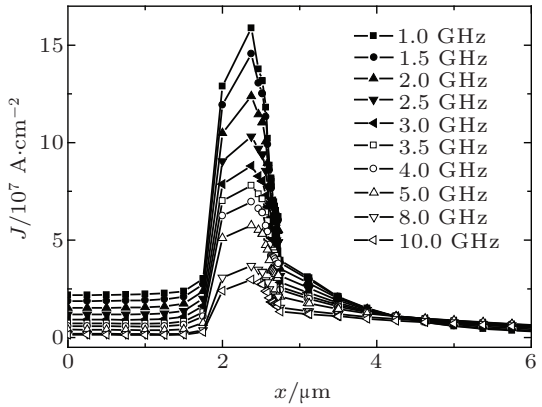


Fig. 8. Current density across the B–E junction at the moment of the valley value at different frequencies along the line $y = 0.1$ μm.

3.1.3. Variation of temperature with frequency

Figure 9 depicts the internal distribution of the temperature for different injected voltage frequencies at the burnout moment along the line $x = 2$ μm. It can be seen that the overall temperature between the p–n junction and the n–n^+ interface rises with increasing frequency. Owing to the fact that the base–emitter junction is the damage position, the increase of power dissipation outside the damage position in the damage process will prolong the burnout time. It is known that the joule heat is the expression of the electric field and the current density. The electric field in the area between the p–n junction and the n–n^+ interface increases with the frequency, and the temperature is mainly determined by the electric field due to the relatively low current density through the epitaxial layer.[12] At the same time, both of the current density and the electric field at the damage position decrease with the signal frequency, so the burnout time increases and the accumulation of the joule heat in the area between the p–n junction and n–n^+ interface increases with time.

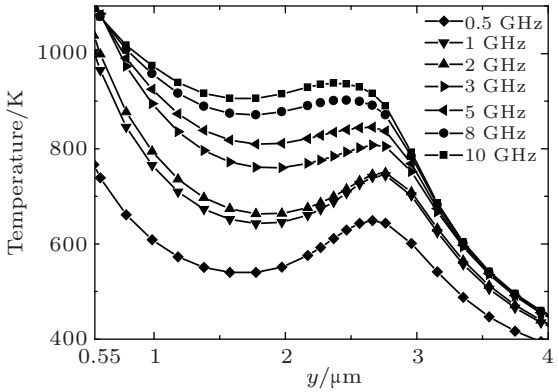


Fig. 9. Distribution of temperature for different signal frequencies along the line $x = 2$ μm.

3.2. Variation of average damage power with frequency

To determine the connection between the damage power threshold and the signal frequency for the bipolar transistor, the device is injected with a 20-ns-width single-voltage pulse by sweeping the frequency over 300 MHz to 10 GHz. Provided the injected voltage could not damage the device, we enlarge the amplitude of the voltage signal until the device is burned out. Figure 10 exhibits the dependence of the average damage power on the signal frequency. It indicates that the average damage power goes up gradually with the signal frequency. The damage power at the frequency of 10 GHz is about 1.6 W/μm, which is about two times larger than that at the frequency of 300 MHz. Adopting the curve fitting method to fit

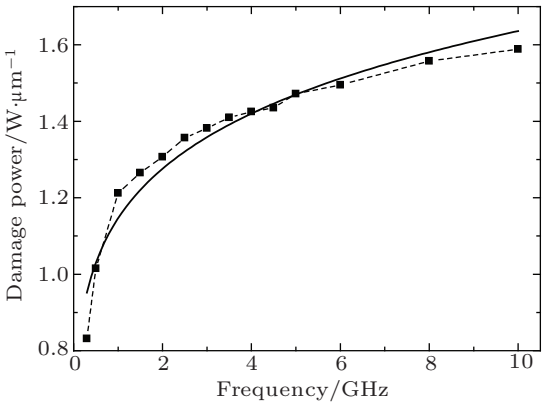


Fig. 10. Microwave average damage power for the transistor versus frequency.

the data points, we obtain the relationship between the damage power (P) and the signal frequency (f)

$$P = 1.15 f^{0.15},$$

where P is in W/μm, and f in GHz. The correlation coefficient R^2 is 0.95, showing high degree of fitting between the burnout power and the signal frequency.

3.3. Influence of the device substrate on the burnout time

The substrate of the device is heavily doped in order to dissipate the heat produced by the current. Due to the high current induced by the high-amplitude voltage, the potential drop across the substrate must not be ignored. The larger the resistance is, the higher the potential drop across the substrate is. Moreover, under the impact of the high-frequency signals, the carriers provided by the voltage source could not be mostly transferred to the damage position. With the increase of the signal frequency, the time the carriers take to move in every half period decreases gradually. In the present paper, we calculate the maximum distance $D_{\max}$ of the carriers as a function of frequency within a half period. Taking the electrons as an example, the maximum value of $v_{\rm sat}$ for electrons is about 1.07×10^7 cm/s, then we have

$$D_{\max} = \frac{v_{\rm sat}}{2f}.$$

When the signal frequency varies from 1 GHz to 10 GHz, the $D_{\max}$ changes from 53.6 μm to 5.36 μm. As we can see in Fig. 1, the thickness of the substrate is 200 μm. This will have a great effect on the damage process of the device. Figure 11 depicts the relationship between the burnout time and the signal frequency with diverse thicknesses of the substrate. It is found that the device with the thinner substrate is susceptible to damage. The burnout time of the device with a 100-μm substrate is only half of that with a 150-μm substrate. Therefore, the factor of the device structure should be taken into consideration to design circuit.

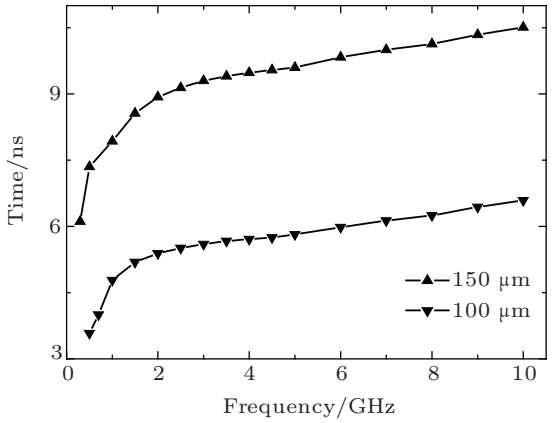


Fig. 11. Burnout time of the device with 100-μm-thick and 150-μm-thick substrates versus frequency.

4. Conclusion

We have established a model of a typical n^+–p–n–n^+ bipolar transistor by utilizing the ISE-TCAD simulator. The damage susceptibility trend as a function of frequency is studied. The findings indicate that the burnout time and the average damage power increase with frequency. By analyzing the time evolutions of the device internal distributions of electric field, current density, and temperature, a detailed investigation into the damage mechanism of the susceptibility trend is performed. It is showed that the distribution of the electric field at a lower frequency is different from that at a higher frequency. In the negative half period, the electric field in the area between p–n junction and n–n^+ interface is very weak at lower frequency, and enhances gradually with increasing frequency. Meanwhile, the potential drop and the current through B–E junction decrease with frequency, which results in the increase of the burnout time. Conclusively, the device with a thinner substrate is susceptible to damage.

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