Scaling properties of phase-change line memory*

Du Xiao-Feng(杜小锋)†, Song San-Nian(宋三年), Song Zhi-Tang(宋志棠), Liu Wei-Li(刘卫丽), Lü Shi-Long(吕士龙), Gu Yi-Feng(顾怡峰), Xue Wei-Jia(薛维佳), and Xi Wei(席 韡)

State Key Laboratory of Functional Materials for Informatics, Laboratory of Nanotechnology, Shanghai Institute of Micro-system and Information Technology, Chinese Academy of Sciences, Shanghai 200050, *China*

(Received 31 December 2011; revised manuscript received 18 April 2012)

Phase-change line memory cells with different line widths are fabricated using focused-ion-beam deposited C–Pt as a hard mask. The electrical performance of these memory devices was characterized. The current–voltage (I–V) and resistance–voltage (R–V) characteristics demonstrate that the power consumption decreases with the width of the phase-change line. A three-dimensional simulation is carried out to further study the scaling properties of phase-change line memory. The results show that the resistive amorphous (RESET) power consumption is proportional to the cross-sectional area of the phase-change line, but increases as the line length decreases.

Keywords: phase-change memory, line structure, scaling properties, three-dimensional simulation

PACS: 84.37.+q, 85.30.De, 85.40.Hp **DOI:** 10.1088/1674-1056/21/9/098401

1. Introduction

Phase-change memory (PCM) is a nonvolatile solid-state memory technology built around the large electrical contrast between highly resistive amorphous (RESET) and highly conductive crystalline (SET) states.[1,2] It has been considered as one of the most promising candidates for next-generation nonvolatile memory because of its low cost, low programing voltage, and excellent scalability to nanometer.[3−9] Phase-change line memory is highly suitable for embedded application because of its low process complexity and ease of integration.[10]

It is well known that nanomaterials have properties that are different from bulk materials of the same composition because surface and interface atoms play an increasing role. For example, it is typical for nanoparticles to have a lower melting temperature than bulk material. In order to ensure that PCM can work perfectly as the size of the cell is scaled down, both scaling properties of the phase-change materials and scaling properties of the PCM devices need to be considered. Scaling studies of phase-change materials have been done on thin films, nanowires, nanoparticles, and PCM devices.[11−15] Lee *et al.*[16] explored the effects of nanoscaling on the memory-storage capability of self-assembled $Ge_2Sb_2Te_5$ (GST) nanowires and found that such nanowires can satisfy many crucial attributes of universal non-volatile memory devices, such as scalability, low power consumption, data non-volatility, and ultrafast switching. However, these nanowires were grown by a metal-catalyst-mediated vapor–liquid–solid method and were single crystals, which are not compatible with complementary metal oxide semiconductor (CMOS) technology. Lankhorst *et al.*[17] introduced a phase-change line memory concept. This phase-change line memory is conceptually simple and its required programming power and current are low compared with conventional mushroom PCM structure. Moreover, Chen *et al.*[18] presented a bridge-structured PCM device consisting of a narrow line of ultra-thin phase-change material bridging two underlying electrodes and the device concept provided for simplified scaling to small cross-sectional area (60 nm^2) through ultra-thin (3 nm) films. Both of these lateral PCM concepts offer the potential for simplified scaling to smaller cross-sectional areas. In this letter, we developed a phase-change line memory fabrication method using focused-ion-beam (FIB) deposited C–Pt as a hard mask and electrical characterizations were performed. Three-dimensional (3D) simulation is carried out to further study power con-

*Project supported by the National Integrate Circuit Research Program of China (Grant No. 2009ZX02023-003), the National Key Basic Research Program of China (Grant Nos. 2010CB934300, 2011CBA00602, and 2011CB932800), the National Natural Science Foundation of China (Grant Nos. 60906003, 60906004, 61006087, and 61076121), and the Science and Technology Council of Shanghai of China (Grant No. 1052nm07000).

†Corresponding author. E-mail: duxiaofeng@mail.sim.ac.cn

© 2012 Chinese Physical Society and IOP Publishing Ltd

sumption with the scaling of phase-change line memory.

2. Experiment

The phase-change line memory device fabrication procedure is schematically illustrated in Fig. 1. At step (a), an 80-nm tungsten layer is deposited on a SiO_2/Si substrate with dc magnetic sputtering techniques. At step (b), electron beam lithography (EBL) and optical lithography are employed to form nanoscale electrode gaps and microscale electrodes for the electrical test. The width of the gap is about 200 nm. At step (c), a 100-nm-thick GST layer is deposited by sputtering a single alloy target at room temperature. At step (d), a nanoscale C–Pt line bridging the tungsten electrode gaps is deposited on the GST layer using the FIB. The C–Pt deposition process has been performed in a dual beam system (FEI Helios 600). The electron-beam-deposited C–Pt is carried out at the primary beam energy of 5 keV and beam current of 0.34 nA. Finally, at step (e), reactive ion etching (RIE) is applied to transfer the pattern onto the GST layer, adopting C–Pt pattern as a hard mask. The RIE is performed in the Oxford 80 plus RIE system, using a CF_4/Ar mixture gas with a ratio of 1/4, a background pressure of 80 mTorr, and a power of 200 W.

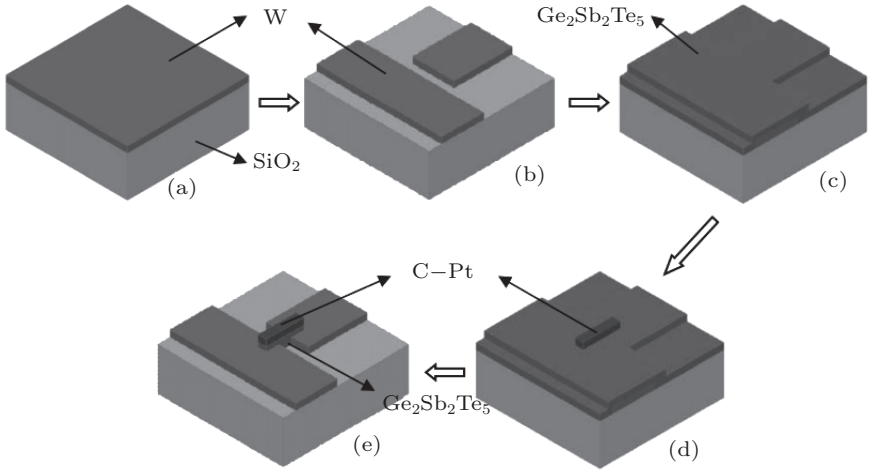


Fig. 1. Phase-change line memory cell fabrication process: (a) deposition of tungsten layer on SiO_2/Si substrate; (b) formation of nanoscale electrode gap by the EBL; (c) GST layer deposition; (d) C–Pt pattern deposition using FIB; (e) transformation of the C–Pt pattern onto GST layer by the RIE.

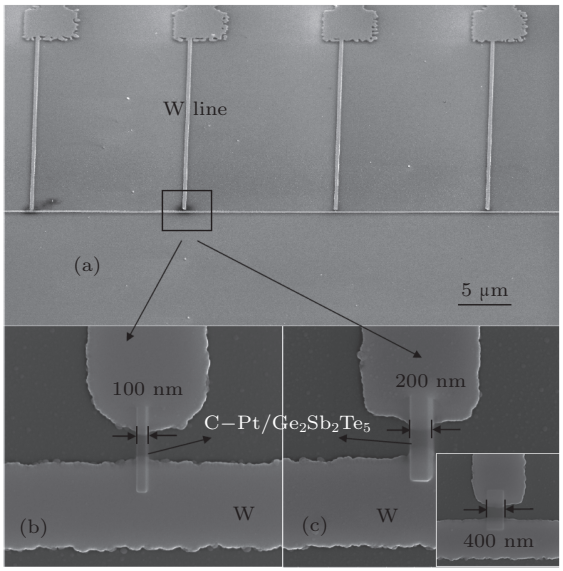


Fig. 2. SEM images of (a) phase-change line memory array, (b) 100-nm-wide cell, and (c) 200-nm-wide and 400-nm-wide (inset) cells.

In this way, the small electrode gap defines the line length (L), the width of the C–Pt pattern defines the line width (W), and the thickness of the phase-change material defines the line height (H). Phase-change line memory cells of different widths with a height of about 100 nm and a length of about 200 nm have been obtained, as shown in Fig. 2. Figure 2(b) shows highly magnified SEM pictures of 100-nm-wide phase-change line memory cell, and Fig. 2(c) shows 200-nm-wide and 400-nm-wide (inset) ones.

3. Results and discussion

3.1. Electrical characteristics

The electrical performance of memory devices with different widths was characterized. Figure 3 shows typical I–V curves (dc characteristics) of the

memory devices. A typical I–V scanning starts from a re-amorphization state. The voltage increases with current when the current is low, but a large snapback of voltage is observed when the applied current is higher than a threshold value, indicating that phase transition from the amorphous state to the crystalline state occurs. With further increase of current, the I–V curve exhibits a typical ohmic characteristic, which suggests that the cell is in a low-resistance state. Comparing the electrical characteristics of devices with different widths as shown in Fig. 3, we find that both the threshold current ($I_{\rm th}$) and voltage ($V_{\rm th}$) are reduced with the line width. For the 400-nm-wide device, the $I_{\rm th}$ almost equals 1.75 μA, and the $V_{\rm th}$ almost equals 1.9 V. For the 200-nm-wide device, the $I_{\rm th}$ almost equals 1.5 μA, and the $V_{\rm th}$ almost equals 1.27 V. For the 100-nm-wide device, the $I_{\rm th}$ almost equals 1 μA, and the $V_{\rm th}$ almost equals 0.79 V. The dc power consumptions are calculated to be 0.79 μW for 100-nm-wide device, 1.9 μW for 200-nm-wide device, and 3.3 μW for 400-nm-wide device. The dc power consumption for 100-nm-wide device is lower than that for 200-nm-wide and 400-nm-wide devices.

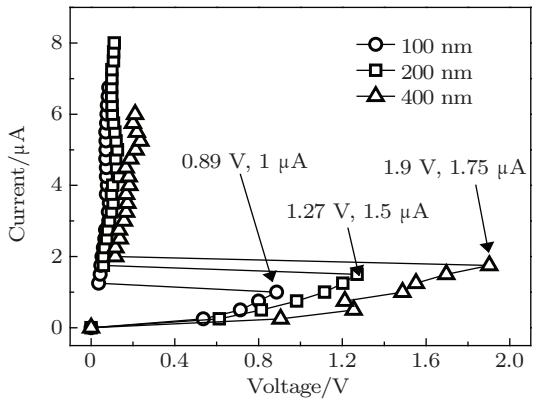


Fig. 3. I–V characteristics of phase-change line memory cells with different widths.

Figure 4 shows the pulsed resistance–voltage (R–V) characteristics (RESET and SET processes) of phase-change line devices with different widths. The R–V characteristics were measured by applying a sequence of voltage pulses of variable duration and magnitude generated by Agilent 4155B pulse generator, and the resistance of the memory cell was recorded at a test voltage of 0.1 V by employing Keithly 2600. As shown in Fig. 4, by applying a 1000-ns-wide voltage pulse, reversible phase change process has been observed, and the resistance of the RESET state is three orders higher than that of the SET state. For 100-nm-wide device, the set voltage ($V_{\rm SET}$) is 1.5 V and the reset voltage ($V_{\rm RESET}$) is 3.5 V. For 200-nm-wide device, the $V_{\rm SET}$ is 2.2 V and the $V_{\rm RESET}$ is 4 V. For 400-nm-wide device, the $V_{\rm SET}$ is 2.8 V and the $V_{\rm RESET}$ is 5 V. The required dissipated energy ($E_{\rm RESET}$) for the RESET operation was estimated using the expression $t_{\rm RESET}V^2_{\rm RESET}/R_{\rm SET}$.[19] The required energies$E_{\rm RESET}$ of 100-nm-wide, 200-nm-wide, and 400-nm-wide devices were calculated to be 7.7×10^{-10}, 1.33×10^{-9}, and 2.08×10^{-9} J, which confirmed the lower power consumption of phase-change line with smaller width.

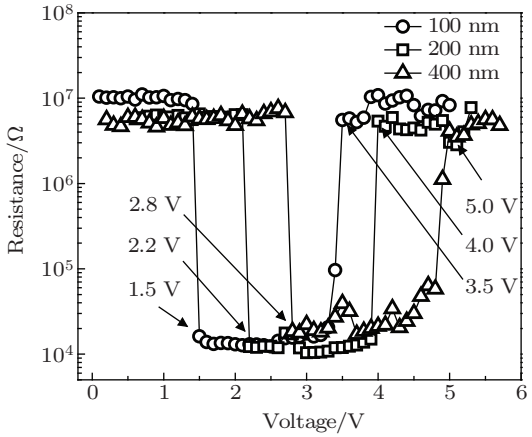


Fig. 4. Typical SET and RESET R–V characteristics of phase-change line memory cells with different widths.

3.2. 3D simulation

In order to gain an understanding of the scaling properties of phase-change line memory, 3D simulation using finite-element modeling was developed. We investigate the scaling perspective for three main parameters for phase-change line cells: line width (W), line height (H), and line length (L). The PCM cell uses Joule heat to change phase-change materials between SET and RESET states. The large power consumption (almost RESET power consumption) has been

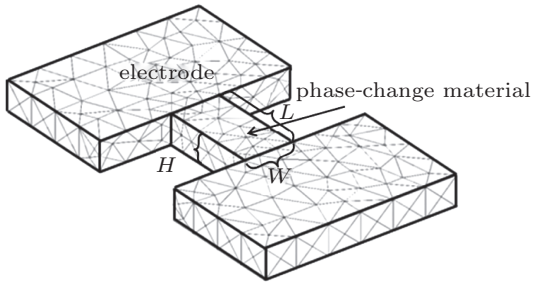


Fig. 5. Schematic of 3D simualtion model of phase-change line memory.

the major obstacle to downsize the cell structure. As sufficient electrical current pulse is applied to the SET-state phase-change line cell, the Joule heat brings the line partly into the molten state, and the line is subsequently cooled down by using a nanosecond pulse trailing edge. A RESET state of phase-change memory is obtained. The RESET current is the minimum electrical current to melt the phase-change line in this simulation. Figure 5 shows the 3D simulation model of phase-change line memory, and the thermal and electrical properties of materials are given in Table 1. The boundary temperature is taken as room temperature, and the interfaces between layers remain in perfect thermal and ohmic contacts.

Table 1. Physical properties of materials used in simulation.[20]

Material	Electrical conductivity/$\Omega^{-1} \cdot \mathrm{m}^{-1}$	Thermal conductivity/$\mathrm{W \cdot m^{-1} \cdot K^{-1}}$
C–GST (Crystalline)	2770	0.5
A–GST (Amorphous)	3	0.2
W	2.0×10^7	178
SiO_2	10^{-14}	1.4

Simulated RESET current of phase-change line structures as a function of line width ranging from 20 to 400 nm, for line height of 50, 100, and 200 nm is shown in Fig. 6. The simulation results show that the RESET current drops steadily as the line width gets narrower. Comparing cells with different heights, we can also find that the RESET current decreases with the height. In Fig. 7, the simulated and measured RESET energy consumptions are plotted as functions of line width, for $H = 100$ nm and $L = 200$ nm. An agreement between the simulation results and the measured data of our experiment is obtained. It is well known that the phase transition is based on the Joule heating effect. The inset in Fig. 7 exhibits the simulated temperature profile of the cross section of phase-change line ($W = 100$ nm, $H = 100$ nm). The isothermal contours with the GST melting temperature ($T = 893$ K) mark the molten region in the RESET operation. The molten region that overlaps the entire phase-change line cross section can be judged as RESET operation completion. For the same operation current pulse, the heat generation predominantly depends on the resistance of the phase change line. Thus, the Joule heat increases sharply and the phase-change material melts easily with decreasing cross-sectional area ($W \times H$). As a result, the RESET current is proportional to the cross-sectional area of the phase-change line.

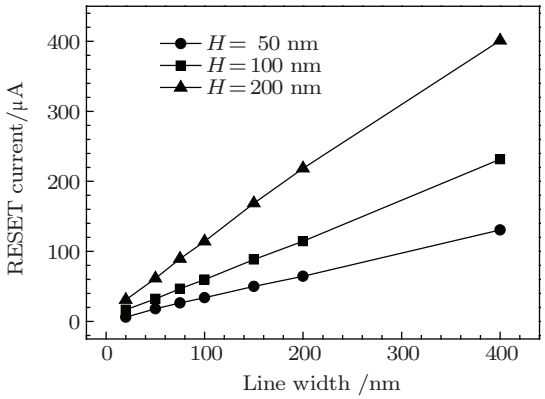


Fig. 6. Simulated RESET current of phase-change line structures as a function of line width ranging from 20 to 400 nm, for $H = 50$, 100, and 200 nm.

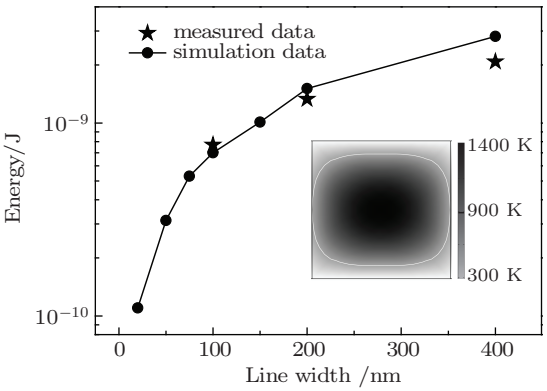


Fig. 7. Simulated and measured RESET energy consumptions as functions of line width, for $H = 100$ nm and $L = 200$ nm. The inset shows the simulated temperature profile of the cross section of phase-change line ($W = 100$ nm, $H = 100$ nm).

Figure 8 shows the simulated RESET current of phase-change line memory as a function of line length L, for $H = 100$ nm and $W = 100$ nm. We can find

the RESET current increases as the line length decreases. Figure 9 show the temperature profiles along the length direction of the phase-change line cells of $L = 50$, 100, and 200 nm. It is clear that the temperature drops faster for a shorter cell. This is because the thermal conductivity of GST is higher than tungsten (Table 1), and the molten volume of a longer GST line becomes increasingly thermally insulated from the tungsten electrode. The heat generated by the electrical current used for heating the phase-change material is less dissipated. As a result, the phase-change material can be molten easily, and a lower RESET current is obtained for a longer cell. Thus, the length of the line must be considered as the device scaling to obtain a less power consumption.

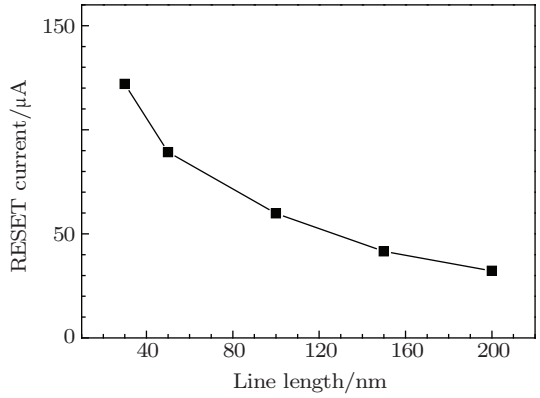


Fig. 8. Simulated RESET current of phase-change line memory as a function of line length L, for $H = 100$ nm and $W = 100$ nm.

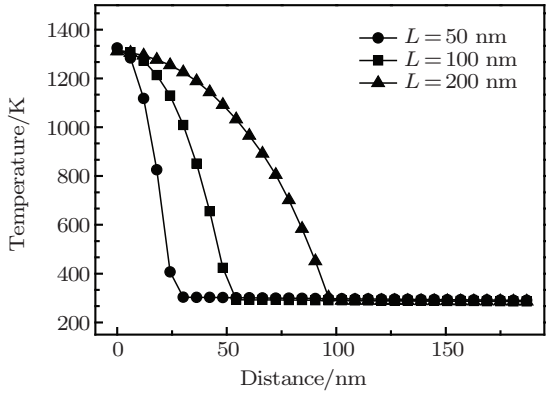


Fig. 9. Temperature profile along the length direction of the phase-change line with $L = 50$, 100, and 200 nm, $H = 100$ nm, and $W = 100$ nm.

4. Conclusions

In summary, GST-based phase-change line memory cells were fabricated using C–Pt as the hard mask. The detail of the method and the electrical characteristics of the cell are presented. Both experimental and simulation results show that the RESET power consumption scales with the cross-sectional area ($W \times H$). The reduced power consumption was believed to result from smaller programming volume of the phase change line. Conversely, the RESET current increases as the line length decreases because the phase-change material is increasingly thermally insulated from the tungsten electrodes.

References

[1] Ovshinsky S R 1968 *Phys. Rev. Lett.* **21** 1450
[2] Lacaita A L and Wouters D J 2008 *Phys. Stat. Sol.* A **205** 2281
[3] Bez R 2009 *IEDM Tech. Dig.* p. 1
[4] Lee J I, Park H, Cho S L, Park Y L, Bae B J, Park J H, Park J S, An H G, Bae J S, Ahn D H, Kim Y T, Horii H, Song S A, Shin J C, Park S O, Kim H S, Chung U I, Moon J T and Ryu B I 2007 *Tech. Dig. Symp. VLSI Technol.* p. 102
[5] Wuttig M and Yamada N 2007 *Nat. Mater.* **6** 824
[6] Pirovano A, Lacaita A L, Benvenuti A, Pellizzer F and Bez R 2004 *IEEE Trans. Electron Dev.* **51** 452
[7] Zhang T, Song Z T, Liu B, Liu W L, Feng S L and Chen B 2007 *Chin. Phys.* **16** 2475
[8] Liu B, Song Z T, Zhang T, Feng S L and Gan F X 2004 *Chin. Phys.* **13** 1167
[9] Liu B, Song Z T, Zhang T, Feng S L and Chen B 2004 *Chin. Phys.* **13** 1947
[10] Attenborough K, Hurkx G A M, Delhougne R, Perez J, Wang M T, Ong T C, Tran L, Roy D, Gravesteijn D J and van Duuren M J 2010 *IEDM Tech. Dig.* p 29.2.1
[11] Raoux S, Rettner C T, Jordan-Sweet J L, Kellock A J, Topuria T, Rice P M and Miller D C 2007 *J. Appl. Phys.* **102** 094305
[12] Milliron D J, Raoux S, Shelby R M and Jordan-Sweet J L 2007 *Nat. Mater.* **6** 352
[13] Satoh H, Sugawara K and Tanaka K 2006 *J. Appl. Phys.* **99** 024306
[14] Raoux S, Jordan-Sweet J L and Kellock A J 2008 *J. Appl. Phys.* **103** 114310
[15] Zhang T, Liu B, Song Z T, Liu W L, Feng S L and Chen B 2005 *Chin. Phys. Lett.* **22** 1803
[16] Lee S H, Jung Y and Agarwal R 2007 *Nat. Nanotech.* **2** 626
[17] Lankhorst M H R, Ketelaars B W S M M and Wolters R A M 2005 *Nat. Mater.* **4** 347
[18] Chen Y C, Rettner C T, Raoux S, Burr G W, Chen S H, Shelby R M, Salinga M, Risk W P, Happ T D, McClelland G M, Breitwisch M, Schrott A, Philipp J B, Lee M H, Cheek R, Nirschl T, Lamorey M, Chen C F, Joseph E, Zaidi S, Yee B, Lung H L, Bergmann R and Lam C 2006 *IEDM Tech. Dig.* p. 1
[19] Song S N, Song Z T, Liu B, Wu L C and Feng S L 2010 *Appl. Phys.* A **99** 767
[20] Gong Y F, Song Z T, Ling Y, Liu Y and Li Y J 2010 *Chin. Phys. Lett.* **27** 068501