Drain-induced barrier lowering effect for short channel dual material gate 4H silicon carbide metal–semiconductor field-effect transistor*

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Sub-threshold characteristics of the dual material gate 4H-SiC MESFET (DMGFET) are investigated and the analytical models to describe the drain-induced barrier lowering (DIBL) effect are derived by solving one- and two-dimensional Poisson's equations. Using these models, we calculate the bottom potential of the channel and the threshold voltage shift, which characterize the DIBL effect. The calculated results reveal that the DMG structure alleviates the deterioration of the threshold voltage and thus suppresses the DIBL effect due to the introduced step function which originates from the work function difference of the two gate materials when compared with the conventional single material gate metal–semiconductor field-effect transistor (SMGFET).

Keywords: silicon carbide, metal–semiconductor contact, dual material gate

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1. Introduction

SiC-based metal–semiconductor field-effect transistors (MESFETs) have become a promising technology for high-power microwave applications such as the transmitters for the commercial and military communications. In recent years, several improved SiC MESFET structures with excellent power characteristics have been reported.[1−6] In order to enhance the frequency performance, the gate length of the device should be reduced. Furthermore, with the development in the very/ultra large-scale integration (VLSI/ULSI) technology, the circuit density keeps increasing, and thus the device is required to decrease in size. Consequently, the short-channel effects should not be neglected. The drain-induced barrier lowering effect (DIBL) is the most common effect in the short-channel devices, which causes threshold-voltage-control problems and the current to be partially controlled by the drain potential rather than the gate potential. High-power and high-frequency 4H-SiC MESFETs are particularly susceptible to this effect due to the large applied drain voltage and their short-channel length. Now that the DIBL effect adversely affects the performance of the device, it should be minimized. It has been reported[7] that the application of the dual material gate in HFET structure introduces a step function in the channel potential distribution, giving rise to the suppression of the short channel effects.

In this paper, the sub-threshold characteristics of the dual material gate SiC MESFET (DMGFET) are studied and its analytical model of the two-dimensional (2D) potential distribution is established. From this model of potential distribution, the analytical expression for the threshold voltage shift is also obtained. Based on these models, the role of the dual material gate structure in suppressing the DIBL is analyzed.

2. Theoretical models

The cross-sectional view of the DMGFET is shown in Fig. l, where the x coordinate represents the direction along the channel and the y coordinate represents the direction perpendicular to the surface. The gate is composed of two materials with the lengths of

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L_1 and L_2, respectively. The thickness and doping concentration of the channel are a and $N_{\rm D}$, respectively. In the channel region, the 2D Poisson's equation can be written as

$$\frac{\partial^2 \Phi(x,y)}{\partial x^2} + \frac{\partial^2 \Phi(x,y)}{\partial y^2} = -\frac{qN_{\rm D}}{\varepsilon}, \quad 0 < y < a, \quad (1)$$

where ε is the permittivity, q is the electronic charge.

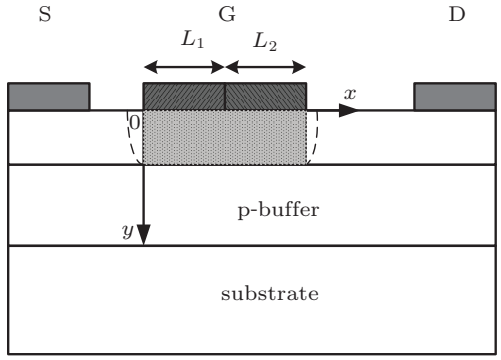


Fig. 1. Schematic diagram for the DMGFET structure.

Under the condition that the gate-source and gate-drain resistances are neglected, the boundary conditions are

$$\Phi_1(x,0) = V_{\rm GS} - V_{\rm bi1}, \quad (2a)$$
$$\Phi_2(x,0) = V_{\rm GS} - V_{\rm bi2}, \quad (2b)$$
$$\frac{\partial \Phi_1}{\partial y}(x,a) = \frac{\partial U_1}{\partial y}(a) = 0, \quad (2c)$$
$$\frac{\partial \Phi_2}{\partial y}(x,a) = \frac{\partial U_2}{\partial y}(a) = 0, \quad (2d)$$
$$\Phi_1(L_1,y) = \Phi_2(L_1,y), \quad (2e)$$
$$\frac{\partial \Phi_1}{\partial x}(L_1,y) = \frac{\partial \Phi_2}{\partial x}(L_1,y), \quad (2f)$$
$$\Phi_1(0,y) = \phi_{\rm SS}, \quad (2g)$$
$$\Phi_2(L,y) = \phi_{\rm SS} + V_{\rm DS}, \quad (2h)$$

where $V_{\rm bi1}$ and $V_{\rm bi2}$ are, respectively, the built-in potentials of the Schottky barriers formed by the metals and the channel layer, a is the channel thickness, $U(y)$ is the solution of one-dimensional (1D) Poisson's equation, $\phi_{\rm SS}$ is the built-in potential across the source/drain-to-substrate, L is the total length of the gate, and $V_{\rm GS}$ and $V_{\rm DS}$ are the applied gate bias and drain bias, respectively.

According to the approach adopted in Refs. [8] and [9], the potential $\Phi(x,y)$ in Eq. (1) can be decomposed into two functions

$$\Phi(x,y) = U(y) + \Psi(x,y), \quad (3)$$

where $U(y)$ and $\Psi(x,y)$ satisfy the following equations

$$\frac{\partial^2 U(y)}{\partial y^{\varepsilon}} = -\frac{qN_{\rm D}}{\varepsilon}, \quad 0 \le x \le L, \quad (4a)$$
$$\frac{\partial^2 \Psi(x,y)}{\partial x^2} + \frac{\partial^2 \Psi(x,y)}{\partial y^2} = 0. \quad (4b)$$

Based on the boundary conditions (2a)–(2h), the solutions of Eqs. (4a) and (4b) are obtained

$$U_{1(2)}(y) = -\frac{qN_{\rm D}}{2\varepsilon}y^2 + \frac{qN_{\rm D}a}{\varepsilon}y + V_{\rm GS} - V_{\rm bi1(2)}, \quad (5a)$$
$$\Psi_{1(2)}(x,y) = \sum_{k=0}^{\infty} \frac{n(y)}{m}\left[A_{1(2)k}\sinh\left(\frac{(2k+1)\pi(L-x)}{2a}\right) + B_{1(2)k}\sinh\left(\frac{(2k+1)\pi x}{2a}\right)\right], \quad (5b)$$

where

$$m = \sinh\left[\frac{(2k+1)\pi L}{2a}\right],$$
$$n(y) = \sin\left[\frac{(2k+1)\pi y}{2a}\right],$$
$$u = \cosh\left[\frac{(2n+1)\pi(L-L_1)}{2a}\right],$$
$$v = \cosh\left[\frac{(2n+1)\pi L_1}{2a}\right],$$
$$A_{1\rm K} = \frac{4(\phi_{\rm SS} - V_{\rm GS} + V_{\rm bi1})}{(2k+1)\pi} - \frac{16qN_{\rm D}a^2}{\varepsilon(2k+1)^3\pi^3},$$
$$B_{1\rm K} = \frac{4(\phi_{\rm SS} + V_{\rm DS} - V_{\rm GS} + V_{\rm bi2})}{(2k+1)\pi} - \frac{16qN_{\rm D}a^2}{\varepsilon(2k+1)^3\pi^3} - \frac{u}{n(y)}(V_{\rm bi2} - V_{\rm bi1}),$$
$$A_{2\rm K} = \frac{4(\phi_{\rm SS} - V_{\rm GS} + V_{\rm bi1})}{(2k+1)\pi} - \frac{16qN_{\rm D}a^2}{\varepsilon(2k+1)^3\pi^3} + \frac{v}{n(y)}(V_{\rm bi2} - V_{\rm bi1}),$$
$$B_{2\rm K} = \frac{4(\phi_{\rm SS} + V_{\rm DS} - V_{\rm GS} + V_{\rm bi2})}{(2k+1)\pi} - \frac{16qN_{\rm D}a^2}{\varepsilon(2k+1)^3\pi^3}.$$

At $y = 0$ level, once the position of the MSVEF ($x_{\rm min}$) is available, the minimum surface vertical electric field (MSVEF) can be obtained through the following equation:

$$-\frac{\partial}{\partial x}\left[\left(\frac{\partial \Phi(x,y)}{\partial y}\right)_{y=0}\right] = 0. \quad (6)$$

Thus, the MSVEF is derived to be

$$E_{ys\,\rm min} = E_{ys}(x_{\rm min}) = \frac{qN_{\rm D}a}{\varepsilon} + \Delta E_{ys\,\rm min}, \quad (7)$$

where

$$\Delta E_{ys\,\rm min} = \sum_{k=0}^{\infty}\left\{\left[\frac{2(\phi_{\rm SS} - V_{\rm GS} + V_{\rm bi1})}{a}\frac{B_{00}+1}{B_{00}}\right.\right.$$

$$+\frac{A_0A_{00}}{B_{00}}\Bigg]\exp\left[-\frac{(2n+1)\pi L}{4a}\right]$$
$$-\frac{8qN_{\rm D}a}{\varepsilon(2n+1)^2\pi^2}\frac{B_{00}+1}{B_{00}}$$
$$\times\exp\left[-\frac{(2n+1)\pi L}{4a}\right]\Bigg\},$$
$$A_0=\frac{2(\phi_{\rm SS}-V_{\rm GS}+V_{\rm bi1})}{a}-\frac{8qN_{\rm D}a}{\varepsilon\pi^2},$$
$$A_{00}=\frac{2(\phi_{\rm SS}-V_{\rm GS}+V_{\rm bi1})}{aA_0},$$
$$B_{00}=(1+A_{00})^{1/2}.$$

At the threshold of a long channel device, all the field lines from the gate terminate on the ionized donor charges in the completely depleted channel.[8] However, as the channel length decreases, a part of the vertical field lines on the surface terminates on source and drain instead and the remaining part terminates on the ionized donor charges in the channel. Consequently, the DIBL effect appears. The $\Delta E_{y\,\min}$ represents the extent of electric field induced by the DIBL effect. Therefore, when a gate bias which equals the long-channel threshold voltage ($V_{\rm TL}$) is applied to the short-channel device, the charge per unit area terminating at the point of the MSVEF is $qN_{\rm D}a-\varepsilon\Delta E_{y\,\min}$. To achieve the threshold condition (that is, complete depletion of the channel at the point of the MSVEF), an additional negative voltage should be applied to the gate to supply the excess charge which is equal to $\varepsilon\Delta E_{y\,\min}$. Hence, the short-channel threshold voltage is $V_{\rm TS}=V_{\rm TL}-\Delta V_{\rm T}$, where $\Delta V_{\rm T}=\Delta E_{y\,\min}a$ is the DIBL-induced short-channel threshold voltage shift. Summing the first infinite series and taking the first term of the second series, we obtain the drain-bias-induced threshold voltage shift $\Delta V_{\rm T}$

$$\Delta V_{\rm T}=\xi\frac{\exp\left[-\dfrac{\pi L}{4(a+a_0)}\right]}{1-\exp\left[-\dfrac{\pi L}{2(a+a_0)}\right]}+\zeta\exp\left[-\frac{\pi L}{4(a+a_0)}\right],\qquad(8)$$

where

$$\xi=2(\phi_{\rm SS}-V_{\rm GS}+V_{\rm bi1})\frac{B_{00}+1}{B_{00}}+\frac{aA_0A_{00}}{B_{00}},$$
$$\zeta=-\frac{8qN_{\rm D}a^2}{\varepsilon\pi_2}\frac{B_{00}+1}{B_{00}}.$$

3. Results and discussion

In our calculations, the length of the first gate material is equal to that of the second one. The doping concentration of the channel layer is 1.7×10^{17} cm^{-3}, and the gate bias is -3 V. The built-in potentials$V_{\rm bi1}$ and $V_{\rm bi2}$ are 1.8[10] and 0.8 V, respectively. The thickness a of the channel layer is 0.08 μm.

In condition that $y=a$ in the potential distribution function $\Phi_{1(2)}(x,y)$, the bottom potentials of the SMGFET and DMGFET are achieved, as shown in Fig. 2. To validate the accuracy of the analytical model derived in our work, the simulated results are also shown in Fig. 2 by using the ISE-TCAD simulator.[11] It is evident that the theoretical predictions of the analytical model are in excellent agreement with the simulated results, thus the validity of our analytical models is verified. There is a minimum for the bottom potential for both structures, which are

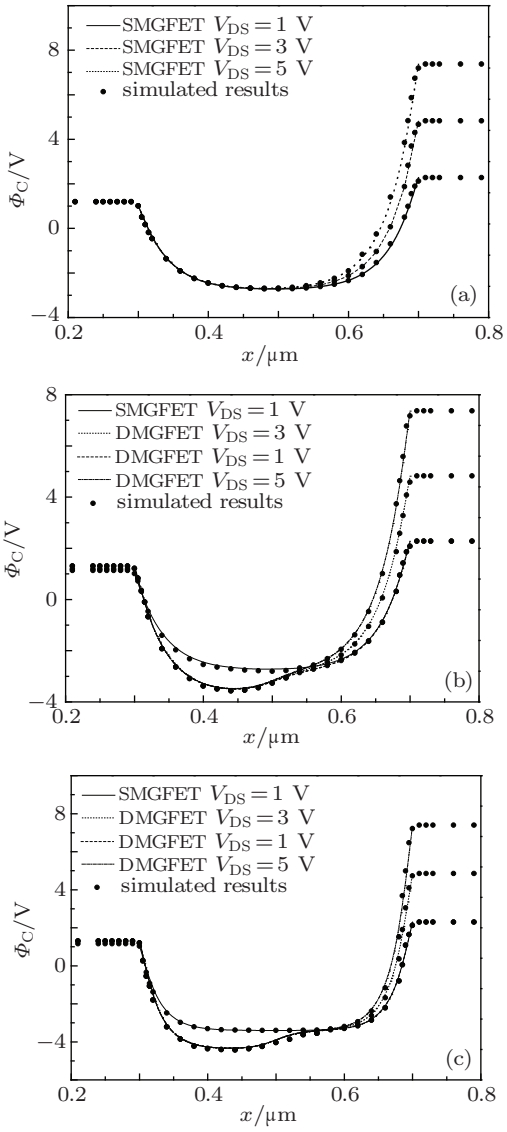


Fig. 2. Variation of the channel potential with respect to the lateral position at $V_{\rm DS}=1$, 3, and 5 (V) for (a) SMGFET, $a=0.08$ μm; (b) DMGFET, $a=0.08$ μm; (c) DMGFET, $a=0.05$ μm.

located at the point of $0.5L$ and $0.4L$ away from the left side of the gate for SMGFET and DMGFET, respectively. Thus, there exists a potential barrier near the source which comes from the potential difference between the source potential and channel potential minimum. This potential barrier is the equivalent of that in the p-n junction between the source and the channel in MOSFETs. It is just this potential barrier that limits the sub-threshold drain current in the channel. Note that in both structures, the minimum bottom potential is raised so that the potential barrier is lowered as the drain–source voltage increases due to the electric field induced by the drain–source voltage, commonly called the DIBL effect. However, it is shown in Figs. 2(b) and 2(c) that in the DMG structure a step function is introduced in the potential distribution due to the work function difference of the two gate materials and does not exist in the potential distribution of the SMGFET, which is similar to the results in Ref. [7]. This step function lowers the minimum of the bottom potential, and thus suppresses the DIBL effect, compared with the SMG structure.

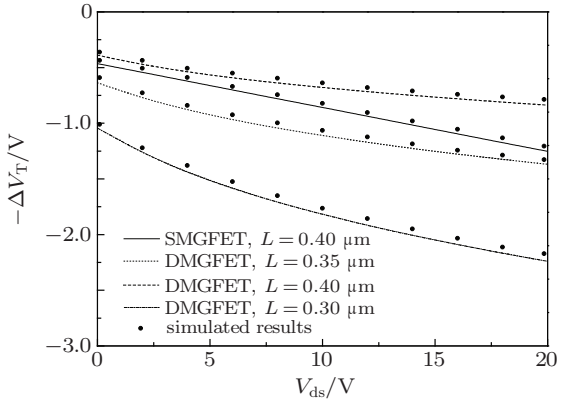


Fig. 3. Threshold voltage shift ($-\Delta V_T$) versus the drain bias for SMGFET and DMGFET at gate lengths of 0.4, 0.35, and 0.30 μm.

One of the negative effects caused by the DIBL is the threshold voltage shift, which is shown in Figs. 3 and 4. It can be seen in Fig. 4 that increasing the drain bias results in the threshold voltage degradation for a given gate length. The origin of this degradation is that as the drain bias increases, more field lines penetrate to the inside of the channel from the drain end. This degradation is more significant for shorter channel devices. It is indicated in Fig. 4 that when the gate length is above 1 μm, i.e., the device is regarded as a long channel device, the threshold voltage does not decrease and the device exhibits long-channel characteristics for both structures. However, when the gate length is less than 1 μm, the DIBL effect plays an increasing role and the threshold voltage decreases. Obviously, due to the introduced step function, the threshold voltage of the DMG structure is degraded more slowly than that of the SMG structure with the increase in the drain bias for a given gate length or the decrease in the gate length at the same drain bias, as shown in Figs. 3 and 4.

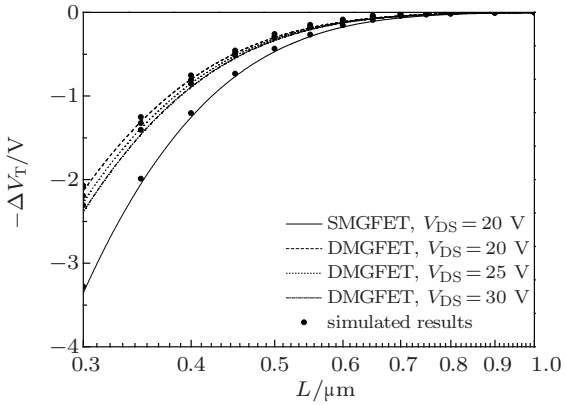


Fig. 4. Threshold voltage shift ($-\Delta V_T$) versus the channel length for SMGFET and DMGFET at V_{DS} = 20 V, 25 V, and 30 V.

4. Conclusion

In this paper, the DMGFET is studied and its analytical model of the 2D bottom potential distribution has been established by solving 2D Poisson's equation. Using this bottom potential model, we have also obtained the analytical expression for the threshold voltage shift. The calculated results reveal that the threshold voltage of the DMGFET is degraded more slowly than that of the SMGFET due to the introduced step function which comes from the work function difference between the two gate materials. Hence, the DIBL effect is significantly suppressed compared with that of the SMGFET. The obtained analytical models and the calculated results will provide valuable references to the improvement in the sub-threshold performance of the power microwave semiconductor devices.

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