Temperature and drain bias dependence of single event transient in 25-nm FinFET technology*

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(Received 28 November 2011; revised manuscript received 20 December 2011)

In this paper, we investigate the temperature and drain bias dependency of single event transient (SET) in 25-nm fin field-effect-transistor (FinFET) technology in a temperature range of 0–135 °C and supply voltage range of 0.4 V–1.6 V. Technology computer-aided design (TCAD) three-dimensional simulation results show that the drain current pulse duration increases from 0.6 ns to 3.4 ns when the temperature increases from 0 to 135 °C. The charge collected increases from 45.5 fC to 436.9 fC and the voltage pulse width decreases from 0.54 ns to 0.18 ns when supply voltage increases from 0.4 V to 1.6 V. Furthermore, simulation results and the mechanism of temperature and bias dependency are discussed.

Keywords: fin field-effect transistor, single event transient, temperature dependence, drain bias dependence

PACS: 94.05.Dd, 85.30.Tv, 02.60.Cb **DOI:** 10.1088/1674-1056/21/8/089401

1. Introduction

With the transistor density increasing and scaling down, scaling beyond a 32-nm node may not be possible using the conventional planar transistor architecture due to the uncontrollable short channel effect (SCE) and the excessive threshold voltage ($V_{\rm th}$) variation.[1] Additionally, reducing the gate oxide thickness to provide better channel control comes with a penalty of increased gate leakage current ($I_{\rm gate}$) and increased channel doping. In order to continue to improve the device performance and to follow the international technology roadmap for semiconductor (ITRS),[2] multiple gate transistor architectures are investigated beyond the 32-nm technology node, mainly because they provide a much better electrostatic control than conventional bulk silicon devices. The fin field-effect-transistor (FinFET) is considered to be a leading candidate because its multi-gate structure allows superior electrostatics over gate control and the compatibility with CMOS.[3] The complexity of the physical chemistry involved in the fabrication of advanced devices, with nanoscale feature sizes, and increasing computer power promote the use of advanced three-dimensional (3D) process modeling to reduce the challenges associated with actual processing. Also, to gain a better understanding of the single event effect (SEE) on advanced FinFETs, 3D simulation study is a necessary part of the radiation evaluation cycle.[4]

Single-event transient (SET) is the main radiation-induced noise and source of soft errors in advanced CMOS integrated circuits (ICs).[5−7] For combinational logic circuits, the time duration of SET determines the probability with which they will arrive at a storage cell during a latching edge of the clock signal, and thus causes the system output to have an error. SET on cross-coupled inverter nodes may cause a storage cell such as static random access memory (SRAM) and flip-flop to produce single event upset (SEU). The parameters that determine the transient pulse shape, such as charge generation and collection process after particle striking, are strong functions of operating temperature and drain bias. Thus, for circuits and devices operating in extreme space environments, temperature is an important factor in radiation hardening. Heavy ion tests and TCAD simulations show that single-event transient (SET) pulse width increases significantly with temperature rising in bulk CMOS technologies, which is caused mainly by the enhancement in the parasitic-bipolar action at elevated temperatures.[8−11]

Recently, dynamic supply voltage scaling (DVS) has been extensively employed to minimize the power of VLSI systems. A subthreshold circuit, which operates at a lower supply voltage than threshold voltage,

*Project supported by the State Key Program of the National Natural Science of China (Grant No. 60836004) and the National Natural Science Foundation of China (Grant Nos. 61076025 and 60906014).

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is a good candidate for ultralow power applications. However, SEE immunity of subthreshold circuits becomes a concern because both the amount of charge collection and the time required to remove the charge change with supply voltage decreasing.[12−14] Reference [12] shows that single event vulnerability does not show a linear relationship with power supply voltage in the subthreshold region. According to Ref. [14], the soft error rate (SER) at 0.3 V is eight times higher than the SER at 1.0 V for 65-nm 10-T SRAM cell.

However, to the best of our knowledge, there has been no study yet revealing the effects of temperature and power supply voltage on the SEE of a FinFET structure. In this paper, 3D device simulations are performed in a temperature range of 0–135 °C and supply voltage range of 0.4 V–1.6 V in 25-nm FinFET technology. The effects of temperature and supply voltage on charge collection and SET shapes are calculated. Simulation results are discussed and the mechanism of temperature and bias dependency is explained.

2. Simulation setup

Synopsys sentaurus TCAD is employed to study the characteristics of SET in the FinFET. The sentaurus process is performed to simulate a raised source-drain the FinFET using the MGOALS3D geometry library, similar to the one reported in Ref. [15]. The electrical characteristics of the device are simulated in three dimensions using the sentaurus device. The following physical models are used: (i) drift-diffusion transport model, (ii) Philips unified mobility model, (iii) high-field mobility degradation, (iv) mobility degradation at the silicon–oxide interface with Lombardi model, (v) density-gradient quantum corrections, (vi) piezo resistive model for stress, (vii) incident heavy ions which are modeled using a Gaussian radial profile with a characteristic $1/e$ radius of 30 nm and a Gaussian temporal profile with a characteristic decay time of 0.5 ps. All simulations are conducted on YINHE high performance computing cluster, and each case will cost about 8 h at a single computed node.

The raised source–drain 3D device structures generated from the Sentaurus Process are shown in Fig. 1. The stress memorization technique (SMT) pocket is used for the n-type FinFET, and the geometry with polyhedron insertion is used for the p-type FinFET. This is used as an SiGe pocket in the final device simulation.[15]

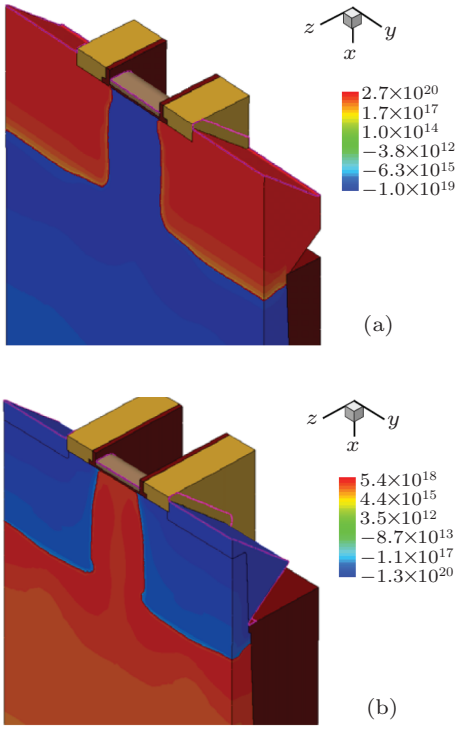


Fig. 1. (colour online) Three-dimensional structure of the FinFET device: (a) n-type FinFET, (b) p-type FinFET.

3. Device calibration

The doping profiles of the 3D models are calibrated by process simulations. Figure 2 shows the plots of drain current versus gate voltage characteristics for the n-type FinFET and the p-type FinFET. Two different drain biases 0.05 V and 1.0 V are simulated in this project for the n-type FinFET, and drain biases −0.05 V and −1.0 V are simulated for the p-type FinFET. These results are similar to those presented in the studies where the same process is used.[14−16] Very good agreement is also observed between the simulated threshold voltage ($V_{\rm tLin}$) and the leakage

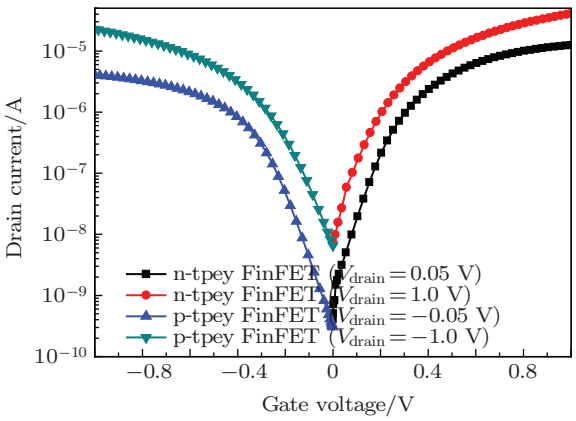


Fig. 2. (colour online) The $I_{\rm d}$–$V_{\rm gs}$ characteristics for (right) the n-type FinFET and (left) the p-type FinFET for two different drain biases.

current ($I_{\rm off}$) with those reported in the papers. Figure 3 shows the characteristics for drain current versus drain voltage for the n-type FinFET and the p-type FinFET.

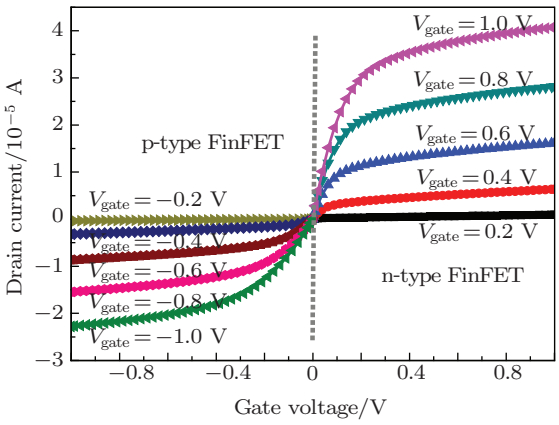


Fig. 3. (colour online) The $I_{\rm d}$–$V_{\rm ds}$ characteristics for (right) the n-type FinFET and (left) the p-type FinFET for five different gate biases.

4. Temperature dependence of charge collection and single event transient pulse shape

4.1. Charge collection versus temperature

Assuming that heavy ions strike at the centre of the reverse biased drain, the temperature dependence of the transient current is investigated. In Fig. 4, the drain currents of the p-type FinFET are plotted each as a function of time for three different temperatures when the device is struck by a 20-MeV·cm^2/mg heavy ion. The temperature plays a significant role in the shape of the transient current. When the temperature increases from 0 to 135 °C, the peak value of the drain current decreases from 229.5 μA to 216.9 μA. We define the duration as the time from the start of the current pulse to the moment when it first reaches 1 μA. Unlike the peak value, the duration of the transient current increases with temperature rising. It shows that the drain current pulse duration increases from 0.6 ns to 3.4 ns when the temperature increases from 0 to 135 °C.

Figure 5 shows the amount of charge collected by the p-type FinFET drain versus temperature. It can be seen that the charge collection of the p-type FinFET transistor increases evidently as temperatures rise. Especially, the increase rate jumps obviously when the temperature is larger than 80 °C.

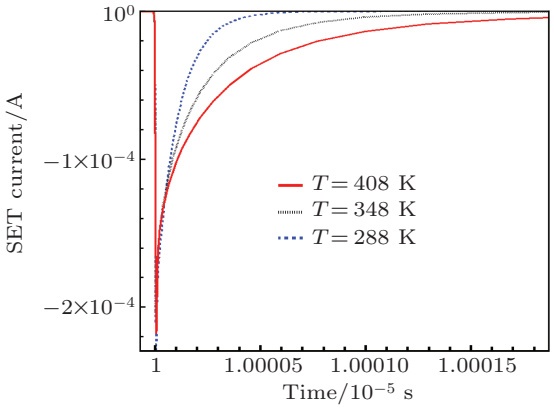


Fig. 4. (colour online) Current transient shapes for different temperatures after an ion striking.

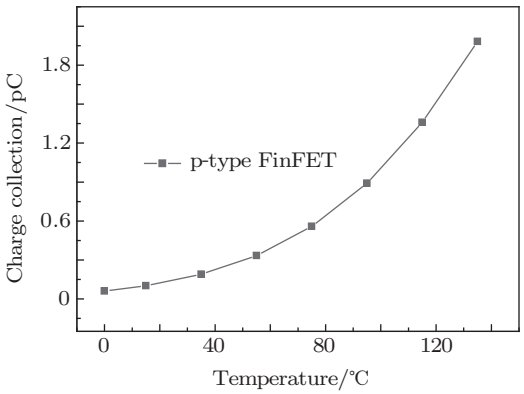


Fig. 5. Charge collection versus temperature for the p-type FinFET.

4.2. Single event transient voltage pulse width versus temperature

To study the temperature dependence of the circuit response, an inverter-chain is constructed in TCAD. Simulation results are shown in Fig. 6. As can be seen from the figure, the voltage full width at half rail (FWHR) pulse width increases with temperature rising, which is consistent with the trend in Fig. 6. The voltage transient is determined by charge collection, in other words, it is caused by

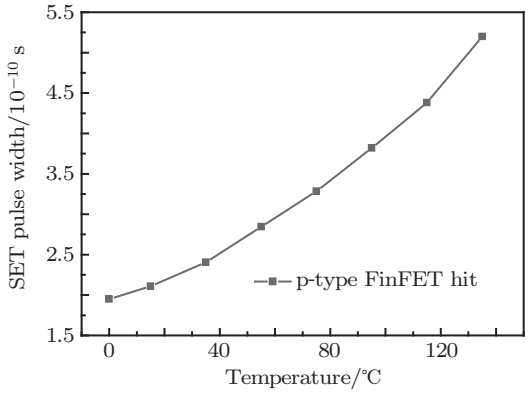


Fig. 6. SET pulse width versus temperature in an inverter chain for the p-type FinFET hit.

current transient. Consequently, the trends for charge collection versus temperature and pulse width versus temperature ought to remain the same.

Charge deposited increases with temperature rising because of band-gap narrowing. Band-gap narrowing of silicon is modeled in Sentaurus TCAD as

$$E_{\rm g} = E_{\rm g}(0) - \partial T^2/(T+\beta), \tag{1}$$

where T is the absolute temperature, $E_{\rm g}(0)$ is the band-gap energy at 0 K, α and β are material parameters. Average energy expended per ionized electron–hole pair in silicon is

$$\varepsilon = 2.2E_{\rm g}(T) + 0.96E_{\rm g}^{1.5}(T)\exp(0.75E_{\rm g}(T)/T). \tag{2}$$

According to expressions (1) and (2), the variation of charge deposited with temperature increasing from 0 to 135 °C can be estimated. Although deposited charge increases with temperature increasing, the increment is relatively small, and it is not the main cause for the temperature dependence of digital SET pulse width.

Earlier study has demonstrated that bipolar amplification is a dominant cause for digital SET pulse broadening with increasing temperature.[8,11] Enhancement of bipolar amplification with temperature increasing can be explained as follows. On the one hand, the resistance between the body contact and the bulk under the gate increases with temperature increasing, resulting in a higher well potential and corresponding larger bipolar amplification. On the other hand, the beta of the parasitic transistor also increases with temperature increasing.

5. Dependence of the single event effect on drain bias

In order to calculate the charge collected in a wide range of supply voltage, the FinFET transistor that can operate even in the subthreshold region is required. Figure 7 shows the amount of charge collected versus supply voltage for the p-type FinFET hit in a single transistor, and also the FWHR SET pulse width versus supply voltage at the inverter output node for a fixed particle LET. As supply voltage decreases, the charge collected by individual transistor increases and the FWHR pulse width decreases. The charge collected increases from 45.5 fC to 436.9 fC and the pulse width decreases from 0.54 ns to 0.18 ns when supply voltage increases from 0.4 V to 1.6 V. As described in Refs. [12] and [13], the amount of charge collected by the reversed drain–bulk junction depends mainly on the strength of the electric field in the funnel region. The electric field is weaker at a lower bias voltage than at a higher voltage. As the supply voltage decreases, the time required to remove the deposited charge increases, thereby increasing the SET pulse width. Thus, lower supply voltage results in a longer SET pulse, but smaller charge collected for a given LET.

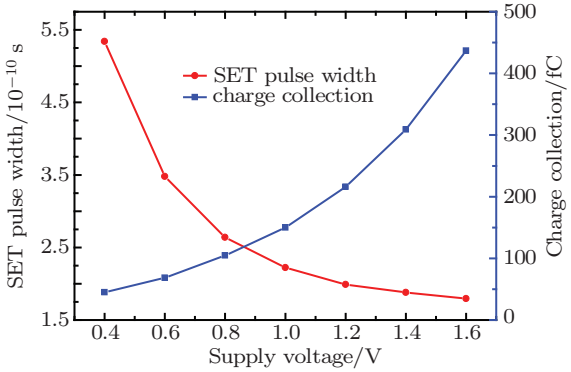


Fig. 7. (colour online) SET pulse width and charge collection versus supply voltage for the p-type FinFET hit.

Note that the charge collected by the p-type FinFET transistor drain is $Q_{\rm coll} = \int_{t=t0}^{\infty} I_{\rm SET}\,{\rm d}t$, where t_0 is the particle hit time. As a result, the $Q_{\rm coll}$ consists of two parts, i.e., the charge collected from the bulk where ion-impact ionization takes place, and the integral of the drain leakage current. The leakage current in the sub-threshold region is determined by

$$I_{\rm D} = I_{\rm S}\exp\left(\frac{V_{GS}}{nKT/q}\right)\left(1-\exp\left(-\frac{V_{\rm DS}}{KT/q}\right)\right) \times (1+\lambda V_{\rm DS}), \tag{3}$$

where $I_{\rm S}$ and n are empirical parameters, with $n \geq 1$, and typically ranging around 1.5.

Table 1. Values of drain leakage current $I_{\rm off}$ at different supply voltages.

No.	Supply voltage/V	Leakage current $I_{\rm off}$/nA
1	0.4	1.808521
2	0.8	2.51213
3	0.8	3.79459
4	1.0	5.97629
5	1.2	9.13752
6	1.4	13.56770
7	1.6	19.68980

The leakage current $I_{\rm off}$ at different supply voltages is calculated, and the results are shown in Table 1. We can see that $I_{\rm off}$ increases more than ten times when supply voltage changes from 0.4 V to 1.6 V. The leakage current as a function of supply voltage is shown in Fig. 8. Especially, the trend

of leakage current with respect to supply voltage is nearly the same as that of the charge collected in Fig. 8. Take supply voltage $V = 1.2$ V as an example: the charge collected by leakage current is about 9.13752 nA $\times 2.0\times 10^{-5}$ s (the simulation time), thus 182.75 fC, which is quite close to the total amount of charge 216.09 fC. It illustrates that the leakage current is a main contributor to charge collection. On the other hand, the leakage current rises exponentially with the supply voltage increasing, which is a shortcoming for multi-voltage circuit application.

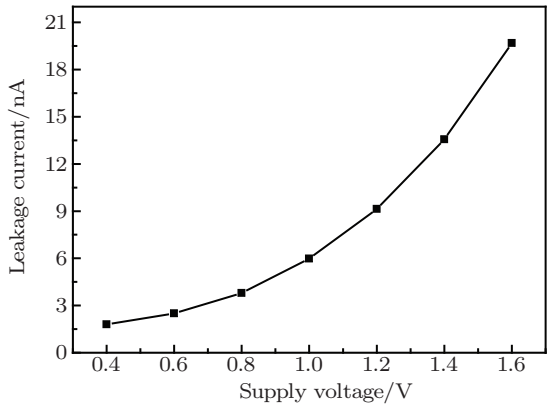


Fig. 8. Plot of leakage current $I_{\rm off}$ as a function of supply voltage.

6. Conclusion

Based on 25-nm raised source–drain FinFET CMOS technology, the temperature and drain bias dependence of single event transient (SET) is studied. TCAD 3D simulational results show that the drain current pulse duration increases from 0.6 ns to 3.4 ns when the temperature increases from 0 to 135 °C, implying that bipolar amplification is a dominant cause for SET pulse broadening with increasing temperature. The charge collected increases from 45.5 fC to 436.9 fC and the pulse width decreases from 0.54 ns to 0.18 ns when supply voltage increases from 0.4 V to 1.6 V. The electric field is weaker at a lower bias voltage than at a higher voltage and the time required to remove the deposited charge increases when bias voltage is lower. Thus, as the supply voltage decreases, the charge collected by the individual transistor increases and the SET pulse width decreases.

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