Fabrication and characterization of 4H–SiC bipolar junction transistor with double base epilayer*

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(Received 8 December 2011; revised manuscript received 13 January 2012)

In this paper we report on a novel structure of a 4H–SiC bipolar junction transistor with a double base epilayer that is continuously grown. The measured dc common-emitter current gain is 16.8 at $I_C = 28.6$ mA ($J_C = 183.4$ A/cm^2), and it increases with the collector current density increasing. The specific on-state resistance (R_{sp-on}) is 32.3 mΩ·cm^2 and the open-base breakdown voltage reaches 410 V. The emitter N-type specific contact resistance and N^+ emitter layer sheet resistance are 1.7×10^{-3} Ω·cm^2 and 150 $\Omega/\square$, respectively.

Keywords: 4H–SiC, bipolar junction transistors, common-emitter current gain, specific on-resistance, open-base breakdown voltage

PACS: 85.30.Pq, 51.50.+v, 78.40.Fy **DOI:** 10.1088/1674-1056/21/8/088502

1. Introduction

Silicon carbide (SiC) power devices are interesting for high-power, high-frequency, and high temperature applications. The power bipolar junction transistor (BJT) is an attractive power switching device free of gate oxide, and has a low specific on-state resistance (R_{sp-on}). At the same time, 4H–SiC power BJTs do not suffer from issues pertaining to metal–oxide-semiconductor (MOS) mobility, gate oxide reliability like the 4H–SiC power metal–oxide-semiconductor field-effect transistors (MOSFETs). In order to reduce the power required by the drive circuit, it is important to increase the common-emitter current gain (β).[1–4] In SiC device fabrication, ion implantation is often a key process step for forming a highly doped p-type Ohmic contact and implementing junction termination. However the problem is that it is difficult to achieve complete dopant activation even after high-temperature annealing, and it can generate lifetime-killing defects.

In our previous research, we have investigated the analytical models for the base transit time, the different structures of the junction termination extension and the high temperature characteristics.[5–7] In the present paper, we report on a 4H–SiC double-base epilayer BJT with an active area of 0.0156 mm^2 for the first time. This novel configuration can accelerate the carriers by the built-in electric field in the base region and reduce the base transit time. Also it can avoid the ion implantation process and reduce the defects introduced by the high-temperature annealing. This typical BJT has a common-emitter current gain of 16.8, a specific on-resistance of 32.3 mΩ·cm^2, and an open-base breakdown voltage of 410 V. The key steps in this approach include the precise control of the etch depth and the formation of a low-resistive P-type Ohmic contact to the epitaxial base.

2. Device design and fabrication

A schematic cross-sectional view of the fabricated 4H–SiC BJT is shown in Fig. 1. Four epilayers were grown on a 4° off-axis N-type 4H–SiC BJT. The structure consists of a 15-μm-thick, 1×10^{15} cm^{-3} N-type collector grown on the N^+ 4H–SiC substrate. The base epilayer consists of a 0.35-μm-thick 1×10^{17} cm^{-3}-doped epilayer, followed by a 0.15-μm-thick 4.6×10^{18} cm^{-3} P^+ epilayer. Finally, a 0.5-μm-thick 1×10^{19} cm^{-3} heavily doped N^+ emitter layer is

*Project supported by the National Natural Science Foundation of China (Grant No. 60876061) and the National Defense Key Laboratory Foundation from Nanjing National Defense Key Laboratory of Nanjing Electronic Devices Institute, China (Grant No. 20090C1403).

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grown. Figure 2 shows a secondary ion mass spectrometry (SIMS) profile of the base epilayers. It is formed with the epilayers growing continuously.

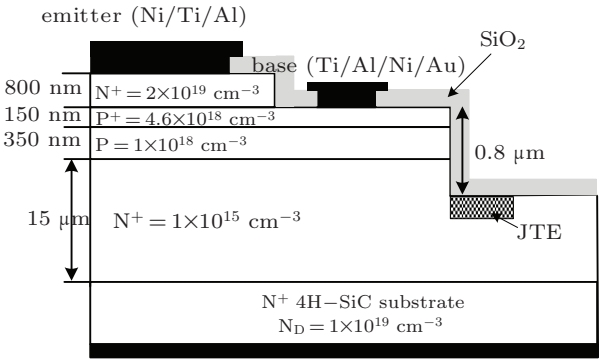


Fig. 1. Schematic cross section of the fabricated 4H–SiC BJT.

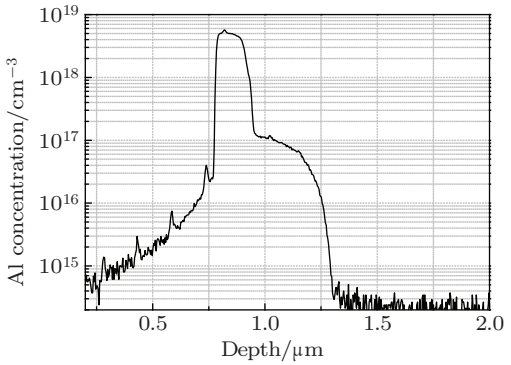


Fig. 2. Al SIMS profile for the base epilayer.

Figure 3 shows the scanning electron microscope (SEM) micrograph of the fabricated 4H–SiC BJT device.

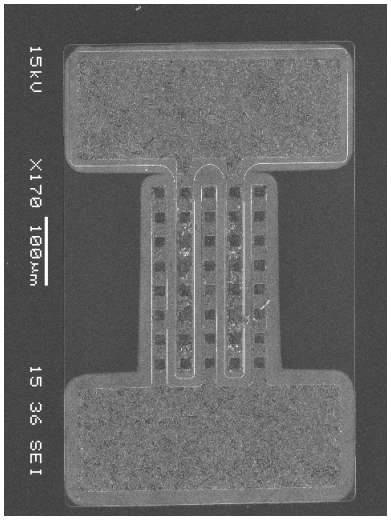


Fig. 3. SEM micrograph of the fabricated 4H–SiC BJT device.

Inductively coupled plasma (ICP) was applied to the dry etching process of the 4H–SiC BJT fabrication, including the emitter finger etching and the isolation mesa formation in a gas mixture of SF_6 and O_2 using the Ni mask. The spacing between the implanted base Ohmic region and the emitter mesa edge is 5 μm. The 4H–SiC surface passivation process included a 3-h wet thermal oxidation at 1100 °C, a 1-h dry thermal oxidation at 1050 °C, followed by a 0.5-h Ar annealing at 1100 °C. After the thermal oxidation, 180-nm SiO_2 were deposited by plasma-enhanced chemical vapour deposition (PECVD) to protect the thermal passivation layer. Contact windows were opened by ICP etching, lift-off patterning and annealing of Ni/Ti/Al and Ti/Al/Ni/Au to form the emitter and base contact respectively. The annealing condition was 1050 °C for 3 min in argon-forming gas (5% H_2 in Ar) in a rapid thermal processing (RTP) system. The low voltage part of the I–V characteristic curve is measured using a probe station equipped with an HP 4156B semiconductor parameter analyzer, while the high voltage part is measured by a Tektronix 371B curve tracer in this paper.

3. Results and discussion

Owing to the existence of the P^+ layer of the base region, the base Ohmic contact is formed on this layer directly. According to our previous research work, a built-in electric field was generated in the bulk of the base to accelerate the transition of the carriers. Therefore, it can reduce the transit time of the electron and improve the common-emitter current gain.

The analytical model of the base transit time for an NPN BJT can be expressed as[5]

$$\tau_{\rm b} = \frac{Q_{\rm B}\cdot J_{n\rm E}}{qD_{n\rm B}^2\cdot n_{i0}^2\cdot\exp\left(\dfrac{qV_{\rm E}}{kT}\right)}\left[\frac{1}{2}L_1^2+\frac{N_2}{N_1}L_1L_2 + \frac{N_1}{N_2}L_2\left(L_1-\frac{1}{2}L_2\right)+L_2^2\right], \quad (1)$$

where N_1 and L_1 are the doping concentration and the thickness of the P^+ layer respectively, and N_2 and L_2 are those of the P layer respectively.

Figure 4 shows the common-emitter ON-state I–V characteristic curves at room temperature of the fabricated BJT with 0.0156 mm^2 active area. The measured maximal DC current gain (β) is 16.8 at $I_{\rm C}$ = 28.6 mA ($J_{\rm C}$ = 183.4 A/cm^2) when $V_{\rm CE}$ = 22 V. In the saturation region, the specific on-resistance was

measured to be 32.3 mΩ·cm^2 (based on the active area) at room temperature. This higher current gain is achieved owing to the built-in electric field created in the novel base region, thereby requiring neither ion implantation nor high-temperature activation annealing.

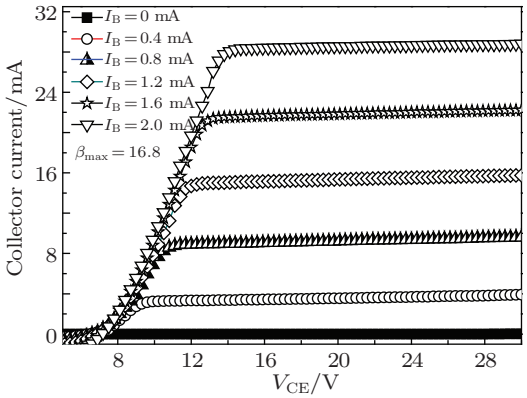


Fig. 4. (colour online) Room-temperature ON-state I_C versus V_{CE} characteristic curves at $V_{CE} = 22$ V.

Figure 5 shows the on-chip transmission line modeling (TLM) structure measurements of the emitter N-type Ohmic contact. The emitter N-type specific contact resistance and N^+ emitter layer sheet resistance are 1.7×10^{-3} Ω·cm^2 and 150 $\Omega/\square$, respectively.

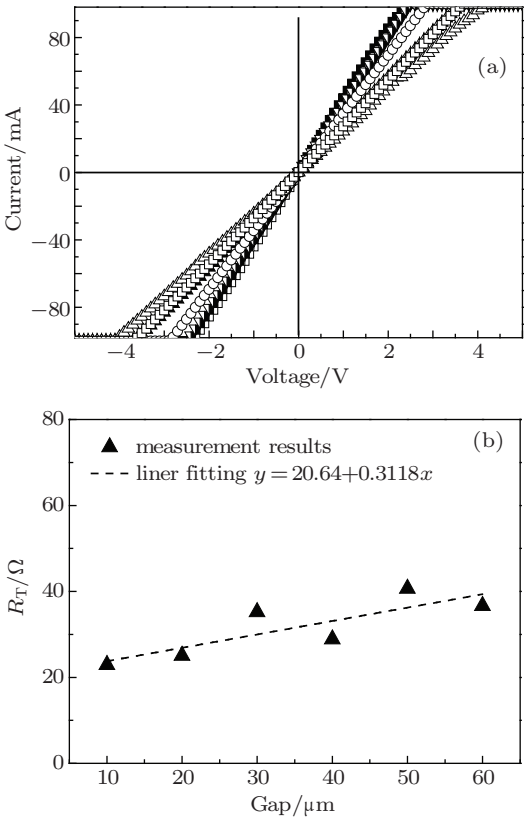


Fig. 5. On-chip TLM measurements of the emitter N-type Ohmic contact (a) TLM I–V characteristic curves, and (b) TLM fitting curve.

Figure 6 shows an experimental relation between common-emitter (CE) current gain (β) and collector current density (J_C). It is seen that β first increases and then decreases at higher J_C. Under the condition of low injection, the base transport factor increases with the injection current increasing. However, under the influences of the self-heating and the series resistance, the current gain decreases at a higher collector current density. The β can keep constant in a wide current range.

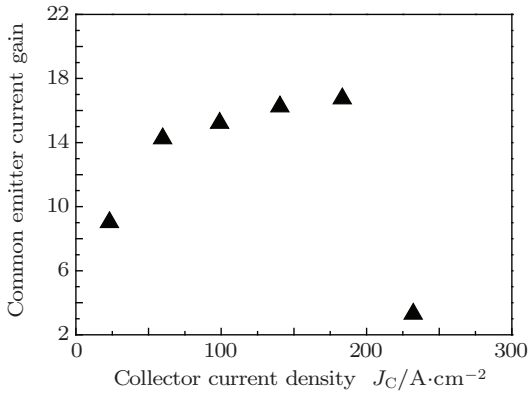


Fig. 6. Current gain in CE configuration versus the collector current density at 300 K.

Figure 7 displays the measurement results of emitter-collector leakage current versus V_{CE} in the open base mode. It can be found that the BV_{CEO} is measured to be 410 V. It is mainly because the incomplete ionization of the base region and the punch through phenomenon appear in the bulk of the base. Another, further improvement of the device performance is possible by using a better performing edge termination structure.

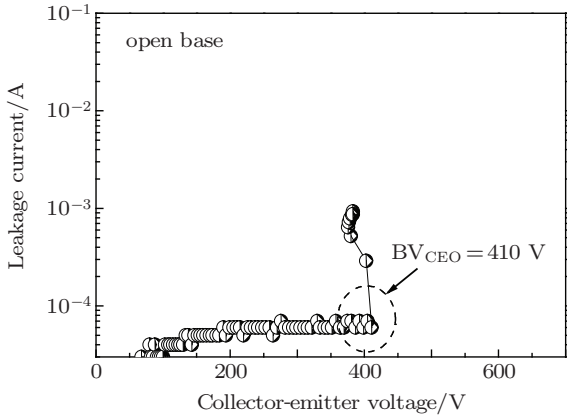


Fig. 7. Measured leakage current versus V_{CE}.

4. Conclusion

A 4H–SiC power BJT with a double base epilayer structure is demonstrated successfully in this paper for the first time. A room temperature dc current gain of 16.8 is measured. The current gain is substantially increased by optimizing the base structure to accelerate the transit of the carriers. The specific on-resistance of 32.3 mΩ·cm^2 and an open-base breakdown voltage of 410 V are measured at room temperature. Further optimization of precise control of the etching depth and the P-type Ohmic contact is needed to improve the dc characteristics of this typical device.

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