Degradation of the transconductance of a gate-modulated generation current in nMOSFET*

Chen Hai-Feng(陈海峰)†, Guo Li-Xin(过立新), and Du Hui-Min(杜慧敏)

School of Electronic Engineering, Xi'an University of Posts and Telecommunications, Xi'an 710121, *China*

(Received 15 January 2012; revised manuscript received 27 April 2012)

The degradation of transconductance (G) of a gate-modulated generation current $I_{\rm GD}$ in a LDD nMOSFET is investigated. The G curve shifts rightward under the single electron-injection-stress (EIS). The trapped electrons located in the gate oxide over the LDD region ($Q_{\rm L}$) makes the effective drain voltage diminish. Accordingly, the G peak in depletion ($G_{\rm MD}$) and that in weak inversion ($G_{\rm MW}$) decrease. It is found that $\Delta G_{\rm MD}$ and $\Delta G_{\rm MW}$ each have a linear relationship with the n-th power of stress time (t^n) in a dual-log coordinate: $\Delta G_{\rm MD} \propto t^n$, $\Delta G_{\rm MD} \propto t^n$ ($n = 0.25$). During the alternate stress, the injected holes neutralize $Q_{\rm L}$ induced by the previous EIS. This neutralization makes the effective $V_{\rm D}$ restore to the initial value and then the $I_{\rm GD}$ peak recovers completely. Yet the threshold voltage recovery is incomplete due to the trapped electron located over the channel ($Q_{\rm C}$). As a result, $G_{\rm MW}$ only recovers to circa 50% of the initial value after the hole-injection-stress (HIS). Instead, $G_{\rm MD}$ almost recovers. The relevant mechanisms are given in detail.

Keywords: generation current, transconductance, electron injection, alternate stress, degradation

PACS: 85.30.De，85.30.Tv **DOI:** 10.1088/1674-1056/21/8/088501

1. Introduction

The gate-modulated generation current $I_{\rm GD}$ in a metal–oxide semiconductor field-effect transistor (MOSFET) is a drain current generated in interface traps under the weakly reverse drain bias.[1,2] In the $I_{\rm GD}$ measurement a classical current hump is often present. This current hump is formed by an increase and subsequent decrease as the gate is swept from accumulation to depletion and then to inversion.[3] The changes in the hump shape and peak can indicate information about the interface traps and oxide-trapped charges.[4−6] Therefore, So $I_{\rm GD}$ is widely utilized to characterize the hot-carrier or radiation-induced damage in the device. Lee *et al.*[7] used this modulated current to study the positive-bias-temperature-effect (PBTI) on nMOSFET with a 1-nm-thick gate oxide.[7] In Refs. [8] and [9], the radiation-induced influence of the device is also observed through this method. Additionally, Goiffon *et al.*[10] used this current hump to study the total dose effect of the device and then on the image sensors.

These studies mentioned above focus mainly on the $I_{\rm GD}$ peak degradation post damage. Although the $I_{\rm GD}$ peak is characterized well, the whole physical picture of $I_{\rm GD}$'s degradation is still not clear. The reason for this is that the $I_{\rm GD}$ curve has the other two important parts, the rising edge and the falling edge, except for the $I_{\rm GD}$ peak. The rising edge and falling edge change after the damage. These changes can be reflected by the values of the gate controlling $I_{\rm GD}$ in different $V_{\rm G}$ regions. Thus it is necessary to introduce $I_{\rm GD}$ transconductance (G) to study its variation. However, so far little attention has been paid to G in this field.

In the present paper, we study the degradation of transconductance of $I_{\rm GD}$ in LDD nMOSFET. G is extracted under single electron-injection-stress (EIS) and alternate stress. Through analyzing the relationship of the G's variation and the trapped charges, the G degradation is deeply discussed and the relevant mechanisms are given.

2. $I_{\rm GD}$ and transconductance physics

The gate-modulated generation current $I_{\rm GD}$ is in direct proportion to the generation rate R of interface

*Project supported by the Shaanxi Provincial Research Project of Education Department, China (Grant No. 11JK0902) and the Xi'an Municipal Applied Materials Innovation Fund, China (Grant No. XA-AM-201012).

†Corresponding author. E-mail: chenhaifeng@xupt.edu.cn

© 2012 Chinese Physical Society and IOP Publishing Ltd

traps according to the Shockley–Read–Hall generation theory.[11] It can be described as

$$I_{\rm GD} \propto R. \tag{1}$$

Assuming that this generation trap is located in the midgap of Si and equally captures electrons and holes, the expression of R is[12]

$$R = \frac{N_{\rm it}\sigma v_{\rm th}(n_{\rm s}p_{\rm s} - n_{\rm i}^2)}{n_{\rm s} + p_{\rm s} + 2n_{\rm i}}, \tag{2}$$

where $n_{\rm i}$ is the intrinsic density of the electron and hole; $n_{\rm s}$ and $p_{\rm s}$ are the electron and hole density at the surface, respectively; $N_{\rm it}$ is the density of the interface traps; σ is the capture cross section; $v_{\rm th}$ is the thermal velocity. R reaches its maximum if $n_{\rm s} = p_{\rm s}$ in Eq. (2). When applied, $V_{\rm D}$ is a small voltage and the channel is in a non-equilibrium state as seen from Fig. 1(a). Then, $n_{\rm s}$ and $p_{\rm s}$ are expressed as

$$\begin{aligned} n_{\rm s} &= n_{\rm i}\exp((E_{\rm FN} - E_{\rm i})/kT) \\ &= n_{\rm i}\exp(q(\varphi_{\rm s} - \varphi_0 - V_{\rm D})/kT), \end{aligned} \tag{3}$$

$$p_{\rm s} = n_{\rm i}\exp(E_{\rm i} - E_{\rm FP}) = n_{\rm i}\exp(q(\varphi_0 - \varphi_{\rm S})/kT), \tag{4}$$

where $\varphi_{\rm s}$ is the surface potential; φ_0 is the difference between $E_{\rm i}$ and $E_{\rm FP}$; $E_{\rm FP}$ and $E_{\rm FN}$ are the quasi-Fermi levels for the hole and electron, respectively.

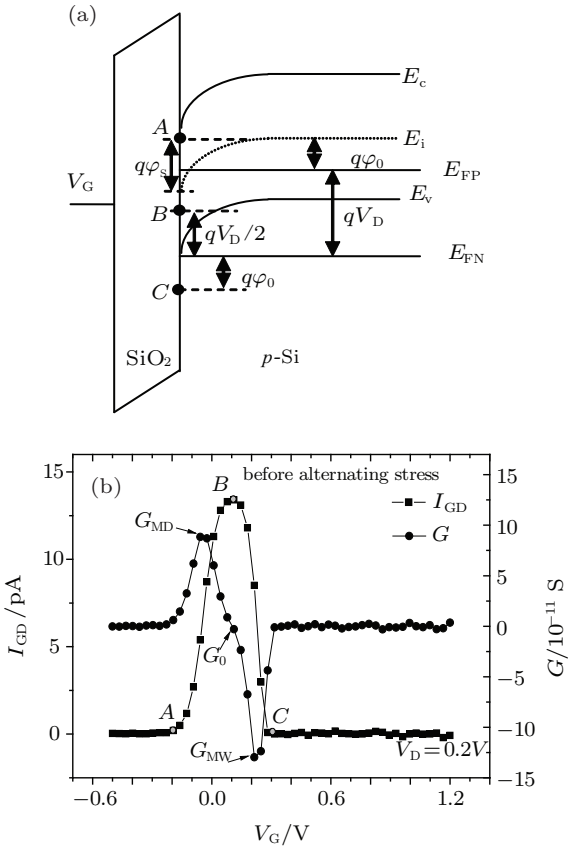


Fig. 1. (a) The diagram of band bending when $v_{\rm G}$ varies; (b) $I_{\rm GD}$ at $V_{\rm D} = 0.2$ V and its transconductance G. $G_{\rm MD}$ and $G_{\rm MW}$ are the maximal values of G in the depletion region (the rising edge of $I_{\rm GD}$ curve) and in weak inversion (the falling edge of $I_{\rm GD}$ curve), respectively. G_0 is the value of G at $I_{\rm GD}$ peak and $G_0 = 0$.

So, R is

$$R = \frac{N_{\rm it}\sigma v_{\rm th} n_{\rm i}(1 - \exp(-qV_{\rm D}/kT))}{\exp(q(\varphi_{\rm S} - \varphi_0 - V_{\rm D})/kT) + \exp(q(\varphi_0 - \varphi_{\rm S})/kT) + 2}. \tag{5}$$

Deduced from Eq. (5), R approaches the peak when $\varphi_{\rm S}$ is equal to $\varphi_0 + V_{\rm D}/2$, because $I_{\rm GD}$ depends on R and R varies with $\varphi_{\rm S}$. Scanning the gate bias $V_{\rm G}$ can vary the silicon surface potential $\varphi_{\rm S}$ from accumulation to depletion and so $I_{\rm GD}$ changes with $V_{\rm G}$. Figure 1(b) shows the $I_{\rm GD}$–$V_{\rm G}$ curve and a hump appearing on the curve. In this hump, A is the flatland point, B is the peak point ($n_{\rm S} = p_{\rm S}$ or surface intrinsic state) and C is the threshold voltage ($V_{\rm th}$) point. Based on the above discussion, A, B, and C correspond to $\varphi_{\rm S} = 0$, $\varphi_{\rm S} = \varphi_0 + V_{\rm D}/2$, and $\varphi_{\rm S} = V_{\rm D} + 2\varphi_0$ in Fig. 1(a), respectively. Obviously, the A–B region is the depletion region and the B–C region is the weak inversion region.

The transconductance of $I_{\rm GD}$ is defined as G and expressed as

$$G = \partial I_{\rm GD}/\partial V_G. \tag{6}$$

Based on the above discussion, there should be

$$\partial I_{\rm GD}/\partial V_{\rm G} \propto \partial I_{\rm GD}/\partial \varphi_{\rm S} \propto \partial R/\partial \varphi_{\rm S}. \tag{7}$$

From Eq. (5), $\partial R/\partial \varphi_{\rm S}$ can be deduced. Then,

$$G \propto \partial R/\partial \varphi_{\rm S} = a(V_{\rm D}) * b(\varphi_{\rm S}), \tag{8}$$

where

$$a(V_{\rm D}) = N_{\rm it}\sigma v_{\rm th} n_{\rm i}[1 - \exp(-qV_{\rm D}/kT)], \tag{9}$$

$$b(\varphi_{\rm S}) = \frac{q[\exp(q(\varphi_{\rm S} - \varphi_0 - V_{\rm D})/kT) - \exp(q(\varphi_0 - \varphi_{\rm S})/kT)]/kT}{[\exp(q(\varphi_{\rm S} - \varphi_0 - V_{\rm D})/kT) + \exp(q(\varphi_0 - \varphi_{\rm S})/kT) + 2]^2}. \tag{10}$$

G reflects the ability of the gate controlling I_{GD}. G at B point is denoted as G_0, and is equal to 0 because it is the peak of the curve. I_{GD} is almost 0 in accumulation and strong inversion and the values of G at A and C points are also equal to 0. So there is a hump located in the A–B region and another hump in the B–C region as shown in Fig. 1(b). The G hump peak in the A–B region is the maximum depletion G (G_{MD}) and that in the B–C region is the maximum weak inversion G (G_{MW}). G_{MD} and G_{MW} can indicate the maximum ability of the gate controlling I_{GD} in the depletion region and the weak inversion region.

It is well known that the hot carriers should be injected into the gate oxide under stress.[13,14] These charges can affect φ_S and V_D. Then, according to Eq. (8), G_{MD} and G_{MW} can change as well. The degradations of G_{MD} and G_{MW} can show the influence of a trapped charge on I_{GD}.

3. Results and discussion

The two devices used in this study are an LDD nMOSFET with an n+ poly-Si gate fabricated by 90-nm CMOS technology. The gate oxide thickness is 4 nm using the decoupled-plasma-nitridation process. The gate length is 0.28 μm and the gate width is 6 μm. For the I_{GD} measurement, the gate is swept from accumulation to strong inversion (-0.5 V $< V_G <$ 1.2 V) at V_D = 0.2 V by floating the source and grounding the substrate, the current then collected by the drain is I_{GD}. G is extracted from I_{GD} pre and post the stress. All electrical tests and stresses are performed using a Keithley 4200 precision semiconductor parameter analyzer.

3.1. Single stress

Figure 2 shows the I_{GD} curves pre and post the electron-injection-stress (EIS). The EIS condition is $V_G = V_D$ = 3.0 V and the stress period lasts 500 s. The I_{GD} curve shifts rightwards and downwards. According to Eq. (6), G is extracted from Fig. 2(a) and shown in Fig. 2(b).

During EIS, there are few or no interface traps generated since I_{GD} in the accumulation region (-0.5 V $< V_G <$ -0.2 V) does not increase after EIS. If the EIS creates new additional interface traps, the I_{GD} in the accumulation region should increase due to the trap assistant band-to-band tunneling. Then, the EIS mainly induces the electron trapping. The electrons are injected into the gate oxide around the gate-drain overlap region. The locations of these trapped electrons cover the gate oxide region both over the channel and the LDD region around the PN junction. The negative charges trapped on the side of channel and LDD region are denoted with Q_C and Q_L, respectively. Accordingly, Q_C and Q_L can reduce φ_S and make the I_{GD} curve shift rightwards. Then, the G curve in Fig. 2(b) also shifts rightward. Since Q_L is located over the LDD region and is negative, it can reduce the effective V_D. Therefore, a (V_D) and b (φ_S) in Eq. (8) decrease and the G peak decreases. This result is shown by the fact that G_{DM} and G_{WM} decrease as the stress time increases in Fig. 2(b). The mechanism of the G peak change above is based on the rationality of the existence of Q_L. If Q_L exists, the maximum of R should be diminished according to Eq. (5) and make the I_{GD} peak decrease. In Fig. 2(a), the peak of the I_{GD} curve decreases after EIS. This result proves the rationality of existence of Q_L.

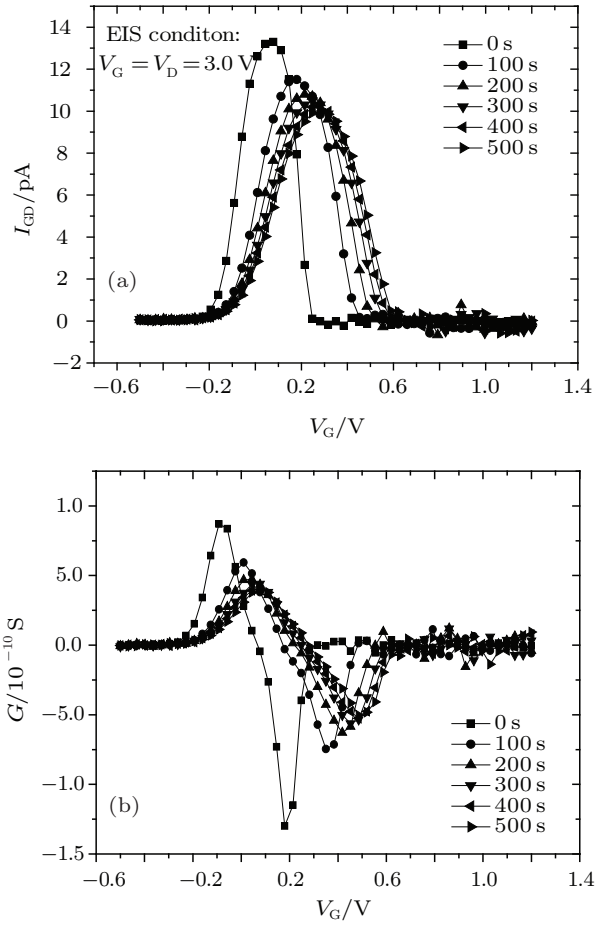


Fig. 2. (a) Curves of I_{GD} before and after a single EIS; (b) curves of G pre and post single EIS. EIS condition: $V_G = V_D$ = 3 V.

Further, Figure 3 shows $\Delta G_{\rm MD}$ and $\Delta G_{\rm MW}$ extracted from Fig. 2(b). It can be seen that both $\Delta G_{\rm MD}$ and $\Delta G_{\rm MW}$ each have a linear relationship with the n-th power of stress time (t^n) in dual-log coordinates. Namely, $\Delta G_{\rm MD} \propto t^n$ and $\Delta G_{\rm MD} \propto t^n$. n denotes the slope of the curve, and $n = 0.25$ in Fig. 3. These expressions are very similar to the traditional hot carrier induced degradation expression: $\Delta \propto t^n$.[15] It indicates that the G peak can also evaluate the degradation of the device.

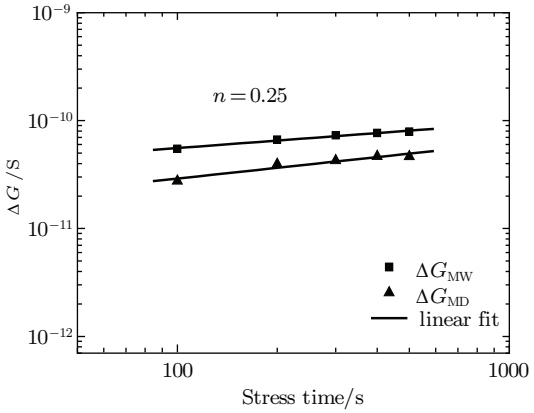


Fig. 3. Relationship between G shift and stress time in dual-log coordinates.

3.2. Alternate stress

Figure 4 shows the G curves of pre and post alternate stresses. The alternate stress is composed of the first EIS period stress and the following hot–hole–injection stress (HIS) period stress. The EIS condition is also $V_{\rm D} = V_{\rm G} = 3.0$ V. HIS adopts the gated-induced drain leakage (GIDL) stress:[16–18] $V_{\rm G} = -1.5$ V and $V_{\rm D} = 3.0$ V. The total time of the alternate stress is 500 s and each single stress period lasts 250 s. It is exhibited that the G curve shifts rightwards and downwards as the stress time increases from 0 s to 250 s in the EIS period in Fig. 4(a). During the sequent HIS, the G curve starts to restore from the end of the EIS state to the initial state (0 s) as can be seen in Fig. 4(b).

Figure 5 shows the relationship of $G_{\rm MD}$ and $G_{\rm MW}$ with the stress time extracted from Fig. 4. After the EIS period, $G_{\rm MD}$ and $G_{\rm MW}$ decrease with stress time increasing and degrade 25% compared with the initial values. The sequent 50-s HIS makes the degraded $G_{\rm MD}$ and $G_{\rm MW}$ increase and these increases almost step into saturation as the HIS continues. The gate voltage region of the weak inversion region of the $I_{\rm GD}$ curve is from the gate voltage at B point ($I_{\rm GD}$ peak) to C point ($V_{\rm th}$). Due to the fact that G_0 which is G at B point is equal to zero, it can be seen that G_0 shifts towards the positive gate voltage as the EIS continues from Fig. 4(a). GIDL HIS takes place in the LDD region and injects holes into the gate oxide above. As aforementioned, $Q_{\rm C}$ and $Q_{\rm L}$ are created during the EIS. So these holes created during HIS should neutralize $Q_{\rm L}$. It is known that $Q_{\rm L}$ dominates the $I_{\rm GD}$ peak from the discussion in the above section. So G_0 returns to the initial position after HIS as shown in Fig. 4(b). This indicates that the gate voltage at the $I_{\rm GD}$ peak keeps constant before and after the alternating stress.

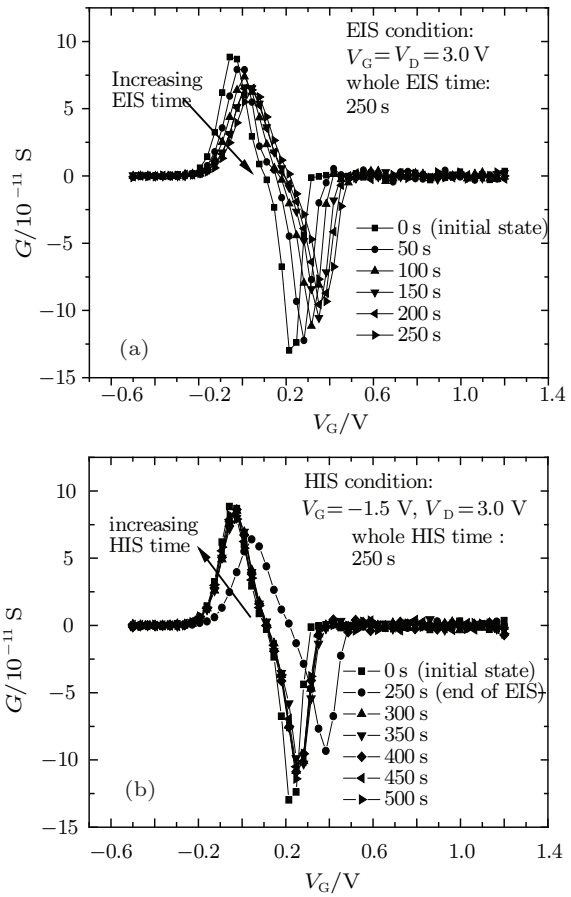


Fig. 4. Degradations and recoveries of the transconductance G of $I_{\rm GD}$ extracted from Fig. 3. (a) The 1st period: 250-s EIS from 0 s to 250 s; (b) the 2nd period: 250-s GIDL HIS from 250 s to 500 s.

Further, both $Q_{\rm C}$ and $Q_{\rm L}$ can affect $V_{\rm th}$ (C point) and make $V_{\rm th}$ increase. However, $Q_{\rm C}$ located over the channel cannot be neutralized during the GIDL HIS and this makes the C point shift from its initial position C_0 to the post-stress position $C_{\rm post}$. Compared with C_0 corresponding to $\varphi_{\rm S} = V_{\rm D} + 2\varphi_0$, $C_{\rm post}$ corresponds to $\varphi_{\rm S} = V_{\rm D} + 2\varphi_0 + |Q_{\rm C}|/C_{\rm OX}$. As a result,

$V_{\rm th}$ after HIS is still larger than the initial value. So the weak inversion region of the $I_{\rm GD}$ curve increases compared with the initial curve in Fig. 5(b). In addition, the $I_{\rm GD}$ peak (B point) after the stress is almost the same as the initial value so that $G_{\rm MW}$ decreases and cannot be restored to the initial value. Because the holes in HIS neutralize $Q_{\rm L}$ and the effective $V_{\rm D}$ restores to the initial value, the voltage applied to the drain PN junction after HIS becomes the same as that before the stress. Consequently, the depletion around the drain PN junction after HIS also becomes the same as that before the alternate stress and the $I_{\rm GD}$ curve in the depletion region almost restores to the initial state as shown in Fig. 5(b). Consequently, the $G_{\rm MD}$ degradation almost recovers its initial value after the alternating stress. Based on the above mechanisms, Figure 5(a) shows a difference in recovery of the degradation induced by the previous EIS between $G_{\rm MD}$ and $G_{\rm MW}$ during the alternating stress. In the case of $G_{\rm MD}$, HIS makesalmost recovers the degradation. However, HIS recovers only circa 50% of $G_{\rm MW}$'s degradation.

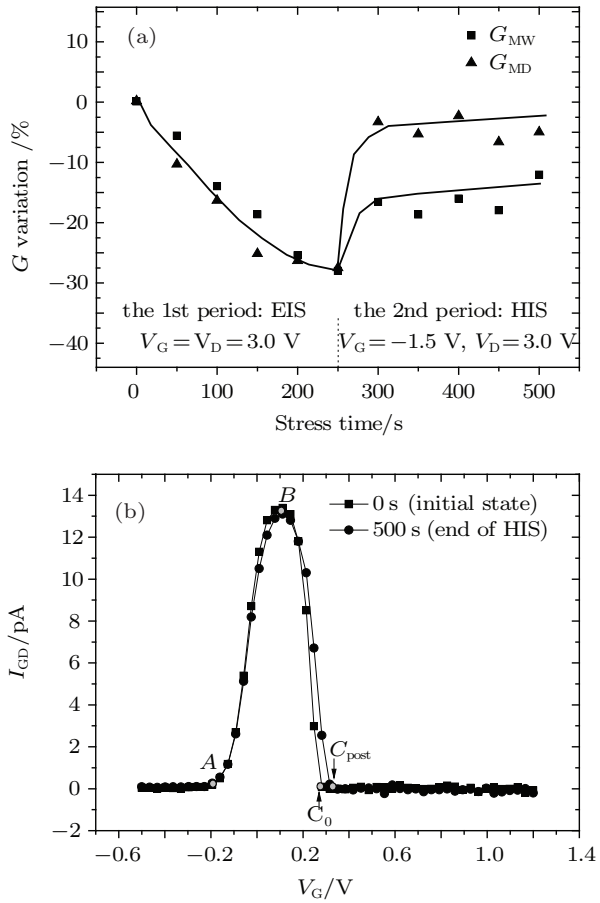


Fig. 5. (a) Variations of $G_{\rm MD}$ and $G_{\rm MW}$ versus the alternate stress time; (b) comparison of the $I_{\rm GD}$ curve before and after the alternate stress.

4. Conclusion

The degradation of the transconductance (G) of a gate-modulated generation current $I_{\rm GD}$ in a LDD nMOSFET is investigated under single and alternate stresses in this paper. During EIS, the electrons are injected into the gate oxide around the gate–drain overlap region and form $Q_{\rm C}$ and $Q_{\rm L}$. Since $Q_{\rm L}$ reduces the effective $V_{\rm D}$, $G_{\rm MD}$ and $G_{\rm MW}$ decrease with increasing EIS time. It is found that $\Delta G_{\rm MD}$ and $\Delta G_{\rm MW}$ each have a linear relationship with the n-th power of stress time (t^n) in dual-log coordinates: $\Delta G_{\rm MD} \propto t^n$, $\Delta G_{\rm MD} \propto t^n$ ($n = 0.25$). These expressions of degradation of $G_{\rm MD}$ and $G_{\rm MW}$ are very similar to the traditional hot carrier induced degradation expression ($\Delta \propto t^n$) and they have potential applications in the evaluation of device damage. During the alternate stress, hot holes are injected during the HIS which neutralizes $Q_{\rm L}$ induced by the previous EIS. This neutralization makes the effective $V_{\rm D}$ increase and almost restores it to the initial value so that the $G_{\rm MD}$ degradation almost recovers to the initial value. However, the threshold voltage recovery is incomplete since $Q_{\rm C}$ is not neutralized during HIS. Accordingly, $G_{\rm MW}$ decreases and cannot be restored to the initial value (circa 50%) after the alternate stress.

These results in this paper should be helpful for understanding the degradation of a gate-modulated generation current using the transconducatance method.

References

[1] Pan J 2009 *IEEE Trans. Electron Dev.* **56** 1350

[2] Rusu A, Badila M and Rusu A 2011 *IEEE Conference on Microelectronic Test Structures* April 4–7, 2011, Amsterdam, The Netherlands p. 136

[3] Chang Y K, You S W, Juan P C, Wang M T and Lee Y M 2009 *IEEE Electron Dev. Lett.* **30** 161

[4] Giebel T and Goser K 1989 *IEEE Electron Dev. Lett.* **10** 76

[5] Czerwinski A, Simoen E, Poyai A, Claeys C and Ohyama H 2003 *IEEE Trans. Nucl. Sci.* **50** 278

[6] Randriamihaja Y M, Bravaix A, Huard V, Rideau D, Rafik M and Roy D 2010 *IRW Final Report* October 17–21, 2010, Crolles, France, p. 61

[7] Lee G D, Chung S S, Mao A Y, Lin W M, Yang C W and Hsieh Y S 2006 *Proceedings of 13rd IPFA*, July 3–7, Singapore, p. 37

[8] Felix J A, Shaneyfelt M R, Dodd P E, Draper B L, Schwank J R and Dalton S M 2005 *IEEE Trans. Nucl. Sci.* **52** 2378

[9] Rao P R, Wang X Y and Theuwissen A J 2008 *Solid-State Electronics* **52** 1407

[10] Goiffon V, Magnan P, Saint-pe O, Bernard F and Rolland G 2008 *IEEE Trans. Nucl. Sci.* **55** 3439

[11] Goifon V, Virmontois C, Magnan P, Girard S and Paillet P 2010 *IEEE Trans. Nucl. Sci.* **57** 3087

[12] Shi M and Wu G Y 2008 *Physics of Semiconductor Devices* (Xi'an: Xi'an Jiaotong University Press) p. 33

[13] Chen Y Y, Hsieh C and Chiu F G 2011 *Appl. Phys. Lett.* **98** 033501

[14] Chen J J, Chen S M, Liang B, He Y B, Chu Y Q and Deng K F 2011 *Chin. Phys.* B **20** 114220

[15] Eiji T, Yang C Y and Akemi M 1995 *Hot-Carrier Effects in MOS Devices* (San Diego: Academic Press) p. 82

[16] Chen H F, Hao Y and Ma X H 2007 *Acta Phys. Sin.* **56** 1662 (in Chinese)

[17] Ma X H, Cao Y R, Gao H X, Chen H F and Hao Y 2009 *Appl. Phys. Lett.* **95** 152107

[18] Han J W, Moon D I, Kim D H and Yang Choi Y K 2009 *IEEE Electron Dev. Lett.* **30** 1108