Low-voltage antimony-doped SnO_2 nanowire transparent transistors gated by microporous SiO_2-based proton conductors*

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A battery drivable low-voltage transparent lightly antimony(Sb)-doped SnO_2 nanowire electric-double-layer (EDL) field-effect transistor (FET) is fabricated on an ITO glass substrate at room temperature. An ultralow operation voltage of 1 V is obtained on account of an untralarge specific gate capacitance (~ 2.14 μF/cm^2) directly bound up with mobile ions–induced EDL (sandwiched between the top and bottom electrodes) effect. The transparent FET shows excellent electric characteristics with a field-effect mobility of 54.43 cm^2/V·s, current on/off ration of 2×10^4, and subthreshold gate voltage swing ($S = \mathrm{d}V_{\mathrm{gs}}/\mathrm{d}(\log I_{\mathrm{ds}})$) of 140 mV/decade. The threshold voltage V_{th} (0.1 V) is estimated which indicates that the SnO_2 namowire transistor operates in an n-type enhanced mode. Such a low-voltage transparent nanowire transistor gated by a microporous SiO_2-based solid electrolyte is very promising for battery-powered portable nanoscale sensors.

Keywords: electric double layer, proton conductor, solid electrolytes, nanowire transistors

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1. Introduction

Substantial effort has been devoted to the developing of a SnO_2 nanowire as a building block for electronic device, due to its fascinating physical and chemical properties, such as a large band gap $E_{\mathrm{g}} = 3.6$ eV, low resistivity of 10^{-4} Ω·cm–10^{-6} Ω·cm and high optical transparency in the visible range (up to 97%). The SnO_2 nanowire is widely regarded as an attractive material for potential applications of chemical sensors, field-emission transistors, dye-based solar cells, and so on.[1−8] At the same time, Li *et al.*[9,10] reported on the research of the ZnO nanowire field-effect transistor with a high on–off current ratio of $\sim 10^5$ and its characterization when exposed to ultraviolet radiation. A field effect transistor (FET) with a SnO_2 nanowire as an active channel has been extensively investigated in the past decades.[11] In general, the operation voltage was too high because of the weak capacitive coupling of commonly used SiO_2 gate dielectrics between the gate electrode and the active layer. The lower the operation voltage, the less energy it consumes. Diminishing the operation voltage is an effective way to optimize the property of transistors. As is well known, film fabricated at near room temperature has exhibited a modest performance-showing with an unacceptably large operating voltage as shown in Refs. [12] and [13]. To obtain low operating voltages of transistors fabricated on glass and paper substrates at room temperature, it is crucial to find a gate dielectric with a large specific gate capacitance. Two approaches to the increasing of the gate specific capacitance are (i) to reduce the dielectric film thickness and (ii) to find a high relative permittivity (high-κ) gate dielectric. Kim *et al.*[14] reported that the operation voltage of an organic thin film transistor (OTFT) was as low as 2 V due to the use of CeO_2–SiO_2 nanocomposite films-based solid electrolyte with high κ. Recently, a low-voltage oxide-based-thin-film transistor gated by microporous SiO_2 with huge EDL capacitance has been demonstrated by our group.[15,16] In the present paper, the operation voltage of an individual SnO_2 nanowire FET is reduced to 1 V due to the huge EDL capacitance of microporous SiO_2-based solid electrolyte. The field-effect electron mobility, current on/off ratio, and subthreshold slope of the transistors are estimated to be 54.43 cm^2/V·s, 2×10^4, 140 mV/decade respectively.

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2. Experiments

Lightly Sb-doped SnO_2 nanowires were synthesized on 10-nm Au covered-Si(100) substrates by the vapour–liquid–solid (VLS) growth mechanism at 900 °C. The specific process was described as follows: well mixed powders of Sb:Sn (1:1000) were first loaded in an alumina boat as the source material, and silicon chips coated with a 10-nm-thick Au film were placed on the top of the alumina boat as a growth substrate. Then the quartz boat was inserted into the quartz tube, and located in the middle of the tube. The furnace was heated from room temperature to 900 °C at a rate of 20 deg $\cdot$ min^{-1} with the source upstream of high purity Ar gas under a flow of 70 sccm (sccm stands for standard cubic centimeter per minute) with a trace of oxygen, and it was maintained for 2 h before ramping the temperature back to 25 °C at a rate of 5 deg $\cdot$ min^{-1}. The morphology of the as-synthesized nanowire was examined with a scanning electron microscope (Hitachi S-4800SEM). Transparent Sb-doped SnO_2 nanowire EDL FET arrays gated by microporous SiO_2-based solid electrolyte were fabricated on a glass substrate at room temperature. i) A 4-μm-thick microporous SiO_2 film was deposited on an ITO glass substrate which had been cleaned with acetone, alcohol, and high purity water sequentially and also by plasma-enhanced chemical vapour deposition (PECVD) using SiH_4 and O_2 as the reactive gases under flow rates of 5 sccm and 18 sccm respectively. The deposition pressure, work power, and deposited time were 25 Pa, 100 W, and 1 h, respectively. ii) A single SnO_2 nanowire was transferred onto the SiO_2/ITO/glass substrate as an active channel layer. iii) The TEM nickel grid mask was placed and fixed on the single nanowire under an optical microscopy. iv) Highly conductive ITO source/drain electrode films each with a thickness of 100 nm were deposited by dc sputtering in pure argon ambient at 0.5 Pa, the channel length and width were 15 μm and 100 nm respectively. v) Finally, the TEM nickel grid mask was removed from its position slightly. The structural characterization of the microporous SiO_2 was investigated by field emission SEM, the electrical characteristics of the nanowire transistors were measured with a Keithley 4200 semiconductor parameter analyzer at room temperature in the dark with a relative humidity of 60%. The capacitance–frequency measurement was performed using a WK 6500B precision impedance analyzer.

3. Results and discussion

The mean diameter of a Sb-doped SnO_2 nanowire is 100 nm. Nanowires separated from growth substrate are dipped into alcoholic solution, and then dispersed by using ultrasonic waves for 2 min. Fill the dropper with alcoholic solution containing nanowires, and then carefully squeeze the drops onto the microporous SiO_2/ITO/glass substrate shown in Fig. 1(a). The remaining SnO_2 nanowires are used as the channel of FETs after the alcohol has been evaporated in a few minutes, and SnO_2 nanowire draws up tightly on the substrate due to the electrostatic force between the substrate and nanowire. Figure 1(d) shows a sample holder consisting of magnets and iron sheets which can generate an external magnetic field. Under the magnetic field, the bar orientation of the TEM nickel grid is restricted into the direction parallel to the magnetic wire. A TEM nickel grid is located above the SnO_2 nanowire with its bar orientation vertical to the length direction of the SnO_2 nanowire. Then the ITO source/drain electrodes are deposited by RF sputtering shown in Fig. 1(b). Figure 1(c) shows an SEM image of the Sb-doped SnO_2 nanowire bridged between two ITO source–drain electrode transistors. The channel length of the transistor is estimated to be 15 μm. The entire process of device fabrication is simple and efficient compared with the gold microwire mask method which has been reported by our group.[17]

Figure 2(a) shows a low-magnification cross-section SEM image of microporous SiO_2 dielectric film deposited on ITO/glass substrate at room temperature. The thickness of the SiO_2 gate dielectric is estimated to be 4 μm. From a high-magnification cross-section SiO_2 dielectric film SEM image in the inset of Fig. 2(a), microporous SiO_2 with nanocolumn-like morphology is observed. The RF electric field between the top and bottom electrodes is very conducible to the formation of nanocolumn arrays. Microporous SiO_2 was deposited using SiH_4 and O_2 as a reactive gas in the PECVD process. Simultaneously, hydrogen dissociated from SiH_4 enters the microporous SiO_2 film, thereby inducing some mobile protons in the SiO_2 layer,[18] as the bare proton cannot exist in SiO_2 film steadily, it is often associated with a bridging oxygen atom to form a three coordinate oxygen centre (Si–OH^+–Si).[19] As shown in Fig. 3(a), the proton moves from one bridging oxygen atom to another along the external electric field direction, which is described as "a sequence of hops".

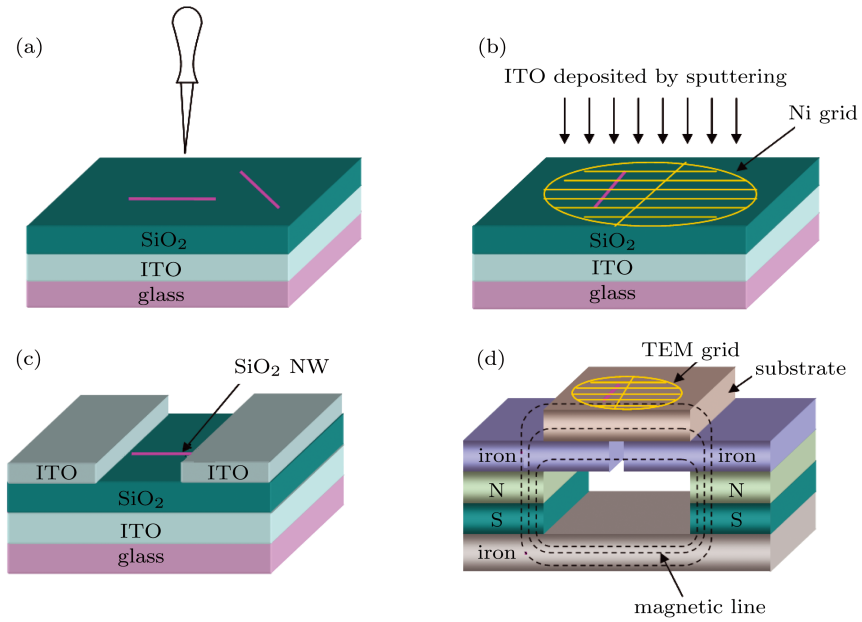


Fig. 1. (colour online) (a) Transfer individual SnO_2 nanowire from growth substrate onto the microporous SiO_2/ITO/glass substrate; (b) ITO source/drain electrodes deposited by RF sputtering and with a nickel grid shadow mask; (c) schematic image of the as-fabricated individual SnO_2 nanowire transistor with bottom-gate figure; (d) schematic image of the designed sample holder with a nickel grid attracted by the magnetic force.

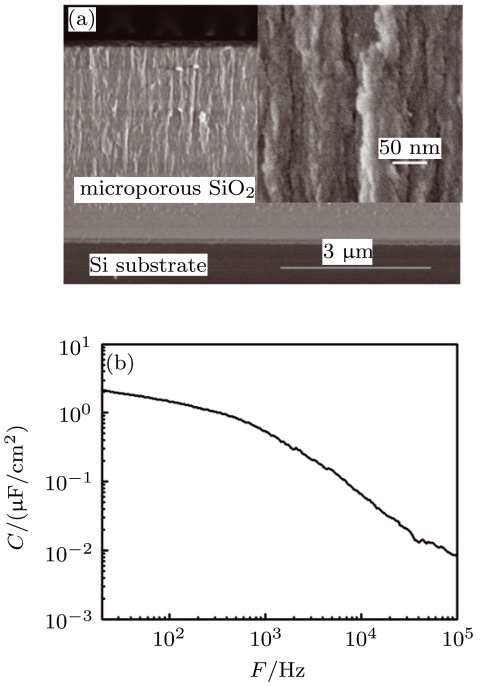


Fig. 2. (colour online) (a) Cross-sectional SEM image of microporous SiO_2 dielectric film deposited at room temperature by the PECVD method with inset showing an HR-SEM image of microporous SiO_2 dielectric. (b) Variation of specific capacitance with frequency in a range from 20 Hz to 100 kHz for a 4-μm-thick microporous SiO_2 film.

So the operation mechanism of SnO_2-based EDL FETs can be described as follows: when a positive gate voltage is applied, a proton moves to a thin boundary layer at the SiO_2/SnO_2 nanowire channel interface. At the same time, electrons accumulate near the interface in the channel due to the combination of the external gate bias and proton-induced image. The said EDL layer between the gate dielectric and channel is formed which plays an important role in optimizing the transistor performance in Fig. 3(b). The EDL formation process of SnO_2-based FET is similar to that in organic transistor gated by ionic liquids or solid-state electrolytes.[20] Frequency-dependent capacitance of the microporous SiO_2 electrolyte gate dielectric with a wide frequency range of 20 kHz–100 kHz using a SnO_2 nanowire/SiO_2/ITO sandwich test structure is shown in Fig. 2(b) which further proves that an EDL layer is formed at the interface. The electrode area is 1.5×10^{-3} cm^2. The capacitance increases as frequency decreases and reaches a peak value of 2.14 μF/cm^2 at 20 Hz. The capacitance value was measured to be 8.18 nF/cm^2 at 100 kHz. The capacitance at 100 kHz is more than two orders of magnitude smaller than that at 20 Hz which indicates that the SiO_2 specific capacitance is strongly dependent on frequency. Comparatively, a 150-nm thick layer of thermally grown dense SiO_2 has a capacitance of 20 nF/cm^2, and is only weakly dependent on frequency. This large EDL gate capacitance results in an ultralow operating voltage of 1 V and an ultrahigh current output of 1 μA. The relationship between

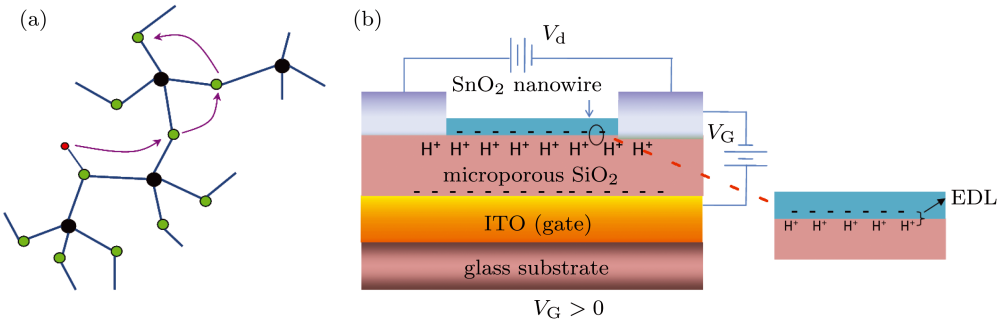


Fig. 3. (colour online) (a) Proton H^+ hopping mechanism in microporous SiO_2. (b) The schematic diagram of EDL formation.

microporous SiO_2 and frequency is consistent with that of ion gel dielectrics. The main contributions to the capacitance at low frequency were interpreted to be the response of the EDL formed at the SiO_2/oxide semiconductor interface. At a low frequency, the mobile ions have enough time to accumulate at the gate dielectric/electrode interface, leading to a cancellation of the electric field in the bulk and the formation of EDL. At a high frequency, the majority of ions in the bulk drift in response to the electric field that persists in the bulk, only a few ions can accumulate at the interface. Thus it becomes an electronically-insulating ionically-conducting dielectric. In our ultralow-voltage-operated SnO_2 nanowire FETs, the figure of merit is embodied in cost reduction, low power consumption, and mechanical flexibility.

Figure 4(a) shows the typical output characteristic I_{ds}–V_{ds} curves of Sb-doped SnO_2 nanowire EDL FETs at V_{gs} increasing from 0.1 V to 0.8 V in steps of 0.1 V. It is easier to form a Schottky contact between undoped SnO_2 nanowire and ITO source/drain electrodes. The doping of Sb atoms in the SnO_2 nanowire shifts the Fermi band downwards, and thus reduces the height of the barrier, resulting in more opportunities for electrons to travel through the depletion region, and making it easier to form Ohmic contact between the SnO_2 nanowire and the ITO source/drain electrodes. The drain current (I_{ds}) increases linearly with the increase of drain voltage (V_{ds}) at low V_{ds}, which further indicates that low-resistance Ohmic contact is formed between the SnO_2 nanowire and the ITO source/drain electrodes, and at a high drain voltage, saturation behaviour is clearly observed, indicating that the Fermi level in the channel is effectively controlled by the gate and drain bias. A high saturation current (1 μA) is obtained under the bias conditions of V_{ds} = 0.5 V and V_{gs} = 0.8 V, which shows that the FETs are promising for low-voltage and/or large on-current application. These devices each exhibit a clear pinchoff, saturation behaviour at high V_{ds}, and excellent linear behaviour at low V_{ds}, demonstrating that neither a charge-trapping effect nor chemical doping occurs in channel layer. Figure 4(b) shows the relative transfer characteristic $(I_{ds})^{1/2}$–V_{gs} curves of the FETs with V_{gs} sweeping from −0.7 V to 1.0 V and back at the V_{ds} = 1.0 V and in relative logarithmic scale. An anticlockwise hysteresis with a very small threshold voltage shift of 0.1 V is observed with a sweep rate of 12.5 mV/s. The V_{th} shift is due to the combination of ion migration in microporous SiO_2 and trapping effects. A proton density of $1.2 \times 10^{12}/cm^2$ is estimated by the equation of $N = V_{th}C_i/e$, where V_{th} is the threshold voltage shift in the transfer characteristics plot. The relatively small hysteresis window is due mainly to the huge gate specific capacitance (2.14 μF/cm^2) relating to the EDL effect. It indicates that the SnO_2 nanowire is free of traps and surface defects which shows the sample holder is extremely suited for nanowire transistor fabrication. The subthreshold slope S is estimated to be as small as 140 mV/decade, which shows that the transistor is easier to switch over to an off-state. The current on/off ratio is 2×10^4. A threshold voltage (V_{th} = 0.1 V) is calculated from the x-axis intercept of $(I_{ds})^{1/2}$–V_g plot in Fig. 4(b), indicating that the Sb-doped SnO_2 nanowire transistors are operating in an enhanced mode. The field-effect mobility (μ) of the device in the saturation operation regime ($V_{ds} > V_{gs} - V_{th}$) is estimated by the following equation:

$$I_{ds} = \left(\frac{\mu C}{2L^2}\right)(V_{gs} - V_{th})^2,$$

where L = 15 μm is the channel length, the electrolyte gate capacitance per unit length can be estimated from $C_g = C/L = 2\pi\varepsilon_0\varepsilon_r/\ln(1 + 2L_D/d)$, where ε_r = 2 is the dielectric constant of the elec-

trolyte medium, ε_0 is the permittivity of free space, and $d = 100$ nm is the diameter of the nanowire. The Debye length ($L_{\rm D}$) is simply defined as the typical distance required to shield the excess charge by the mobile carriers present in a material.[21] We assume the thickness of the EDL (1.0 nm) to be the Debye length according to the definition of the $L_{\rm D}$. Hence, the $L_{\rm D}$ is estimated to be 1.0 nm. Based on this model, the field effect electron mobility is estimated to be 54.43 $\rm cm^2/V\cdot s$, this mobility value is slightly larger than that of other oxide semiconductor-based transistors with traditional compact gate dielectrics.[22] The large mobility is attributed to high carrier density in the channel which is caused mainly by the huge EDL capacitance.

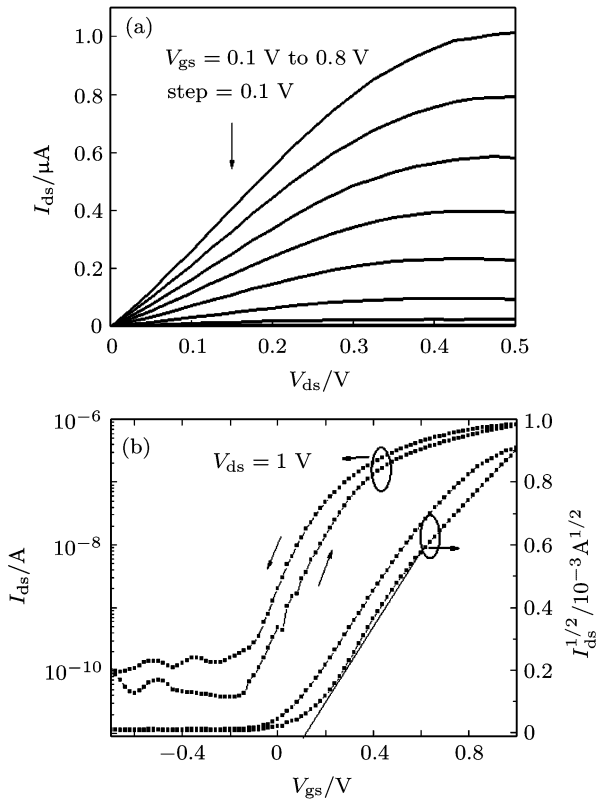


Fig. 4. (a) Output characteristic $I_{\rm ds}$–$V_{\rm ds}$ curves of the electric double-layer SnO_2 nanowire transistors with $V_{\rm gs}$ = 0.1 to 0.8 V in steps of 0.1 V increasing from bottom to top. (b) Transfer characteristic $I_{\rm ds}$–$V_{\rm gs}$ curves of the same device at $V_{\rm ds}$ = 1.0 V. The curves are displayed in logarithmic scales (left curve) and square root scales (right curve).

4. Conclusion

In this paper, room-temperature deposited 4-μm-thick microporous proton-conducting SiO_2 dielectric films each have a huge gate specific capacitance of 2.14 $\mu\rm F/cm^2$ due to the EDL effect. Battery drivable low-voltage (1 V) SnO_2 nanowire transistors gated by such a gate dielectric film are fabricated at room temperature. The threshold voltage ($V_{\rm th}$), field-effect mobility, current on/off ration, and subthreshold gate voltage swing (S) are estimated to be 0.1 V, 54.43 $\rm cm^2/V\cdot s$, 2×10^4, and 140 mV/decade respectively. This synthesis technique of SnO_2 nanowire transistors is simple and consumes low energy. Such ultralow-voltage EDL SnO_2 nanowire transistors gated by microporous SiO_2 dielectric are promising for one-battery-powered portable "see-through" sensor applications.

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