Rapid Communication

Vertical assembly of carbon nanotubes for via interconnects*

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The via interconnects are key components in ultra-large scale integrated circuits (ULSI). This paper deals with a new method to create single-walled carbon nanotubes (SWNTs) via interconnects using alternating dielectrophoresis (DEP). Carbon nanotubes are vertically assembled in the microscale via-holes successfully at room temperature under ambient condition. The electrical evaluation of the SWNT vias reveals that our DEP assembly technique is highly reliable and the success rate of assembly can be as high as 90%. We also propose and test possible approaches to reducing the contact resistance between CNT vias and metal electrodes.

Keywords: carbon nanotube, via interconnects, dielectrophoresis, electrical properties, contact resistance

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1. Introduction

As the complementary metal–oxide semiconductor (CMOS) devices scale down into the nanometer for high performances, Cu interconnects face several severe problems:[1−3] (i) the resistivity rises rapidly as the width of interconnects is reduced into nanoscale, owing to the increased interface and surface scattering effects; (ii) the enhanced electromigration failure effects in nanoscale threaten the interconnects' reliability. Therefore, currently there is a pressing need to seek alternatives beyond copper interconnects.[1,4]

Carbon nanotubes (CNTs), as one-dimensional conductors, have unique physical properties. The electron mean-free path can be of the order of micrometers, in contrast to 40 nm in bulk copper.[5] The current density can be higher than 10^9 A/cm^2,[6] two to three orders of magnitude larger than that of copper. In addition, the thermal conductivity of CNT can reach as high as 6000 W/mK.[7] The most outstanding feature is that single-walled carbon nanotubes (SWNTs) are immune to electromigration even at high current densities.[8] Recently, some theoretical work has shown that CNTs can be an ideal substitution for copper interconnects.[1,4]

Despite these promises, there have existed only a few experimental studies on CNT interconnects. Among these studies, most were coplanar interconnects.[1,4] So far, few attempts have been made to fabricate the vertical interconnects, referred to herein as via interconnects. The main challenges may come from the following aspects: how we can realize the three-dimensional (3D) vertical assembly of CNTs, how we can filter the favoured metallic carbon nanotubes for interconnects and how we can develop assembly techniques compatible to the CMOS process.

In this paper, we demonstrate a simple, effective, and reproducible method to prepare the SWNT via interconnects, which is based on dielectrophoresis (DEP). DEP is a natural phenomenon in which a force

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is exerted on a dielectric particle when it is exposed to a non-uniform alternating electric field.[9] The DEP technique has been successfully used for preparing oriented nanotubes[10−13] and separating metallic nanotubes from semiconducting nanotubes.[14] Here using the DEP technique, carbon nanotubes can be successfully vertically assembled within the via-holes from dimethylformamide (DMF) suspension at room temperature under ambient conditions. The electrical measurements of the fabricated SWNT vias indicate that our assembly technique is effective and the success rate of assembly can be as high as 90%. We also propose and test possible approaches to reducing the contact resistance between CNT vias and metal electrodes.

2. Experiment

The SWNT bundles were vertically assembled within a via-hole using the DEP method. The principle is as follows: first, the alternating electric field induces electric dipole moments in the nanotubes in DMF suspension. The dipole moments then interact with the inhomogeneous electric field and produce a DEP force. The nanotubes thus move along the electric field gradient and be aligned within the via-holes.[10] The DEP force is given by $F_{\mathrm{DEP}} = \Lambda\varepsilon_{\mathrm{p}}\,\mathrm{Re}\,\{k_{\mathrm{f}}(\omega)\}|\nabla|E||$, where Λ is the factor dependent on geometry, ε_{p} is the relative permittivity and k_{f} is the Clausius–Mossotti factor relating to both geometry and frequency.[15,16] Using the DEP method, theoretically, metallic nanotubes can be selectively deposited from the nanotube DMF suspension to via-holes, leaving the semiconducting nanotubes in suspension. The metallic nanotubes are preferred for interconnect application.

Figure 1(a) shows a 3D configuration of the DEP assembly setup. A small drop of SWNT/DMF solution was first cast onto the chip containing via-holes. Then an ac voltage ($V_{\mathrm{p-p}}$) of 10 V at 3 MHz was applied using a function generator for 5 min. The drop had been gently blown off the chip surface by a stream of nitrogen gas before the generator was switched off. This assembly process was carried out at room temperature under ambient conditions.

Via holes were fabricated using standard microfabrication techniques. Both the 3D structure and the process flow are schematically shown in Figs. 2(a)–2(c). The lower Au/Ti metal electrodes (100 nm/10 nm) were determined using optical lithography and the lift-off process on the 300-nm SiO_2/p-doped Si wafer, followed by the deposition and patterning of the dielectric layer (SiO_2). This dielectric layer acted as an insulation barrier, deposited by plasma enhanced chemical vapour deposition (PECVD) (see Fig. 2(b)). The thickness of the SiO_2 was 1 μm. After the upper Au/Ti electrodes (100 nm/10 nm) were determined, the via-holes were made by etching through the dielectric layer, reaching down to the lower electrodes. Figure 2(d) shows an example of arrays with via holes. The via-hole is square shaped with side length ranging from 5 μm to 20 μm (Fig. 2(e)).

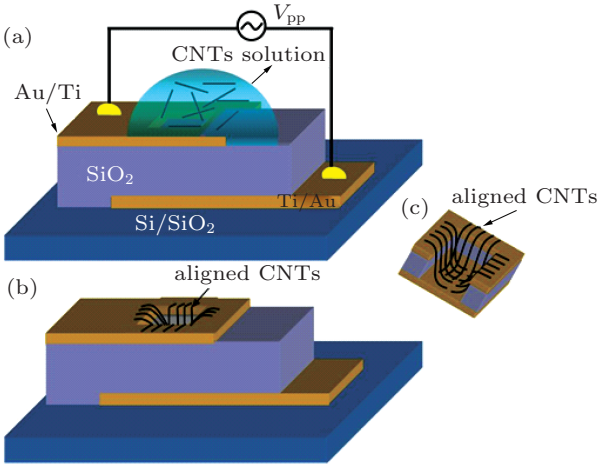


Fig. 1. (colour online) Schematic plot of the DEP assembly process for SWNT via interconnects, showing (a) 3D configuration of the DEP assembly setup, (b) aligned nanotubes after the DEP process, and (c) SWNT bundles within the via-hole.

The SWNTs were grown by DC arc discharge technique. The diameters of the nanotube bundles were 10 nm–50 nm and the length of the nanotubes varied from 1 μm to 5 μm. The nanotubes were ultrasonically dispersed in N, N-dimethylformamide (DFM) solution. The concentration of the solution used was about 10 μg/ml.

The field-emission scanning electron microscope (FE-SEM) images of SWNT vias were taken by FEI NanoSEM 430. Electrical measurements were carried out using HP 4156B precision semiconductor parameter analyzer. Raman spectra of SWNT bundles were collected by a micro-Raman spectrometer with an excitation energy of 2.41 eV (514 nm). *In-situ* deposition of SWNTs by Au nanoparticles (NPs) was achieved by an electroless deposition method. The details were reported in our previous work.[17]

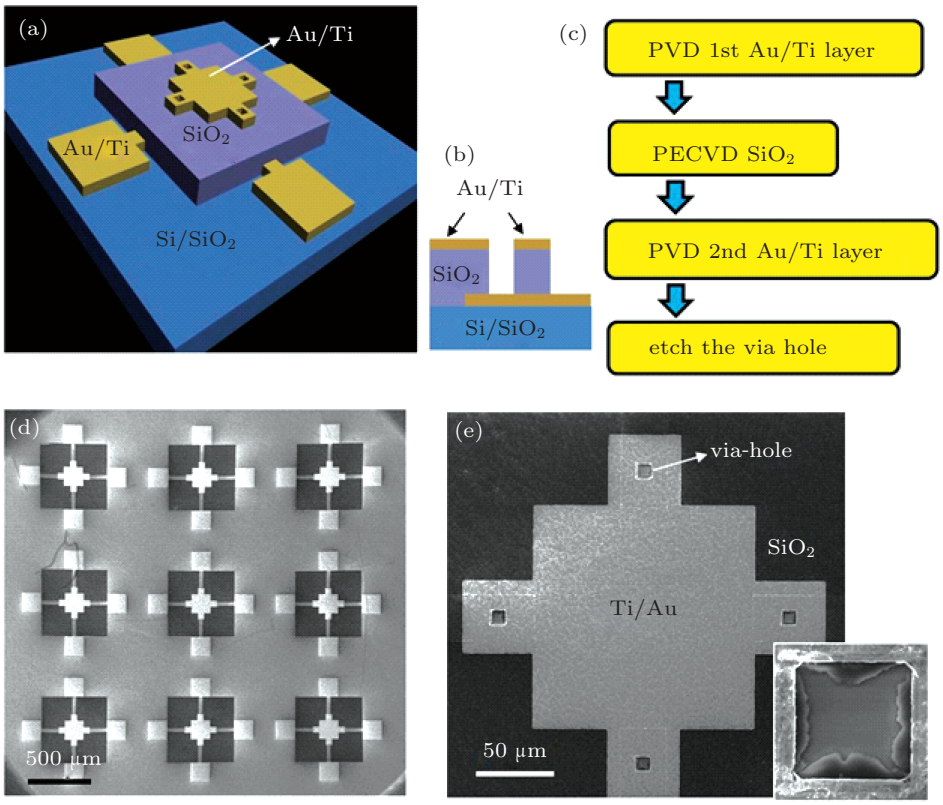


Fig. 2. (colour online) Schematics of via-holes, showing (a) 3D configuration of the via-hole structure, (b) cross section of a via-hole, (c) process flow of the via-hole fabrication, (d) SEM images of the via-hole arrays, and (e) zoomed-in SEM image of via-holes, with inset exhibiting the SEM image of one square hole.

3. Results and discussion

Carbon nanotubes are successfully vertically assembled within the microscale via-holes using the DEP method. This method is effective and the success rate of assembly can reach as high as 90%. Figure 3 shows the SEM images of SWNT bundles in the via-holes. The tube bundles, connecting the upper and lower Au/Ti electrodes, are aligned along the direction of the electric field. Nearly all these SWNT bundles are perpendicular to the edges of the upper-layer electrode (Figs. 3(a)–3(c)). The alignment condition of the SWNTs shows strong dependences on frequency (f) and magnitude of an applied ac voltage ($V_{\rm pp}$). More tube bundles are arranged in the direction parallel to each other if we apply higher f and $V_{\rm pp}$ (see supplementary information, Figs. S1 and S2 at the end of this paper). Furthermore, at high frequencies (or $V_{\rm pp}$), the end of the nanotube bundles exhibits tree-like structures (nanotrees, Fig. 3(d)). All of these tube nanotrees were firmly bonded to the electrode surface by van der Waals forces,[14,18] indicating that the structure of SWNT via interconnects is stable and reliable.

The density of the aligned SWNTs is also highly dependent on $V_{\rm pp}$, f, and time for assembly (t). The density of the tubes can be controlled by tuning $V_{\rm pp}$, f, and t (See supplementary information, Figs. S1–S3 at the end of this paper). The density of the nanotubes can be much higher. The nanotubes do not form an electric contact with Au in the presence of a DMF solution during the DEP process.[16] The reasons may be as follows: i) although there are abundant COOH groups on the ends or sidewalls of the acid treated SWNTs, the COOH groups have no affinity to the Au electrode surfaces;[13,19] ii) there exists an adsorbed layer of DMF between the nanotubes and the gold surface, which will prevent an electrical contact from forming in liquid environments.[13] Our previous work indicated that the tube density can be further improved by using higher concentration SWNTs in DMF solution.[20]

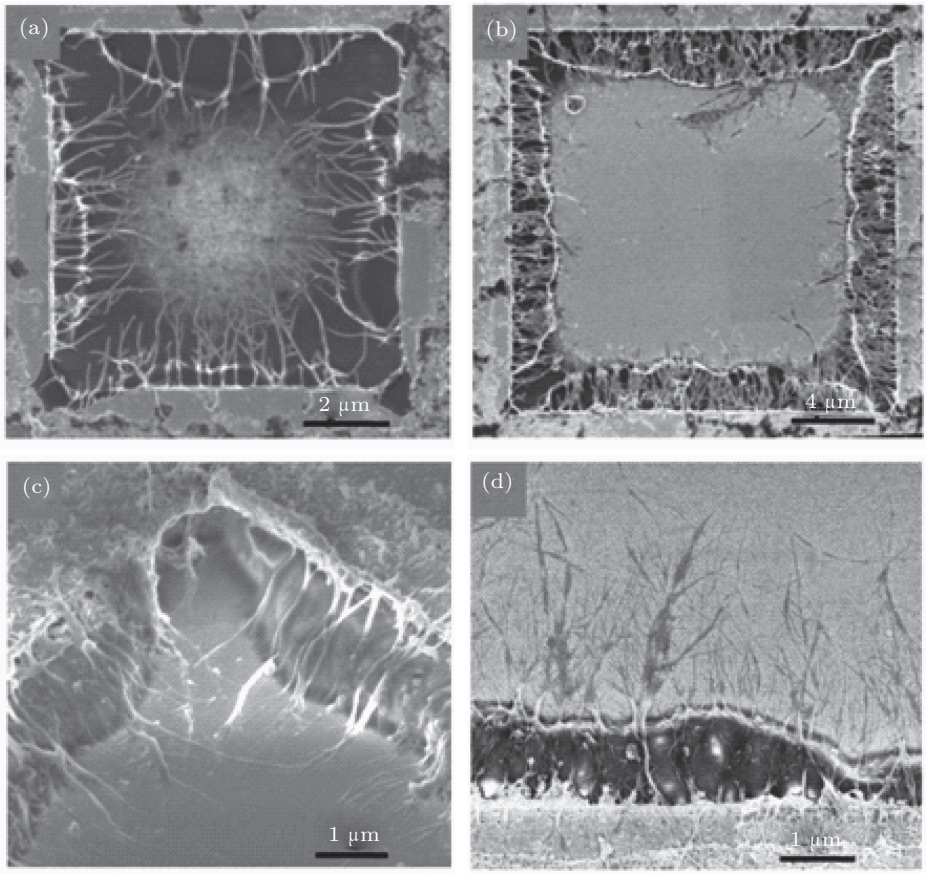


Fig. 3. SEM images of SWNT via interconnects with sizes of (a) 10 μm and (b) 20 μm. (c) Bird's eye-view of the corner of a via-hole; (d) SWNT nanotrees structure on the surface of the lower electrode.

The electrical evaluation of the SWNT vias reveals that our DEP assembly technique is highly reproducible, which is a prerequisite for creating via interconnects for an electronic circuit. The electrical transport measurements were performed in an HP probe station in an ambient environment. Out of the 65 samples that we have tested, we find that in $\sim 90\%$ cases the upper- and lower-electrodes were connected by SWNT bundles, confirmed by both SEM and I–V measurements. Figure 4(a) shows the typical current–voltage (I–V) characteristics of the SWNT vias with various sizes (5, 10, and 20 μm)). At low bias voltages, the I–V curves are nearly linear for all tube via interconnects, indicating that the contact between the SWNT bundles and Au/Ti electrodes is Ohmic. The currents of the SWNT vias depend on the sizes of the via-holes. It is found consistently that higher currents (lower resistances) for SWNT vias were obtained when we assembled SWNTs in larger vias. As an example, the current of the SWNT via with a size of 20 μm×20 μm is ~ 15 times as large as that of via with 5 μm×5 μm (Fig. 4(a)). This phenomenon is easy to understand, since we have more parallel SWNTs connecting the two electrodes in larger via holes, they inevitably have lower resistance than that in smaller via holes.

Figure 4(b) shows the statistical distribution of 58 resistance measurements of SWNT vias with various sizes. We can see that the values of two-terminal resistances (R_{2t}) are in a range of 500 Ω–100 MΩ for SWNT vias. Among these samples, approximately 80% of these R_{2t} values lie in a range of 1 kΩ–100 kΩ. Note that here we used a two-terminal configuration, i.e., the contact resistance (R_c) should be included, $R_{2t} = 2R_c + R_{SWNTs}$. As is well known, the SWNTs prepared by the arc-discharge technique usually have fewer structure defects, and hence a longer mean free path (> 1 μm) and a lower resistivity.[4,21] The metallic SWNT has two conducting channels, thus its minimum resistance is $R_Q/2$, where R_Q is resistance quantum ($R_Q = h/2e^2 = 12.9$ kΩ).[22] Since hundreds of SWNTs were connected in parallel here within the via-holes, their total resistance should be less than one hundredth of the resistance quantum. In our SWNT

vias, however, only 9% of samples have resistances (R_{2t}) much less than resistance quantum (R_Q). For other samples, the R_{2t} has the same order of magnitude as R_Q. Therefore, it clearly indicated that the contact resistance (R_c) contributes to the majority of two-terminal resistance.

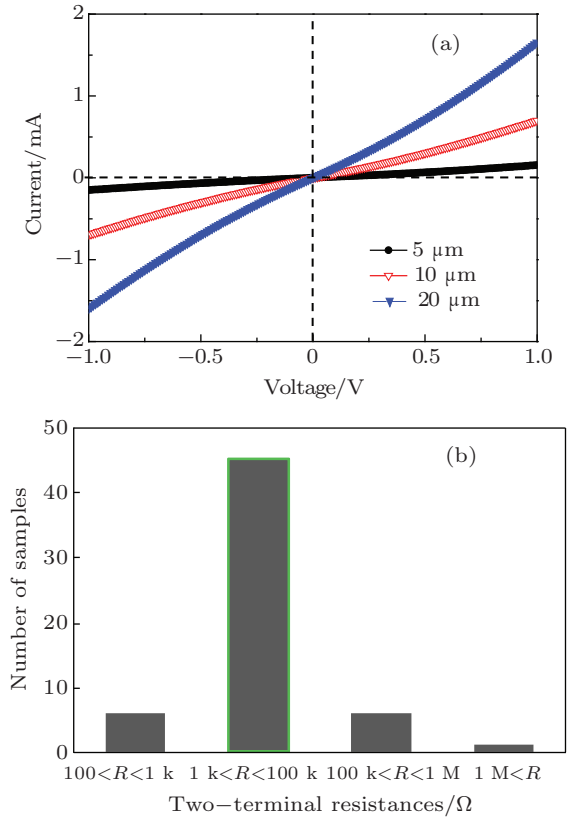


Fig. 4. (colour online) Electric properties of SWNT via interconnects: (a) I–V curves of different via-holes with sizes of 5 μm, 10 μm, and 20 μm; (b) statistical distribution of two-terminal resistances of SWNT via interconnects.

The question arises why the contact resistance is so large. The reasons are as follows: a) the configuration of our SWNT vias is a nanotube-on-metal one, as illustrated in Fig. 1(c), which usually has a high contact resistance (in MΩ range);[23] b) unlike the reported low-resistance conditions (e.g. Ti–C) resulting from covalent bonds,[24] there are no chemical bonds between the nanotubes and gold surface besides the van der Waals interactions;[23] c) some semiconducting nanotubes still exist in via-bundles assembled by DEP, introducing a Schottky barrier at the CNT-metal electrode interface, and hence increasing the contact resistance.[11,20] It was predicated that the semiconducting SWNTs can be completely removed by the DEP process if all nanotubes in the DMF solutionare dispersed as individual tubes.[14,25] The SWNTs used here, however, are bundles which contain the semiconducting components. This can be confirmed from the Raman spectrum (Fig. 5). The metallic and semiconducting tubes can be distinguished by the tangential G modes in the Raman spectrum.[14,25] Figure 5 shows that the G-band feature for SWNTs has two peaks, one is at 1594 cm^{-1} (G^+) and the other at 1570 cm^{-1} (G^-). The lineshape of G^- feature is extremely sensitive to the electronic structure. The lineshape in Fig. 5 exhibits a Lorentzian-type, revealing that the via-bundles contain semiconducting tubes.

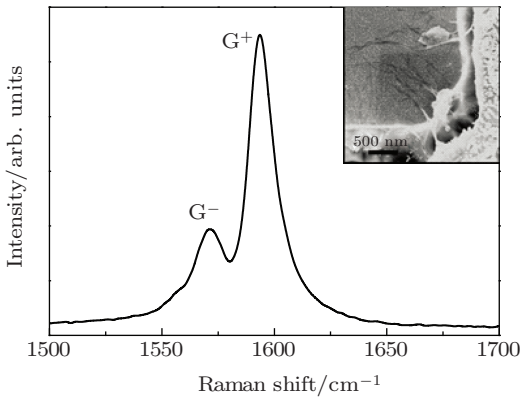


Fig. 5. G-band Raman spectrum of SWNT bundles within a via-hole.

How can we reduce the contact resistance in our SWNT vias? Here we demonstrated two methods, including annealing and *in-situ* electroless deposition of gold nanoparticles. After annealing in an Ar atmosphere at 400 °C for 20 minutes, the currents of the SWNT vias are increased by up to three orders of magnitude (Fig. 6(a)). This may be due to two reasons: (I) improved gold-nanotube interface, and (II) desorption of residual organic solvents from the tube surface.[23] We can also reduce the contact resistance by an *in-situ* electroless deposition process. As shown in Figs. 6(c) and 6(d), both the ends and sidewalls of the tubes are coated by gold nanoparticles (NPs). Similarly, the contact resistance can be reduced by 1–3 orders of magnitude (Fig. 6(b)). After annealing or electroless metal deposition, however, the resistance is still of the order of the quantum of resistance (tens of kilohms). This is a very interesting phenomenon which needs further investigation.

Before addressing this question, we first compare a set of data. Table 1 shows some contact resistance data previously reported for carbon nanotubes. The electrode material, configuration of the device, and electric properties of the samples are summarized in

this table. From Table 1, we can find that the contact resistances for all carbon nanotube devices are of the same orders of magnitude as those of our interconnect samples, i.e., in the 0.5 kΩ–30 kΩ range. It indicates that the contact resistances are dependent only on the electrode material regardless of the shape, the configuration, and the subsequent processing of the nanotube device. Lim *et al.*[26] have confirmed that the resistance is affected mainly by two physical parameters of the metal: the wettability and the work function. This is why the resistance is still of the order of the resistance quantum even after annealing or electroless metal deposition.

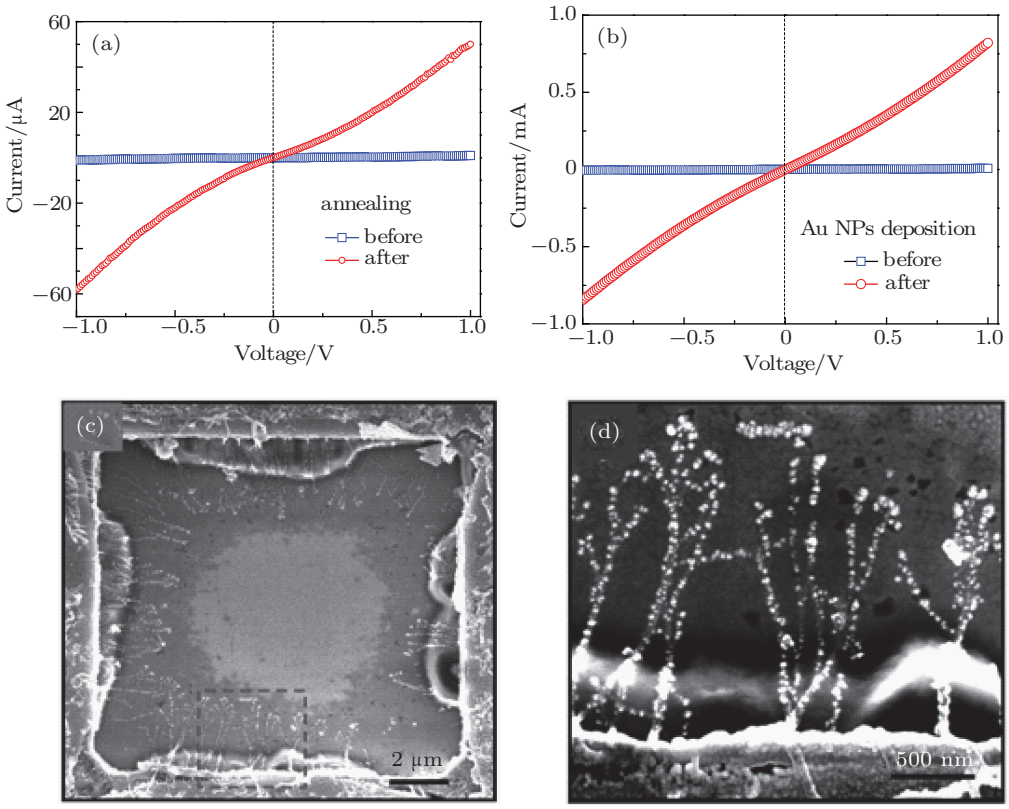


Fig. 6. (colour online) *I*–*V* curves of SWNT via interconnects before and after (a) annealing; (b) electroless gold nanoparticles (NPs) deposition; (c) SEM image of SWNT via interconnects after gold NPs deposition; (d) zoomed-in SEM image of SWNT bundle with gold NPs.

Table 1. Contact resistances for some carbon nanotube devices.

Nanotube	Electrode material	Configuration of device	Contact resistance	Reference
MWNT bundles	Au	end-contacted	1.8 kΩ	[26]
SWNT thin films	Au	side-contacted	10 kΩ	[27]
Individual MWNT soldering with Au	Au	side-contacted	2 Ω–15 Ω	[28]
Individual SWNT after rapid annealing	Au/Ti	side-contacted	0.5 kΩ–50 kΩ	[29]
SWNT bundles after annealing or Au deposition	Au/Ti	side-contacted	10 kΩ–30 kΩ*	this work

* These resistances are measured by the two-terminal method.

A qualitative explanation can be given by comparing a set of reported data. Table 1 shows some contact resistance data previously reported for carbon nanotubes with different electrode materials, device configurations, and electric properties. From Table 1, we find that the contact resistances for all carbon nanotube devices are of the same orders of magnitude as those of our interconnect samples, i.e., in 0.5 kΩ–30 kΩ range. We may infer that the contact resistances have intrinsic values dependent only on electrode materials regardless of forms, configuration, and subsequent processing of nanotube devices. As evidence of this view, Lim *et al.*[26] have shown that the resistance is mainly affected mainly by two physical parameters of the metal: the wettability and work function. Therefore we can understand why the resistances of our

SWNT vias are still of the order of resistance quantum after annealing or electroless metal deposition.

4. Conclusion

We presented a promising method to create SWNT via interconnects using the ac DEP technique. The carbon nanotubes can be successfully vertically assembled in the microscale via-holes. The electrical evaluation of the SWNT vias reveals that our DEP assembly technique is highly reliable and the success rate of assembly can reach as high as 90%. We studied the electrical properties of SWNT vias and found their two-terminal resistances to be in the range of 1 kΩ–100 kΩ. Some possible reasons are given to explain such high resistances. The contact resistance can be reduced by 1−3 orders of magnitude by either annealing or *in-situ* electrodeless deposition of gold nanoparticles. Our DEP technique is compatible with conventional CMOS process, which may become a recipe for SWNT interconnects in ULSI ultra-large scale integrated circuits. Both the assembly technique and the possible reasons for high contact resistances in our SWNT vias will arouse theoretical and engineering interest.

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Supplementary information

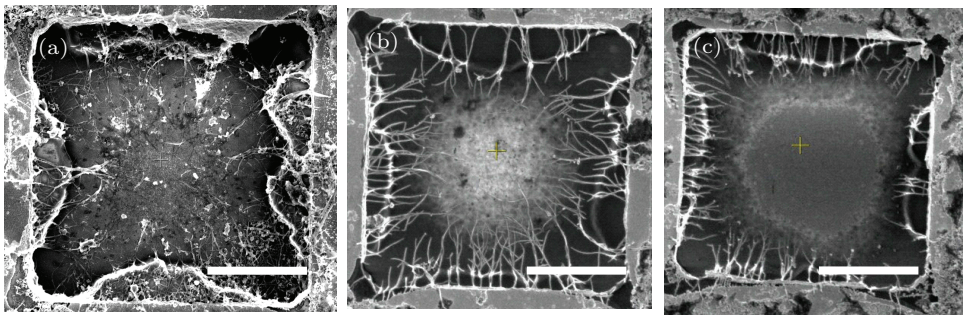


Fig. S1. SEM images of aligned nanotube bundles assembled with frequencies of (a) 10 kHz; (b) 3 MHz; (c) 20 MHz; scale bar: 4 μm, (V_{pp} = 10 V, 5 min.).

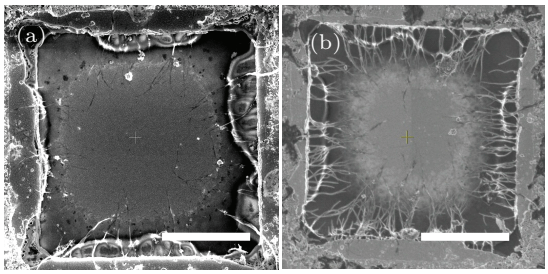


Fig. S2. SEM images of aligned nanotube bundles assembled at (a) 3 V; (b) 10 V; scale bar: 4 μm (5 min, 3 MHz.).

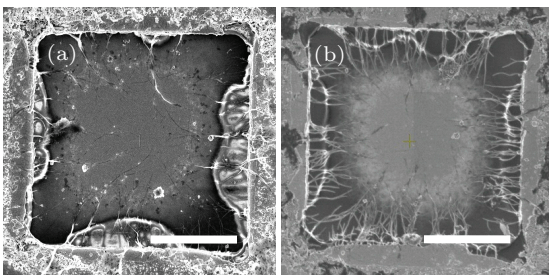


Fig. S3. SEM images of aligned nanotube bundles assembled for times of (a) 1 min and (b) 5 min; scale bar 4 μm (V_{pp} = 10 V, 3 MHz).

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