Investigation of a 4H–SiC metal–insulation–semiconductor structure with an Al_2O_3/SiO_2 stacked dielectric*

Tang Xiao-Yan(汤晓燕)†, Song Qing-Wen(宋庆文), Zhang Yu-Ming(张玉明), Zhang Yi-Men(张义门), Jia Ren-Xu(贾仁需), Lü Hong-Liang(吕红亮), and Wang Yue-Hu(王悦湖)

School Microelectronics, Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, Xi'an 710071, *China*

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Atomic layer deposited (ALD) Al_2O_3/dry-oxidized ultrathin SiO_2 films as a high-k gate dielectric grown on 8° off-axis 4H–SiC (0001) epitaxial wafers are investigated in this paper. The metal–insulation–semiconductor (MIS) capacitors, respectively with different gate dielectric stacks (Al_2O_3/SiO_2, Al_2O_3, and SiO_2) are fabricated and compared with each other. The I–V measurements show that the Al_2O_3/SiO_2 stack has a high breakdown field ($\geq$12 MV/cm) comparable to SiO_2, and a relatively low gate leakage current of 1×10^{-7} A/cm^2 at an electric field of 4 MV/cm comparable to Al_2O_3. The 1-MHz high frequency C–V measurements exhibit that the Al_2O_3/SiO_2 stack has a smaller positive flat-band voltage shift and hysteresis voltage, indicating a less effective charge and slow-trap density near the interface.

Keywords: 4H–SiC, Al_2O_3, high-k dielectric

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1. Introduction

Metal–oxide–semiconductor field-effect transistors (MOSFETs) based on 4H–SiC have been intensively investigated for high power device applications because of the excellent physical and electronic properties of 4H–SiC.[1−3] However, the relatively low dielectric constant of the native oxide SiO_2(3.9) compared with that of SiC(9.8) can contribute to severe oxide breakdown and reliability issues,[4] because an electric field as high as approximately 2.5 times is imposed on the oxide rather than on the SiC. Recently, extensive investigations have focused on searching for a suitable alternative high-k dielectric[5−8] to reduce the electric field in the gate dielectric layer. However, one challenge exists in applying high-k gate dielectric materials, in which the low band offset between the high-k and SiC material results in a high leakage current. To solve this problem, an ultrathin SiO_2 interfacial layer is usually introduced between the high-k dielectric and SiC.[9] Aluminium oxide (Al_2O_3) is attractive as an alternative gate dielectric because it simultaneously presents a dielectric constant of 9 and a large band offset to 4H–SiC in comparison with other high-k materials.[9]

In the present paper, atomic layer deposition (ALD) high-k gate dielectric Al_2O_3 and SiO_2 stacked films on the 8° off-axis 4H–SiC (0001) epitaxial wafers are studied. The ultrathin SiO_2 interfacial layer is formed by dry-oxygen oxidation. The electrical characteristics are investigated by current voltage (I–V), and high frequency (HF) capacitance voltage (C–V) measurements. Results exhibit that the Al_2O_3/SiO_2 stack has attractive characteristics, which are a low leakage current, high breakdown voltage, small positive flat-band voltage shift, and a very small hysteresis voltage, compared with the single Al_2O_3 or SiO_2 stack on 4H–SiC.

2. Device structure and fabricating process

Figure 1 shows the schematics of the fabricated 4H–SiC metal–oxide–semiconductor (MOS) capacitors respectively with SiO_2, Al_2O_3, and Al_2O_3/SiO_2 stacks. An n-type 10-μm epilayer doped by nitrogen with a concentration of 3.0×10^{15} cm^{-3} was grown on

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†Corresponding author. E-mail: xytang@mail.xidian.edu.cn

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each N-type 4H–SiC [0001] 8° off-axis wafer, which is used to fabricate the MOS capacitor. The wafers were cleaned with the conventional Radio Corporation of America (RCA) clean procedure, and then dipped into a diluted hydrofluoric acid solution to remove native oxide from the SiC surface. After cleaning, samples

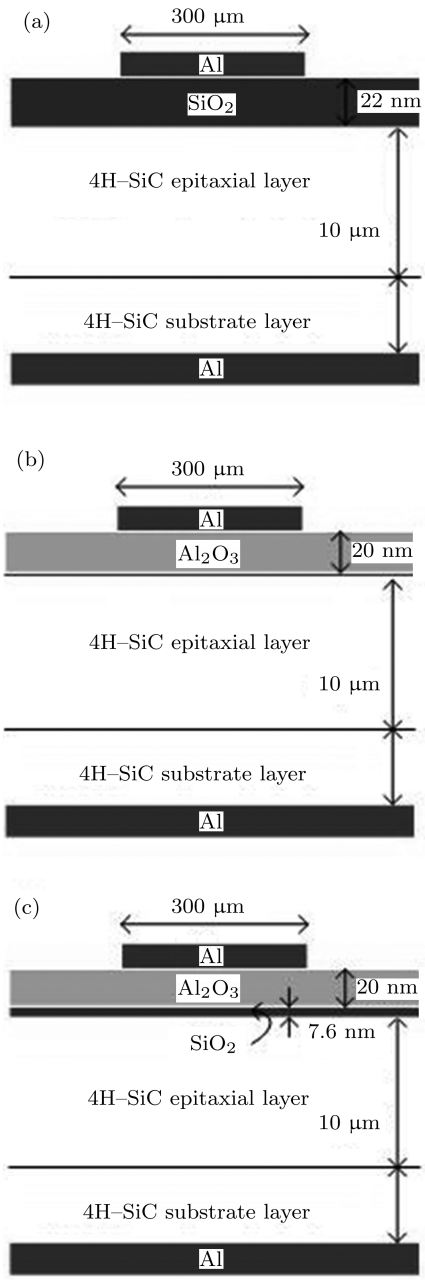


Fig. 1. The schematic plot of the 4H–SiC metal–oxide–semiconductor capacitors respectively with SiO_2 (a), Al_2O_3 (b), and Al_2O_3/SiO_2 stacks (c).

No. 1 and No. 2 were thermally oxidized in dry O_2 ambient at 1050 °C for 60 min and 180 min respectively, to grow SiO_2 with thicknesses of 7.6 nm and 22 nm measured by spectroscopic ellipsometry (SE). Samples No. 1 and No. 2 were then annealed in N_2 for 60 min. The 20-nm thick Al_2O_3 layers were grown on SiO_2/4H–SiC (sample No. 1) and 4H–SiC (sample No. 3) using the ALD technique. Subsequently, a 200-nm thick aluminum (Al) layer was deposited on all three samples by magnetron sputter and then patterned for gate electrodes to fabricate MOS capacitors whose areas were equal to 7.07×10^{-4} cm^{-2}. The atomic force microscope (AFM) measurements of the surface morphology images for the dry-oxygen oxidized SiO_2 and the ALD Al_2O_3 deposited on the SiO_2/4H–SiC epitaxial layer are shown in Fig. 2. The root-mean-square (RMS) values of surface roughness are 0.97 nm and 0.91 nm over a 10-μm^2 area, respectively, which reveals that the Al_2O_3 deposited on the dry-oxygen oxidized SiO_2/4H–SiC has better step coverage and thickness uniformity. Electrical characterization was performed by 1-MHz HF C–V and the I–V measurements using a computer controlled HP4156 B with a bias sweep rate of 0.1 V/s, and Keithley 4200 semiconductor parameter analyzer. All measurements were implemented at room temperature.

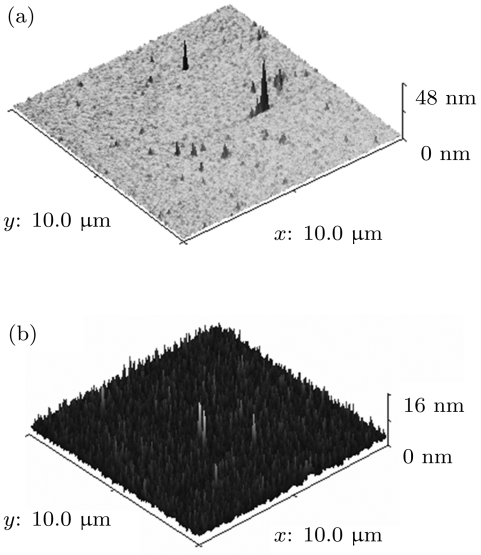


Fig. 2. Images of surface morphology from AFM for the dry-oxygen oxidation SiO_2 (a) and the ALD Al_2O_3 deposited on a SiO_2/4H–SiC epitaxial layer (b).

3. Results and discussion

Figure 3 shows the HF C–V characteristics of the MOS capacitors for these samples, normalized to different oxide capacitances (C_{ox}). The gate voltage was swept from accumulation to depletion. The electrical parameters extracted from the HF C–V curve including C_{ox}, flat-band voltage shift (ΔV_{FB}), effective charge density (Q_{eff}), and interface state density (D_{it}) are presented in Table 1. The positive ΔV_{FB} is found by comparing the experimental and theoretical results,

and $Q_{\rm eff}$ is deduced from $\Delta V_{\rm FB}$ and $C_{\rm ox}$. It is observed that the Al_2O_3/SiO_2 stack has the smallest value of $-Q_{\rm eff}$. $D_{\rm it}$ at 0.26 eV below the conduction band (flat-band condition) is calculated using Terman's method.

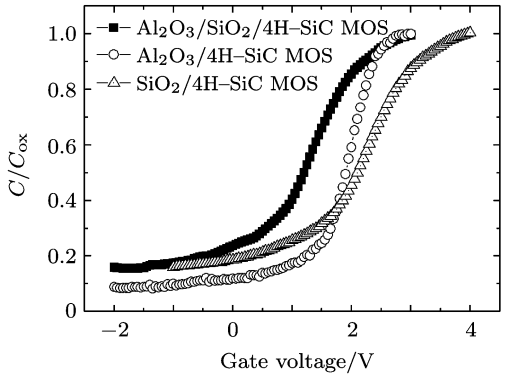


Fig. 3. High frequency C–V characteristics of the 4H–SiC MOS capacitors for the samples.

Samples No. 1 and No. 3 have almost the same values of $D_{\rm it}$, whereas sample No. 2 has the largest value of $D_{\rm it}$ because of carbon accumulation produced by oxidation process at the interface.[10]

To further investigate the hysteresis characteristic, bi-directional high-frequency (1 MHz) C–V measurements on three samples were carried out. The gate voltage was swept from accumulation to depletion and then back to accumulation. The hysteresis voltage ($\Delta V_{\rm h}$) and slow-trap density ($Q_{\rm st}$) near the interface obtained from the bi-directional C–V are presented in Table 1. Sample No. 1 has the smallest hysteresis voltage and the lowest slow-trap density of all three samples.

The above results indicate that the Al_2O_3/SiO_2/4H–SiC MOS structure possesses the best interface quality. The improvement of interface quality can be explained as follows: the SiO_2 interfacial layer between the Al_2O_3 and 4H–SiC can also effectively prevent the oxygen in the Al_2O_3 from diffusing into the interface, thereby lowering the amount of SiC_xO_y at the interface.

Table 1. Parameters extracted from the HF C–V curve.

Sample	$C_{\rm ox}$/pF	$\Delta V_{\rm FB}$/V	$Q_{\rm eff}/(10^{11}/{\rm cm}^2)$	$D_{\rm it}$ at 0.26 eV/$(10^{12}$ cm$^{-2}\cdot$ eV$^{-1})$	$\Delta V_{\rm h}$/mV	$Q_{\rm st}/(10^{18}/{\rm cm}^3)$
No. 1	104	0.477	–4.39	8.80	48	0.15
No. 2	115	1.14	–11.6	11.8	60	2.05
No. 3	208	0.94	–17.3	9.15	77	4.74

The current density–electric field curves (J–E) of 4H–SiC MOS structures respectively with Al_2O_3/SiO_2, SiO_2, and Al_2O_3 as gate dielectrics are shown in Fig. 4, which is transformed from I–V curves. The electric field is approximated by $(V_{\rm G} - V_{\rm FB})/{\rm EOT}$, where V_G and EOT are the gate voltage and the equivalent oxide thickness with respect to SiO_2. The EOT values of the single Al_2O_3 and the Al_2O_3/SiO_2 stack are 8.67 nm and 16.3 nm, respectively.

The current density in the Al_2O_3/SiO_2/4H–SiC structure is very low and is nearly constant (10^{-8} A/cm^2–10^{-7} A/cm^2) in the whole voltage range, similar to that of the SiO_2/4H–SiC structure. But a hard breakdown is observed for the SiO_2/4H–SiC MOS at an electric field of 4.0 MV/cm, while the Al_2O_3/SiO_2/4H–SiC MOS does not break down in the whole voltage range ($0 \sim +20$ V), whose breakdown field is higher than 12 MV/cm. The current in the Al_2O_3 /4H–SiC MOS structure is about 3×10^{-4} A/cm^2 at 4.0 MV/cm, about three orders of magnitude higher than that of Al_2O_3/SiO_2 stack. The high leakage current of the Al_2O_3/4H–SiC MOS may be due to the low conduction band offset at the Al_2O_3/4H–SiC interface compared with SiO_2/4H–SiC interface.[11]

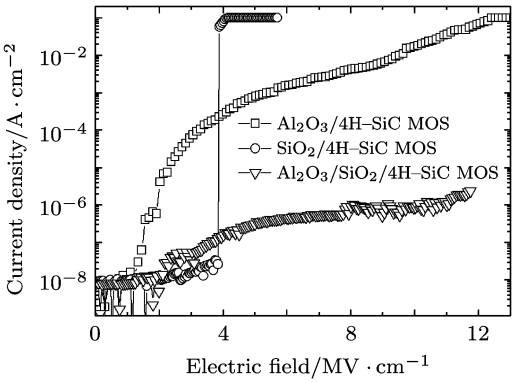


Fig. 4. The J–E characteristics of 4H–SiC MOS structures respectively with Al_2O_3/SiO_2, SiO_2, and Al_2O_3 as gate dielectrics.

4. Conclusions

To reduce the high leakage current of high-k gate dielectric material, an ultrathin SiO_2 layer is introduced between Al_2O_3 and SiC materials. In this pa-

per, 4H–SiC MIS structures with Al_2O_3/SiO_2, SiO_2, and Al_2O_3 gate dielectrics respectively, formed by ALD and dry-oxygen oxidation process are systematically investigated. AFM characterization indicates the ALD Al_2O_3 deposited on ultrathin SiO_2/4H–SiC epitaxial layer has better step coverage and thickness uniformity. The 1-MHz HF C–V measurements exhibit that the Al_2O_3/SiO_2 stack has an obviously smaller positive flat-band voltage shift and hysteresis voltage, indicating less effective charge and slow-trap density near the interface. The interface state density of the Al_2O_3/SiO_2 stack is slightly smaller than that of the other two. The I–V characteristics reveal that the Al_2O_3/SiO_2 stack has a higher breakdown field ($\geq$12 MV/cm), and relatively low gate leakage current of 1×10^{-7} A/cm^2 at an electric field of 4.0 MV/cm. These results indicate that the Al_2O_3/SiO_2/4H–SiC MOS structure possesses a better interface quality and lower leakage current. These ideal characteristics imply the great potential of the ALD Al_2O_3/ultrathin SiO_2 stacks for SiC high power device applications.

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