Chip design of a 5.8-GHz fractional-N frequency synthesizer with a tunable G_m–C loop filter

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This paper proposes a novel G_m–C loop filter instead of a conventional passive loop filter used in a phase-locked loop. The innovative advantage of the proposed architecture is tunable loop filter bandwidth and hence the process variations of passive elements of resistance R and capacitance C can be overcome and the chip area is greatly reduced. Furthermore, the MASH 1-1-1 sigma-delta ($\Sigma\Delta$) modulator is adopted for performing the fractional division number and hence improves the phase noise as well. Measured results show that the locked phase noise is -114.1 dBc/Hz with lower G_m–C bandwidth and -111.7 dBm/C with higher G_m–C bandwidth at 1 MHz offset from carrier of 5.68 GHz. Including pads and built-in G_m–C filter, the chip area of the proposed frequency synthesizer is 1.06 mm^2. The output power is -8.69 dBm at 5.68 GHz and consumes 56 mW with an off-chip buffer from 1.8-V supply voltage.

Keywords: G_m–C loop filter, phase-locked loop, PLL, voltage-controlled oscillator (VCO)

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1. Introduction

Recently, there has been much interest in seeking the improvement of loop filters, which dominate the performance of PLLs.[1−3] In Ref. [1], the authors added a transconductor after the loop filter and simulated results proved that the locking time is shorter than the traditional type II PLL. Reference [2] presented a novel loop filter which utilized a switched resistor instead of a large resistor for fast locking time and low phase noise. Reference [3] adopted a locking detector which detects the locking situation of a PLL. Before locking, the loop bandwidth should be wider so that performs fast locking time. After locking, the loop bandwidth should be narrower, which will then achieve low phase noise performance. The approach proposed in Refs. [1]–[3], however, suffers from process, voltage, and temperature (PVT) variations. Their conventional passive 4-th order PLL is shown in Fig. 1. For reducing the phase noise, a passive loop filter is often built in the chip, but the process variation may cause deviation of the loop bandwidth and is shown in Fig. 2, in which the $\omega_{\mathrm{C,opt}}$ is the optimum loop bandwidth for the phase noise. From Fig. 2(b), the loop bandwidth is chosen to be higher than $\omega_{\mathrm{C,opt}}$, but higher bandwidth will pass more phase-and-frequency-detector (PFD) referred noise to the output of the PLL, and hence contributes to the out-of-band phase noise. Contrarily, in Fig. 2(c), while the bandwidth is set to be lower than $\omega_{\mathrm{C,opt}}$, more voltage-controlled oscillator (VCO) phase noise will be included into the PLL, and thus excess phase noise appears in the loop band. Hence, a solution is needed to solve those problems.

This paper presents a fractional-N frequency synthesizer with a tunable loop filter composed of passive and active components. The main idea is to solve the problems of process variation after manufacturing and utilize the characteristics of adjusting of a G_m cell being a part of loop filter in PLL. In addition, integer-N frequency synthesizers suffer from essential tradeoffs between loop bandwidth and channel spacing and allow alternative tradeoffs among PLL design constraints for phase noise, locking time, and reference spurs,[4] hence we add the MASH 1-1-1 $\Sigma\Delta$ modulator to resolve these problems and perform the fractional-N frequency synthesizer.

The rest of this paper is organized as follows. Section 2 describes the circuit blocks of the frequency synthesizer. The measured results are given in Section 3 and, in Section 4, a conclusion is provided.

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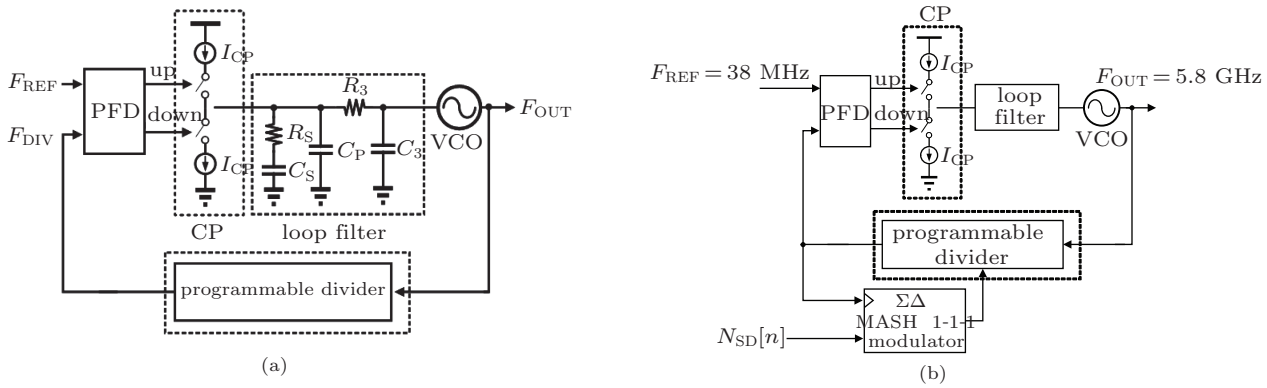


Fig. 1. Fractional-N PLL (a), conventional passive 4th order PLL (b), the proposed G_m–C filter with MASH 1-1-1 modulator.

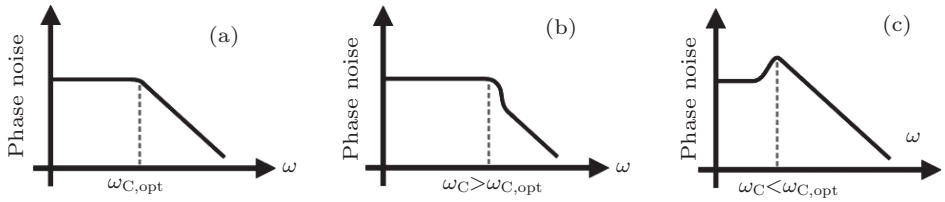


Fig. 2. Noise performance of (a) optimization of bandwidth, (b) bandwidth is greater than optimization of bandwidth, (c) bandwidth is smaller than optimization of bandwidth.

2. System block diagram

2.1. Frequency synthesizer architecture

The proposed fractional-N frequency synthesizer mainly consists of a PFD, a charge pump (CP), a tunable G_m–C loop filter, and a VCO in the feed–forward path and a frequency divider which is controlled by MASH 1-1-1 ΣΔ modulator in the feedback path as shown in Fig. 3. The ΣΔ modulator generates a pseudo-random bit sequence to switch the frequency divider's division ratio so that the desired fractional division ratio is obtained. The PFD detects the phase error between the reference signal F_{REF} and the feedback signal F_{DIV}. The digital output signals of the PFD determine whether the CP circuit charges or discharges the tunable G_m–C loop filter, which linearly control the oscillation frequency of the VCO connected to the frequency divider which is adjustable to determine the output frequency, F_{DIV}.

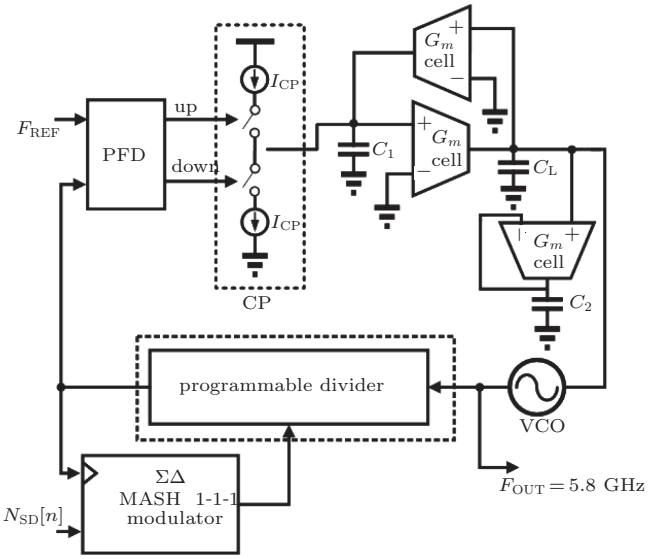


Fig. 3. Proposed fractional-N frequency synthesizer.

2.2. Voltage-controlled oscillator (VCO)

The cross-coupled VCO in a complementary metal–oxide semiconductor (CMOS) has attracted considerable interest due to its easy start-up and good phase noise characteristics.[5] On the other hand, the Colpitts configuration features superior phase noise because the noise current from active devices is injected into the tank during the minima of the tank voltage when the impulse sensitivity is low. Unfortunately, the conventional Colpitts VCO suffers from poor start-up characteristics, i.e., higher power consumption is needed to ensure reliable start-up in the presence of standard PVT variations. The capacitor feedback network also reduces its tuning range. Finally, there is a lack of the differential outputs needed to suppress common-mode coupling. In or-

der to resolve the poor start-up characteristics, and improve the phase noise, the current-switching differential Colpitts VCO is adopted as shown in Fig. 4(a) in which the phases of gate voltages of M_1 and M_2 are as the same as the phases of drain voltages of M_2 and M_1, respectively. Connecting them together will have the effect of a G_m-boosting scheme. However, the differential Colpitts VCOs only consist of N-MOS or P-MOS, so large gate–source voltage of M_1 and M_2 are necessary to obtain better properties. Figure 4(b) is the schematic plot of the proposed balanced VCO, modified from Ref. [6]. The proposed balanced VCO consists of two single-ended LC-tanks and two pairs of complementary NP metal–oxide semiconductor field-effect transistors (NP-MOSFETs) so that their gate–source voltages become small. To enhance the start-up oscillation condition of the balanced Colpitts VCO, an NP-MOSFET core is chosen to reuse the dc current. Since the dc current is reused, although the proposed balanced VCO uses four MOSFETs, the consumed current still remains very small, therefore low power dissipation can be achieved.

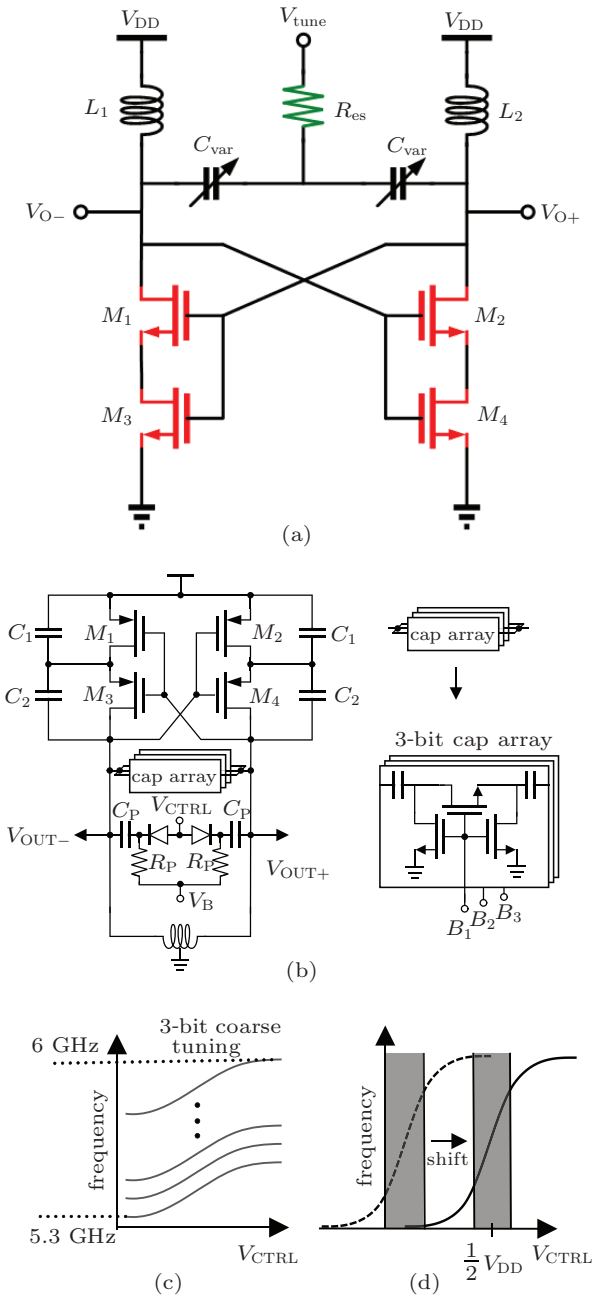


Fig. 4. (colour online) The VCO circuit: (a) typical VCO circuit, (b) proposed Colpitts VCO circuit, (c) the coarse tuning curves, (d) shifting of the VCO tuning characteristic.

The capacitor C_{var} in parallel with the inductor forms the LC-tank resonator. The accumulation-mode MOS varactors are used for tuning the VCO output frequency. The oscillation frequency is given by

$$f_o = \frac{1}{2\pi\sqrt{L_{1,2}C_{vnet}}}, \tag{1}$$

where C_{vnet} is the effective capacitance of the balanced VCO, as shown in Fig. 4(b). To have a wide tuning range and small VCO gain, a 3-bit binary weighted capacitor array is connected to the LC tank for coarse tuning, as shown in Fig. 4(b). To fully utilize the capacitance tuning range over a limited voltage range, the varactor is biased at a more linear region by applying a dc voltage to shift its operating point, as illustrated in Fig. 4(c). Finally, in order to reduce the chip area, the transformer is adopted.

2.3. G_m–C loop filter

It is well known that the loop filter is one of the most important building blocks in PLL and the circuit noise performance and locking behavior are affected by loop bandwidth. The general 3rd order passive loop filter is chosen and illustrated in Fig. 5. The inductor can be emulated by G_m cells and a capacitor. The passive

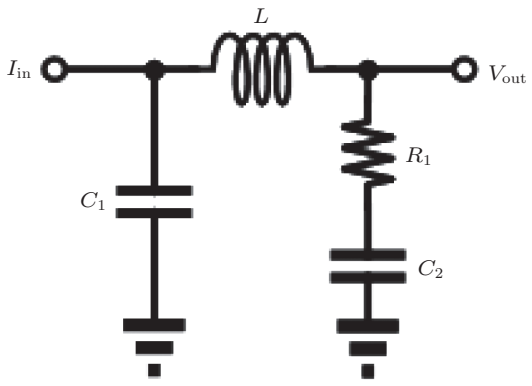


Fig. 5. Passive 3rd order loop filter circuit.

transfer function of the 3rd order loop filter is given as

$$\frac{V_{\rm out}}{I_{\rm in}} = \frac{1}{s\,(C_1+C_2)}\frac{1+sR_1C_2}{1+sR_1C_p+s^2LC_p}, \quad (2)$$

where $C_p = C_1C_2/(C_1+C_2)$.

After some arrangements, the transfer function of the 3rd order loop filter is extracted as

$$H(s) = \frac{K_{\rm LP}(1+s/\omega_z)}{s[1+s(1/\omega_pQ_p)]+s^2(1/\omega_p^2)}, \quad (3)$$

where $K_{\rm LP}$ is the DC gain of the loop filter that can be expressed as

$$K_{\rm LP} = K\frac{N}{K_{\rm V}I_{\rm CP}}, \quad (4)$$

where K is the gain of the function, N is the division ratio, $K_{\rm V}$ and $I_{\rm CP}$ are the gain of VCO and the current of charge pump, respectively. Comparing both transfer functions of Eqs. (2) and (3), dominate pole, ω_p, can be evaluated as

$$\omega_p = \sqrt{\frac{1}{LC_p}}. \quad (5)$$

The main idea is to control the dominate pole ω_p. From Eq. (5), the ω_p is a function of the inductor. Practically, a G_m–C filter can be realized by using a practical gyrator with active elements such as op-amps or transconductors. A gyrator with transconductors is preferable in high-frequency filters. The grounded gyrator consists of two transconductors: one with an inverting input and one with a non-inverting input, as shown in Fig. 6. An ideal gyrator is obtained if the transconductances are equal or $g_{m1} = g_{m2}$. Actually, it is possible that $g_{m1} \neq g_{m2}$ due to either transistor or design mismatch. A grounded gyrator can be used for grounded inductor simulation. The implementation of the floating gyrator is obtained by using two grounded gyrators. The input impedance at one port is proportional to the reciprocal of the terminating impedance at the other port. The relationship between the input and output terminals can be expressed as

$$Z_{\rm in} = \frac{1}{g_{m1}g_{m2}Z_L} = \frac{sC_L}{g_{m1}g_{m2}}, \quad (6)$$

where g_{m1} and g_{m2} are the transconductances, $Z_{\rm in}$ is the input impedance, and Z_L is the terminating impedance. If Z_L is the impedance of a capacitor C_L, then an equivalent inductance $L_{\rm eq} = C_L/g_{m1}g_{m2}$ is obtained. The circuit in Fig. 6 is thus equivalent to an inductor. Therefore the inductor in the loop filter is replaced by G_m cells and a capacitor. Its inductance can be defined as

$$L = \frac{C}{g_m^2}. \quad (7)$$

Equation (7) implies that the inductor can be changed by adjusting the g_m value. The total G_m–C filter is shown in Fig. 7 and its schematic plot of a G_m cell is depicted in Fig. 8,[7] where I_{C3} is ajustable to tune the g_m value, and $R_{\rm eq}$ is the source degenerative resistor used to improve the linearity.

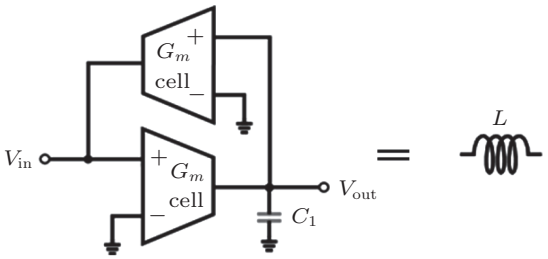


Fig. 6. The schematic plot of a G_m–C inductor.

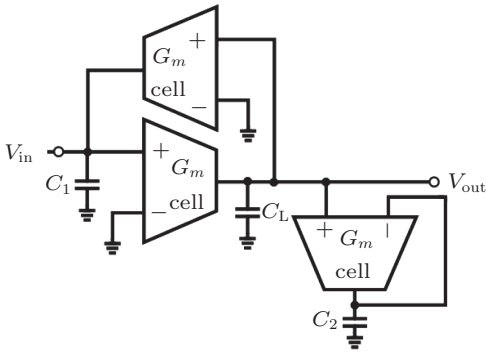


Fig. 7. The proposed G_m–C loop filter.

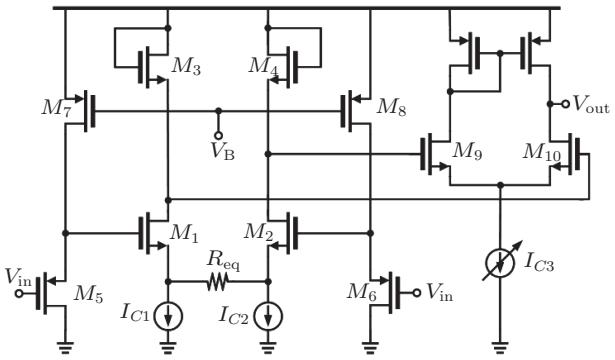


Fig. 8. A G_m–C circuit.

2.4. Multi-modulus frequency divider and modulator

Figure 9 shows the MMFD architecture, which consists of seven asynchronous divided-by-2/3 stages and logic gates.[8] The architectures of 2/3 divider and

logic gate are a true single phase clock (TSPC) circuit and a traditional logic circuit, respectively. The MMFD treats frequency division over a wide continuous range, has less time delay and can be programmable. The output frequency of the frequency synthesizer can therefore be tuned by controlling the ports from MC_1 to MC_8 and then the division number (DN) is adjusted from 256 to 511. The DN can be programmable and expressed as:

$$\mathrm{DN} = 2^8 + 2^7 * \mathrm{MC}_8 + 2^6 * \mathrm{MC}_7 + \cdots + 2^0 * \mathrm{MC}_1. \quad (8)$$

With reference to Fig. 10(a), the 2/3 divider architecture consists of the traditional reforming TSPC DFF (D flip–flop) illustrated by the circuit of Fig. 10(b), which achieves high data rate.[9] The high-speed portions (the first three divide-by-2/3 stages) of the MMFD are implemented in current mode logic (CML), while the rest are designed in static CMOS logics for low-power and robust operation. The proposed TSPC DFF circuit makes the output discharge stop when Y_1 is high during the evaluation period. The NMOS transistor M_{N4} is controlled by $\bar{Y}_I$ inserted from the output stage of the DFF. M_{N4} is turned off by Y_1 by an added inverter before the end of the recharge phase, then the discharge path for $\bar{Q}$ is cut off safely before M_{NS2} is turned on in the evaluation period.

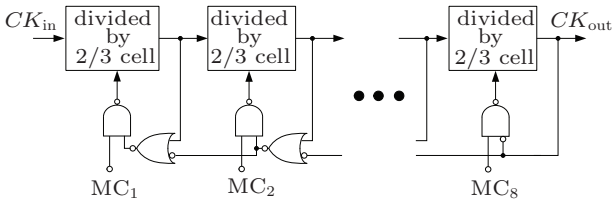


Fig. 9. Multi-modulus frequency divider.

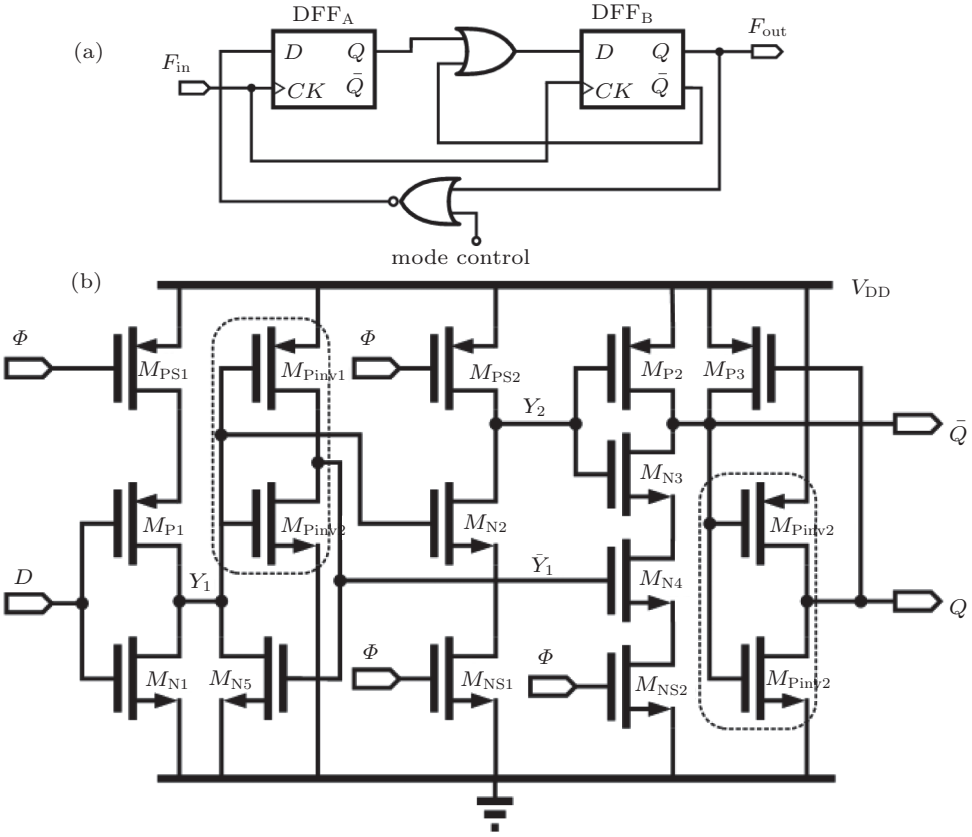


Fig. 10. A 2/3 divider (a) schematic (b) TSPC DFF circuit.

The MMFD division ratio is controlled by the MASH 1-1-1 modulator illustrated in Fig. 11. The MASH architecture is preferred in this implementation, since it is unconditionally stable, and it can accommodate a wide-range input for high resolution frequency synthesizers. An on-chip 3rd order loop filter is employed to suppress the high-pass-shaped modulation noise.

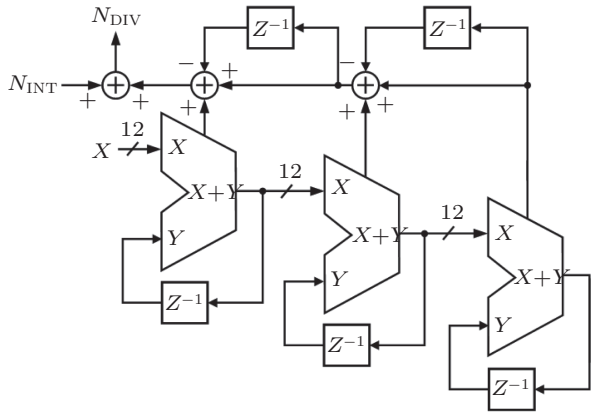


Fig. 11. A ΣΔ MASH 1-1-1 modulator architecture.

3. Measurement and discussion

The simulation results of the proposed fractional-N frequency synthesizer with a tunable G_m–C loop filter are carried out with ADS and Spectre RF simulators. In addition, the performances of the circuits are also simulated after layout and parasitic extraction by ADS and Momentum RF. The fabricated PLL chip photograph is shown in Fig. 12. The chip area including pads and an on-chip G_m–C low-pass filter occupies 1.0 mm × 1.06 mm (1.06) mm^2. A two-layer commercial printed-circuit board (PCB) FR4 glass-epoxy double-sided laminate ($\varepsilon_r = 4.4$) is used for chip testing. Measurements have been performed with an HP 8510C network analyzer, an Agilent 8975A noise figure analyzer and an Agilent E4407B spectrum analyzer.

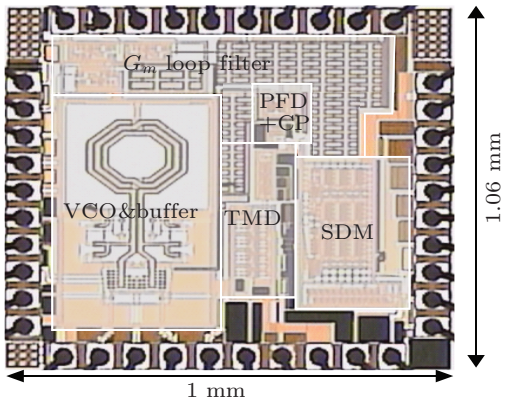


Fig. 12. (colour online) Die micrograph of the proposed frequency synthesizer with a chip area of 1.06 mm^2.

The measured results are shown from Figs. 13–15. Figure 13 shows the VCO free-running output power of −4.06 dBm at 5.67 GHz. Figure 14 shows the VCO free-running phase noise which is −116.3 dBc/Hz at 1-MHz offset from 5.67 GHz. Figure 15 shows the measured VCO tuning curves with different controlled codes varied from 000 to 111. There are eight curves in total with a frequency tuning range from 5.25 GHz to 5.75 GHz. Figure 16 shows the frequency synthesizer output spectrum, as one can see, the two small signals which locate away about 38 MHz from main tone are due to the reference clock of 38 MHz. The

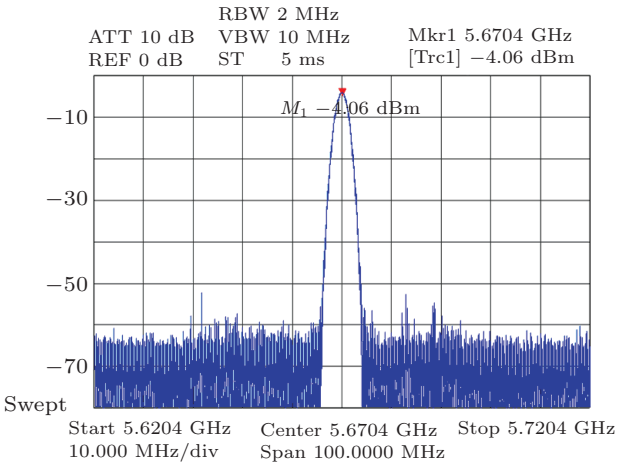


Fig. 13. (colour online) VCO free-running output spectrum.

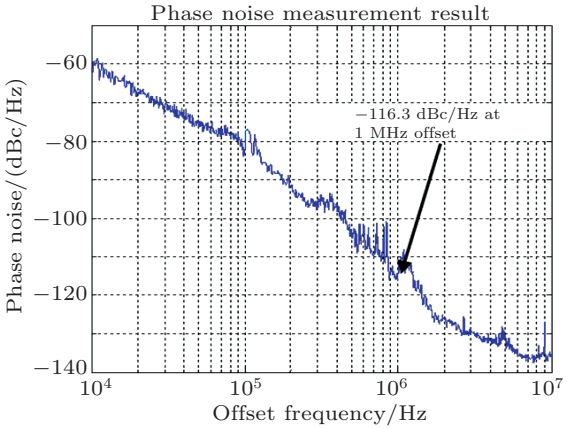


Fig. 14. (colour online) VCO free-running phase noise from 5.67 GHz.

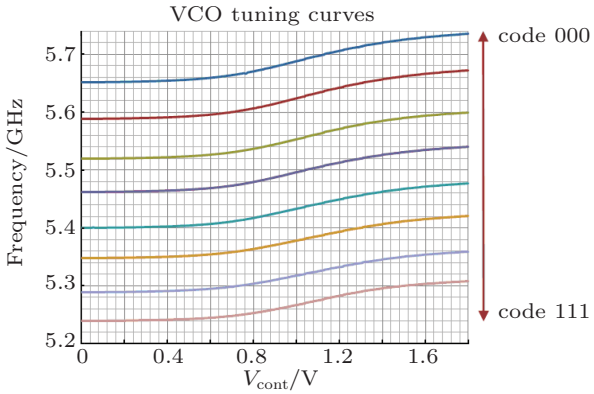


Fig. 15. (colour online) VCO tuning curves with different controlled codes varied from 000 to 111.

locked output power is about −8.69 dBm at 5.68 GHz. Figure 17 shows the locked PLL phase noise versus offset frequency with varying G_m–C loop bandwidth.

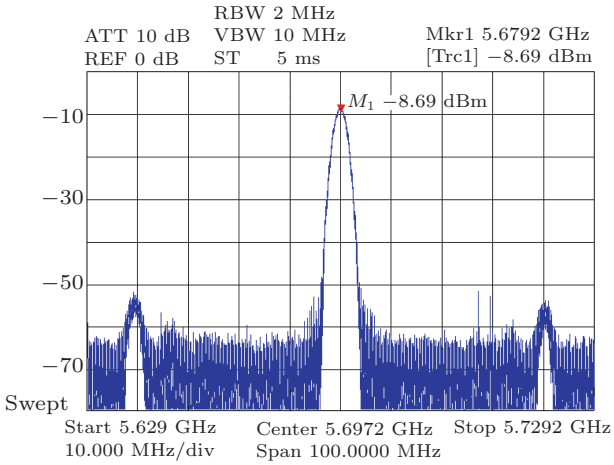


Fig. 16. (colour online) Measured output spectrum of PLL.

As a result, when the loop bandwidth goes down, the phase noise is about −114.1 dBc/Hz with lower bandwidth. On the other hand, when the loop bandwidth goes up, the phase noise becomes worse and is about −111.7 dBc/Hz. Obviously, the loop filter bandwidth affects the phase noise performance. A wider loop bandwidth causes worse phase noise.

The proposed 5.8-GHz fractional-N frequency synthesizer is implemented in a TSMC 0.18-m CMOS process. The design performance is summarized in Table 1. Measured data are close to those of post-simulation. Table 2 summarizes the measured performance in comparison with some other previously published PLL papers. Obviously, our design achieves the widest tuning range from 5.25 GHz to 5.75 GHz and the smallest chip area. Except for Ref. [9], the proposed PLL accomplishes the lowest phase noise of −1141 dBc/Hz. Comparing to Ref. [9], our chip area is 1.06 mm^2, which is much smaller than 4.8 mm^2 found in Ref. [9].

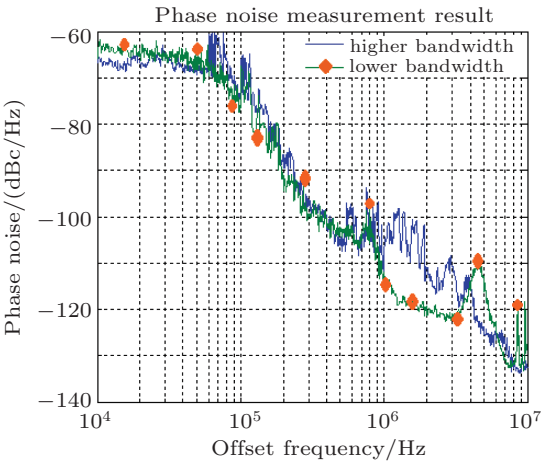


Fig. 17. (colour online) Measured locked phase noises with different loop bandwidths, −114.1 dBc/Hz as the G_m–C at lower bandwidth and −111.7 dBc/Hz as the G_m–C at higher bandwidth from the carrier frequency of 5.68 GHz.

Table 1. Summary of the proposed 5.8-GHz fractional-N frequency synthesizer with G_m–C loop filter.

	Pre-sim.	Post-sim.	Measurement
Supply voltage/V		1.8	
Power consumption with buffer/mW		45	56
VCO tuning range/GHz	6.00–6.75	5.4–6.0	5.25–5.75
VCO phase noise at 1 MHz/(dBc/Hz)	−121.6	−121.6	−116.3
PLL phase noise at 1 MHz/(dBc/Hz)	–	–	−114.1
Reference clock/MHz		38	
Chip area/mm^2		1.06	1.06

Table 2. Performance comparison of the proposed PLL with previously published papers.

Parameters	JSSC 2007[9]	TRANS 2009[10]	JSSC 2008[11]	This work
Type	fractional-N	fractional-N	hybrid	fractional-N
Process/μm	0.18	0.18	0.18	TSMC 0.18
Supply voltage/V	1.8	1.8	1.8	1.8
Tuning range/GHz	2.4	2.2–2.6	2.37–2.50	5.25–5.75
Phase noise at 1 MHz/(dBc/Hz)	−120	−105.5	−113	−114.1*
Power consumption/mW	38	22	29.6	56
Chip area/mm^2	4.8	2.25	2.08	1.06

* with lower G_m–C filter bandwidth.

4. Conclusion

A novel 5.8-GHz fractional-N frequency synthesizer with a tunable G_m–C loop filter is implemented in a TSMC 0.18-μm CMOS process. In order to achieve lower phase noise, a Colpitts VCO with a capacitor array is adopted. Furthermore the MASH 1-1-1-modulator, which is designed to perform the fractional division number can improve the phase noise as well. This new technique can adjust the loop bandwidth to optimize bandwidth, which is varied by process variation after manufacture. This synthesizer achieves −114.1 dBc/Hz phase noise with lower G_m–C bandwidth and −111.7 dBc/Hz phase noise with a higher G_m–C bandwidth at 1 MHz offset from 5.68 GHz. Including pads and the 3rd order G_m–C loop filter the chip area of the frequency synthesizer is only 1.06 mm^2. The power consumption is 56 mW from a 1.8-V supply voltage.

Acknowledgements

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