Thermal analysis of GaN laser diodes in a package structure*

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Using the finite-element method, the thermal resistances of GaN laser diode devices in a TO 56 package for both epi-up configuration and epi-down configuration are calculated. The effects of various parameters on the thermal characteristics are analysed, and the thicknesses of the AlN submount for both epi-up configuration and epi-down configuration are optimized. The obtained result provides a reference for the parameter selection of the package materials.

Keywords: laser diodes, thermal, GaN

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1. Introduction

GaN-based violet/blue laser diodes (LDs) are of significance for the applications in such as optical data storage, communication systems, and micro projectors.[1,2] For practical applications of LDs, the device reliability is indispensable. A high junction temperature will degrade the optical performances, thus cause potential device failure and reliability problems.[3−9] The improvement on thermal characteristics of GaN LD products is important for realizing reliable devices with a long life-time. The thermal resistance is defined as a most useful indicator of the thermal performance of an LD package and becomes a prime interest to package designers of high power GaN-based LDs.[10−13]

In this paper, analysis of the thermal characteristics of GaN-based LDs in the TO 56 package is carried out by using the finite-element method (FEM). The numerical results of both epi-up and epi-down configurations are obtained and the influences of various parameters on the device thermal resistance are discussed.

2. Simulation model

The following heat conduction equation is numerically solved for the analysis of the thermal characteristics of GaN LDs

$$\rho c \frac{\partial T}{\partial t} = q_v + \kappa \nabla^2 T, \tag{1}$$

where T is the temperature, ρ the density, c the specific heat, t the time, q_v the heat generation rate per unit volume, and κ the thermal conductivity, which is treated as an isotropic parameter.[14] In this work, the numerical solution is achieved by using the finite-element method (FEM).

We suppose that GaN LDs in the TO 56 package are seated on a thermoelectric cooler (TEC). For steady-state analysis, $\partial T/\partial t$ is equal to zero, the solution is independent of density and the specific heat of the material. Ideally, considering that the heat convection surface of the stem is in contact with the air, and the ambient temperature is taken as a fixed temperature of 300 K if it is not specially mentioned, the steady-state temperature distribution in the LD chip could be obtained by solving this equation.

Based on the calculation results, the value of the

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thermal resistance R of the device is derived using the following equation:

$$R = \Delta T/Q, \tag{2}$$

where ΔT is the temperature difference between the junction and the ambient, and Q is the total thermal power of the device. In GaN-based LDs, except for the active region, the heat generation in the p-cladding layer is also relatively large,[4] which often makes the maximum temperature take place in the p-cladding layer, not in the active region as in usual GaAs-based LDs.[15] However, the temperature difference between the active region and the p-cladding layer is not very large. In the following calculation of thermal resistance, we will take the maximum temperature as the value of junction temperature.

Figure 1 schematically shows a GaN LD chip mounted on an AlN submount in a TO 56 package. The AlN submount is attached to the Kovar heat sink. The submount attachment material with both an LD chip (up) and a heat think (down) is AuSn solder. The MQW LD is grown on a GaN substrate with a stripe-type waveguide. Table 1 shows the parameters used in the thermal simulation. We suppose that the GaN LD in the TO 56 package operates at $I = 100$ mA, $U = 5$ V, and the light power $P_{\text{light}} = 50$ mW. It is assumed that the heat is generated in the active region, the P-waveguide layer, the P-cladding layer, and the P-contact layer. 80% of the thermal power is uniformly distributed in the P-cladding layer and the P-contact layer, the rest of the thermal power is evenly distributed in the active region and the P-waveguide layer.

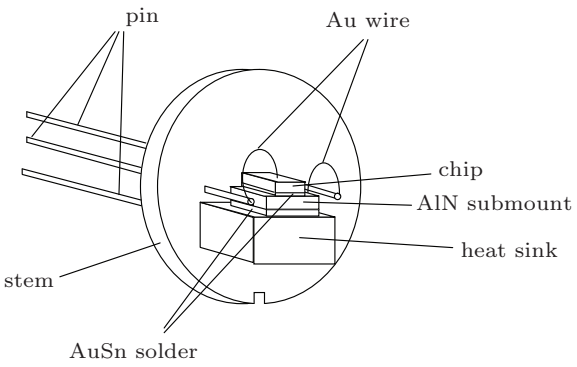


Fig. 1. Schematic diagram of a GaN-based LD in a TO 56 package.

Table 1. Material parameters in the simulation at 300 K.

	Component in the packaged structure	Material	Thermal conductivity/W·mK^{-1}
1	Stem	Kovar	46
2	Heat sink	Kovar	46
3	Solder (down)	AuSn	57
4	Submount	AlN	170
5	Solder (up)	AuSn	57
6	Substrate	GaN	130
	Buffer layer		
7	N-cladding layer	$Al_{0.08}Ga_{0.92}N$	20[3]
	N-waveguide layer	GaN 100 nm	
		$In_{0.04}Ga_{0.96}N$ 80 nm	
8	Active region	$In_{0.15}Ga_{0.85}N$/GaN MQWs	70
9	P-waveguide layer	$In_{0.04}Ga_{0.96}N$ 80 nm	
	P-EBL	$Al_{0.2}Ga_{0.8}N$ 20 nm	
	P-waveguide layer	GaN 100 nm	
10	P-cladding layer	$Al_{0.16}Ga_{0.84}N$/GaN	20
	P-contact layer	GaN 20 nm	
11	Insulating layer	SiO_2	27
12	Plating layer	Au	317

3. Results and discussion

Using the above-mentioned parameters, we can calculate the temperature distributions in different parts of the LD package structure. Figure 2 shows the calculated results of temperature distribution in a contour plot for epi-up (a) and epi-down (b) configurations, respectively. For an epi-up configuration, the local temperature increases steeply in the vicinity of the light-emitting layer. The obtained thermal resistance is 37.16 K/W, which is almost equal to 37.9 K/W

as reported by Hwang *et al.*[1] However, for an epi-down configuration, the local temperature increases most steeply in the P-type stripe area and the AuSn solder (up), and the thermal resistance is 28.71 K/W. The thermal resistance of the epi-down configuration is 9.19 K/W, smaller than that for the epi-up configuration. In addition, the temperature difference inside the LD chip for epi-down configuration is smaller than that for the epi-up one.[1]

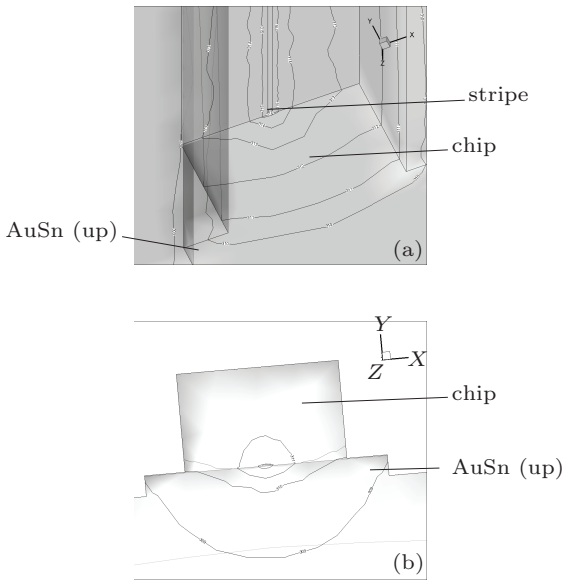


Fig. 2. Temperature distributions near the front cavity facet of GaN LD devices in a TO 56 package for epi-up configuration (a) and epi-down configuration (b) in a contour plot (units: K)

The numerical calculation of the thermal resistance of different parts of the packaged LD structure is conducted. At first, the thermal resistance of the GaN diode chip is calculated on the assumption that other parts of the package structure each have an infinitely high thermal conductivity. Afterwards, the AuSn (up) with a limited thermal conductivity is considered to calculate the new value of the thermal resistance, which minus the thermal resistance of the GaN LD chip, thereby obtains the thermal resistance of AuSn (up). The other outer parts of the package structure can be calculated one by one in a similar way. The calculated thermal resistances of the stem, the heat sink, the solder (down), the AlN submount, the solder (up), and the chip are 4.5 K/W, 12.92 K/W, 0.55 K/W, 4.43 K/W, 2.29 K/W, and 12.48 K/W, respectively. The thermal resistance value of the heat sink is the largest one among them, followed by the chip, the stem, and the AlN submount. This result suggests that the heat sink, chip, stem, and AlN submount parameters should be optimized.

3.1. Effect of thermal conductivity on the thermal resistance

To gain a deep insight into the effect of various parameters on the thermal characteristics, we analyse the effects of thermal conductivities of different parts in the package structure on the thermal resistance for both epi-up and epi-down configurations. As shown in Figs. 3 and 4, the thermal conductivity of the heat sink has the largest influence on thermal resistance.

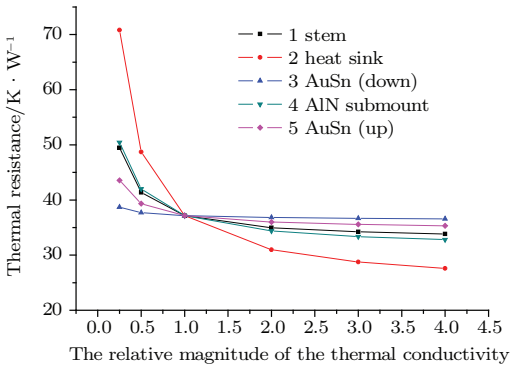


Fig. 3. Effects of thermal conductivities of different parts in the packaged structure on the thermal resistance of an epi-up LD device in the TO 56 package.

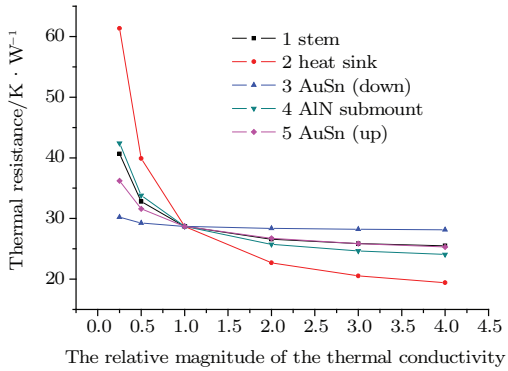


Fig. 4. Effects of thermal conductivities of various parts on the thermal resistance of an epi-down LD device in the TO 56 package.

It plays the most significant role in the thermal resistance among these packaging parts no matter whether it is in an epi-up configuration or in an epi-down one. For the epi-up configuration, this result is consistent with the fact that the thermal resistance of heat sink is the largest one among these parts. Based on the results in Fig. 4, it would be better to change the heat sink material from Kovar to, for example, Cu in order to increase the thermal conductivity. The thermal conductivity of Cu is 398 W/mK, which is much larger than the 46 W/mK of Kovar. By using Cu

as the heat sink, the thermal resistance in the epi-up configuration decreases from 37.16 K/W down to 25.6 K/W; in the epi-down configuration, the thermal resistance decreases from 28.71 K/W to 17.47 K/W. So the thermal resistance will be effectively reduced when a material with better thermal conductivity is chosen to make the heat sink.

3.2. Effect of the thickness of GaN substrate on the thermal resistance

It is noted that due to the lack of a GaN substrate, cheaper sapphire is often used as the substrate to grow GaN LDs. However, sapphire has a poor thermal conductivity (47 W/mK). We also calculate the thermal resistances for both the epi-up configuration and the epi-down configuration with the GaN-based LDs grown on sapphire substrate instead of GaN substrate. For an epi-up configuration, it is found that the thermal resistance increases from 37.16 K/W up to 51.22 K/W, indicating that the substrate may seriously affect the thermal resistance and reliability of a GaN LD device. But for an epi-down configuration, the obtained result of thermal resistance is almost the same for both substrates, the thermal resistance of the GaN LD device is 28.71 K/W approximately. This result can be well explained by the fact that in the epi-down case most of the heat flux is not dissipated through the substrate. In addition, we also investigate the effect of the thickness of GaN substrate on the thermal characteristics of LDs grown on GaN substrate in the epi-up configuration. As shown in Fig. 5, the thermal resistance increases linearly with the increase of the thickness of the GaN substrate, suggesting that the substrate should be made as thin as possible to reduce thermal resistance.

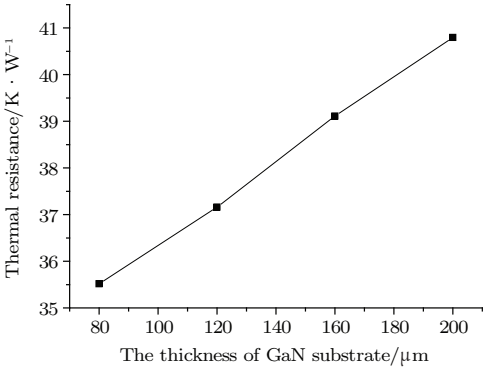


Fig. 5. Effect of the thickness of GaN substrate on the thermal resistance of an epi-up LD in a TO 56 package.

3.3. Effect of the thickness of the AlN submount on thermal resistance

As mentioned above, we have tried to optimize the parameters of the heat sink and the GaN substrate. Now we analyse the effects of the stem and AlN submount parameters on the thermal characteristics of GaN LDs in a TO 56 package. However, the size of commercially-available stems is standardized, and normally the stem material is also fixed for convenience of sealing. In this case, we calculate only the thermal resistances each as a function of the thickness of AlN submount for both the epi-up configuration and the epi-down configuration. The thermal conductivity of AlN is taken to be 170 W/mK. As shown in Figs. 6(a) and 6(b), with the increase of the thickness of AlN submount, the thermal resistance decreases down to the minimum value and then increases again. This interesting phenomenon can be analysed as follows. The heat sink has poor thermal conductivity (46 W/mK), and the heat is generated in the LDs within a very small area.

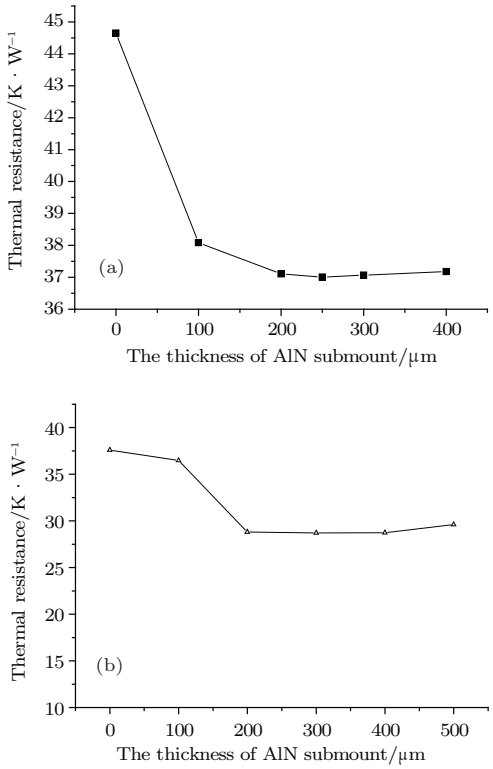


Fig. 6. Effects of the thickness of the AlN submount on the thermal resistance of epi-up LDs (a) and epi-down LDs (b) in a TO 56 package.

When the thickness of the AlN submount is too small, the generated heat cannot propagate to a large area

immediately, as schematically shown in Fig. 7(a). The effective heat conduction area is limited to be very small, which makes the thermal resistance very high. However, with the increase of the thickness of the AlN submount, the heat can dissipate to a larger area, and then better dissipate in the heat sink, as shown in Fig. 7(b). The effective heat conduction area becomes larger, which eventually lowers the thermal resistance down to a minimum. However, as the thickness continues to increase, the heat flux will have to propagate and pass through the thicker material, which raises the thermal resistance again. As shown in Fig. 6, the optimal thicknesses for epi-up configuration and epi-down configuration are 200 μm–300 μm and 200 μm–400 μm, respectively.

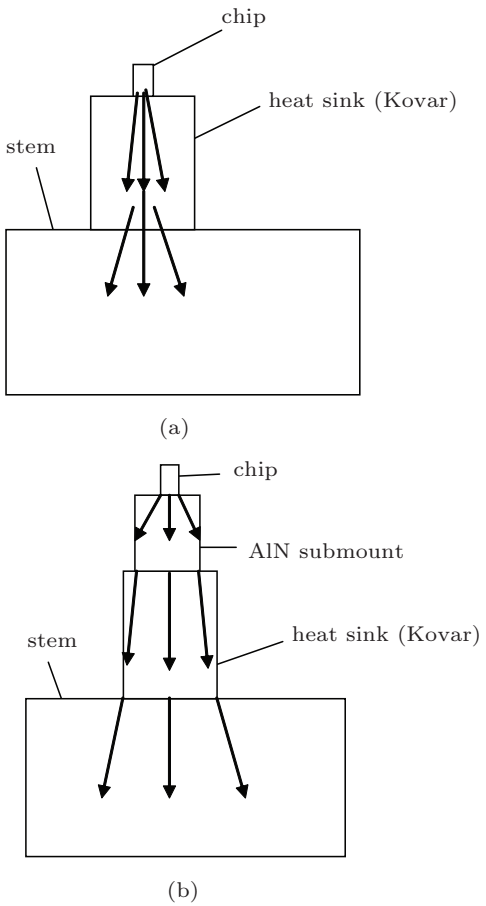


Fig. 7. Distributions of the heat flux for GaN LDs in a TO 56 package without AlN submount (a) and with AlN submount (b).

3.4. Effect of the heat distribution on the thermal resistance

For GaN-based LD a large amount of heat may also be generated in the P-waveguide layer, the P-contact layer, and the P-cladding layer apart from the active region. The distributions of heat in these regions will affect the thermal resistance of the GaN LD device, too. We suppose that the heat distribution in the P-contact layer and the P-cladding layer is uniform, and name it region 1, the rest of heat source is uniformly distributed in the active region and the P-waveguide layer. The dependences of thermal resistance on the heat generated in region 1 for both epi-up LDs and epi-down LDs are calculated, and the results are shown in Figs. 8(a) and 8(b) respectively. From Fig. 8, it is found that when the heat generated in the region 1 is reduced, the thermal resistance of the device decreases linearly no matter whether it is epi-up LDs or epi-down LDs, but the slope is small in the epi-down case because it has a lower thermal resistance.

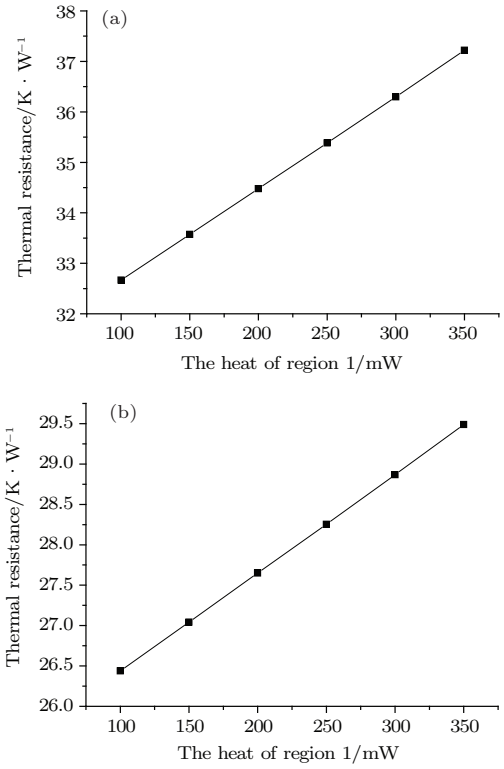


Fig. 8. Effects of the heat source on thermal resistance of epi-up LDs (a) and epi-down LDs (b) in a TO 56 package.

4. Conclusion

We calculated the thermal resistances of the package materials of GaN LDs in a TO 56 package, and analysed the effects of various thermal parameters on the thermal characteristics of GaN LDs for both epi-up configuration and epi-down configuration. From the analyses it is suggested that the heat sink material should be made of materials with relatively high

thermal conductivity. The epi-up and epi-down LDs have optimal thicknesses of AlN submount, which are 200 μm–300 μm and 200 μm–400 μm, respectively.

References

[1] Hwang W J, Lee T H, Nam O H, Kim H K, Kwak J S, Park Y J and Shin M W 2006 *Phys. Status Solidi* C **3** 2174

[2] Ji L, Jiang D S, Zhang S M, Liu Z S, Zeng C, Zhao D G, Zhu J J, Wang H, Duan L H and Yang H 2010 *Chin. Phys.* B **19** 124211

[3] Nakamura S, Senoh M, Nagahama S, Iwasa N, Yamada T, Matsushita T, Sugimoto Y and Kiyoku H 1996 *Appl. Phys. Lett.* **69** 3034

[4] Hatakoshi G, Onomura M, Yamamoto M, Nunoue S, Itaya K and Ishikawa M 1999 *Jpn. J. Appl. Phys.* **38** 2764

[5] Nakamura S, Senoh M, Nagahama S, Iwasa N, Yamada T, Matsushita T, Sugimoto Y and Kiyoku H 1996 *Appl. Phys. Lett.* **69** 4056

[6] Nakamura S, Senoh M, Nagahama S, Iwasa N, Yamada T, Matsushita T, Sugimoto Y and Kiyoku H 1997 *Appl. Phys. Lett.* **70** 868

[7] Nakamura S, Senoh M, Nagahama S, Iwasa N, Yamada T, Matsushita T, Sugimoto Y and Kiyoku H 1997 *Appl. Phys. Lett.* **70** 1417

[8] Kim J M, Kim S, Kang S B, Kim Y J, Jeong H, Lee K, Kim J, Lee S, Suh D, Yi J H, Choi Y, Jung S G and Noh M 2010 *Phys. Status Solidi* C **7** 1801

[9] Takahashi K, Matsuoka D, Harima H, Kisoda K, Tsuda Y, Yuasa T and Taneya M 2007 *Phys. Status Solidi* C **4** 2802

[10] Ryu H, Ha K, Chae J, Nam O and Park Y 2005 *Appl. Phys. Lett.* **87** 093506

[11] Lee M, Boucke K, Gotz M, Meyer A, Kelemen M, Lehman N and Sopra F 2008 *Proc. SPIE* **6876** 687609

[12] Yang L, Jang S, Hwang W and Shin M 2007 *Thermochimica Acta* **455** 95

[13] Shan Q, Dai Q, Chhajed S, Cho J and Schubert E F 2010 *J. Appl. Phys.* **108** 084504

[14] Zhu C, Zhang Y G, Li A Z and Tian Z B 2006 *J. Appl. Phys.* **100** 053105

[15] Zhu C, Zhang Y G, Li A Z and Zheng Y L 2005 *Semicond. Sci. Technol.* **20** 563