The influence of thermally assisted tunneling on the performance of charge trapping memory*

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We evaluate the influence of the thermally assisted tunneling (TAT) mechanism on charge trapping memory (CTM) cell performance by numerical simulation, and comprehensively analyse the effects of the temperature, trap depth, distribution of trapped charge, gate voltage and parameters of TAT on erasing/programming speed and retention performance. TAT is an indispensable mechanism in CTM that can increase the detrapping probability of trapped charge. Our results reveal that the TAT effect causes the sensitivity of cell performance to temperature and it could affect the operational speed, especially for the erasing operation. The results show that the retention performance degrades compared with when the TAT mechanism is ignored.

Keywords: thermally assisted tunneling, charge trapping memory, erasing/programming/retention performance

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1. Introduction

With the progress in non-volatile semiconductor memory, products with high density, high performance and low cost have developed rapidly. However, the conventional floating gate flash memory encounters barriers due to its decreased coupling ratio and cell-to-cell interference during scaling down.[1] Charge trapping memory (CTM) can be used as the next generation of non-volatile memory for its scalability, complementary metal oxide semiconductor (CMOS) process compatibility, and improved reliability. Simulator tools are important for investigating device performance under different conditions, analysing the physical mechanisms, and predicting changes without increasing the complexity and fabrication costs. The detrapping mechanism of trapped charge in the charge storage layer is one of the most important aspects influencing CTM performance. As one dominant detrapping mechanism, thermally assisted tunneling (TAT) is investigated by our simulator, accompanied by types of important mechanisms in CTM including direct/Fowler–Nordheim tunneling,[2] trap assisted tunneling,[3] thermal excitation, and carrier capture processes.[4] We evaluate its effects on the performance of CTM based on the $TaN/Al_2O_3/Si_3N_4/SiO_2/Si$ (TANOS)[5–8] structure with different temperatures, trap depths, gate voltages, trapped charge distributions, and TAT parameters. The results are helpful for optimizing the performance and enhancing the reliability of the charge trapping memory.

2. The TAT model and simulation method

TAT is a kind of charge detrapping mechanism in the charge trapping layer of CTM, as shown in Fig. 1(a). TAT is a two-step detrapping effect, in which trapped electrons/holes are first thermally excited above the ground trap level and then tunnel through the barrier. The TAT effect combines the thermal excitation and tunneling as a whole part and can better describe the charge-detrapping phenomenon in silicon nitride.

Due to the Poole–Frenkel effect,[9,10] the barrier near the trapped charge is reduced. The trapped electrons/holes can be thermally excited to the first excited state above the ground trap level, and then they can tunnel out of the trap state to the conduction band for electrons and the valance band for holes.[11] The ionization energy $q\Phi_t$ is reduced by the trapped

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charge applied electric field E for $q\Delta\Phi_t$

$$q\Delta\Phi_t = q^{3/2}(E/\pi\varepsilon_0\varepsilon_{Si_3N_4})^{-1/2}. \quad (1)$$

e_{TAT} is the thermally assisted tunneling probability

$$e_{TAT} = \nu_{TAT}\exp[-(q\Phi_t - q\Delta\Phi_t - q\Delta\Phi_{TAT})/\kappa T] \times T(q\Phi_t - q\Delta\Phi_t - q\Delta\Phi_{TAT}), \quad (2)$$

where T is the temperature, $q\Delta\Phi_{TAT}$ is the first excited state energy, ν_{ThAT} is the TAT coefficient, referred to as the attempt-to-escape frequency, and $T(q\Phi_t - q\Delta\Phi_t - q\Delta\Phi_{TAT})$ is the probability of trapped charge tunneling from the first excited state to the conduction band or valance band of Si_3N_4.

The above-mentioned TAT mechanism is included in the simulator[12] of the self-consistent simulation of the erasing/programming/retention operation of CTM with an arbitrary trap state profile in the charge storage layer, which was developed by ourselves. The simulator is initiated by the ISE–TCAD tool and can obtain the performance of CTM during erasing/programming/retention operation. The key parameters used in this work are listed in Table 1. The structure of CTM with TANOS, used for the verification and evaluation of the TAT effect, is shown in Fig. 1(b). The simulator has been verified with experimental data.[13]

Table 1. The default parameters used in this work.

Parameters	Description	Value
Φ_{t_e}, Φ_{t_h}/eV	Electron/hole trap depth in Si_3N_4	1.6/1.6
Φ_{e,SiO_2}, Φ_{h,SiO_2}/eV	TAT trap Depth in SiO_2	1.82/1.23
σ_e, σ_h/cm^2	Capture cross section	1.0×10^{-13}/1.0×10^{-13}
m^*_{e,SiO_2}, m^*_{h,SiO_2}	Electron/hole effective mass in SiO_2	0.42/0.96
m^*_{e,Si_3N_4}, m^*_{h,Si_3N_4}	Electron/hole effective mass in Si_3N_4	0.848/0.95

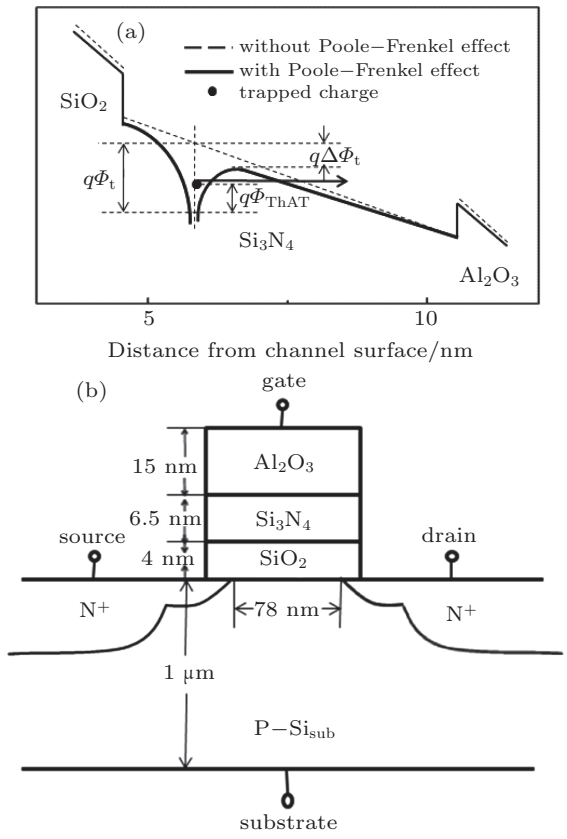


Fig. 1. (a) Schematic of the TAT effect, and (b) cross section of the TANOS device used in this work.

3. Results and analysis

TAT is an important charge detrapping mechanism for CTM. It increases the probability of the trapped charge escaping to the conduction band for electrons and to the valance band for holes. In order to evaluate its influence, the erasing/programming performance of TANOS is studied with and without TAT. The critical parameters of TAT, including trap depth Φ_t, attempt-to-escape frequency ν_{TAT} and first excited state energy $\Delta\Phi_{TAT}$, which affect TANOS performance, are investigated.

The effects of TAT on the erasing and programming performances at different gate voltages are shown in Fig. 2. Figure 3 shows the operational speed with the erasing/programming window reaching 6 V. From the results we can see that a higher gate voltage can increase the erasing/programming speed and weaken the influence of the TAT effect. Additionally, the TAT effect causes higher erasing speed and lower programming speed. The erasing operation starts with the Si_3N_4 layer storing more electron trap states, and the programming operation starts with the condition that hole trap states occupy the Si_3N_4 layer. The TAT mechanism can accelerate the erasing speed since it helps the trapped electrons escape to the conduction band of Si_3N_4 and then tunnel to the substrate. We can see that the erasing speed could be higher with TAT than without it in the whole process of the erasing operation. However, due to the fact that the detrapping of trapped holes needs a quite low trap

depth and high energy of the first excited state, TAT hardly affect the speed at the beginning of the programming operation. However, after the Si_3N_4 layer has stored some trapped electrons, TAT could cause them to detrap again, which results in a relatively low programming speed after about 10^{-6} s.

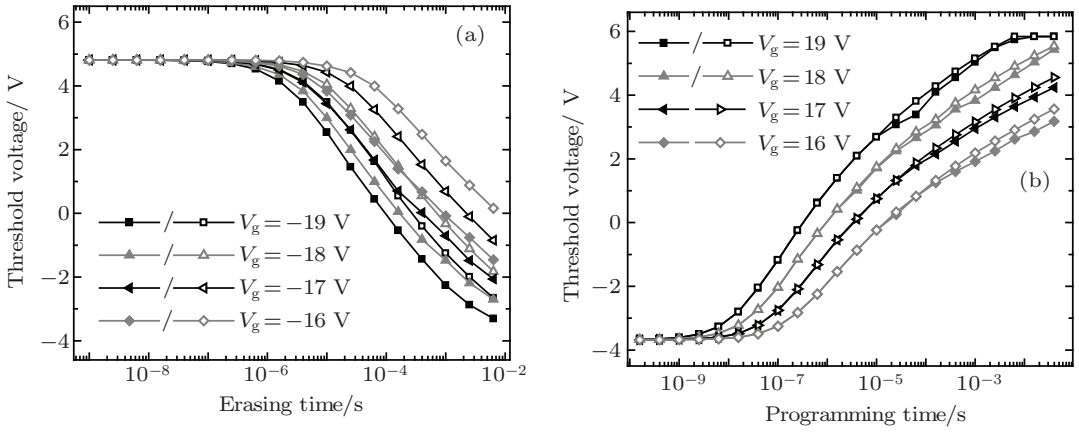


Fig. 2. The effect of TAT on (a) erasing and (b) programming performance. Solid curve: with TAT; open curve: without TAT.

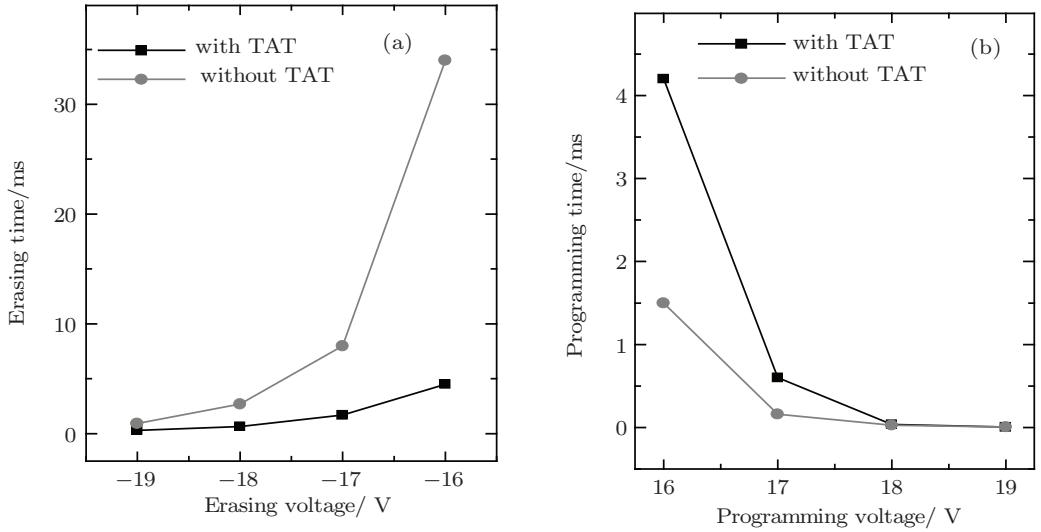


Fig. 3. The effects of TAT on (a) erasing and (b) programming speed under different gate voltages. $\Phi_t = 1.6$ eV, $\Phi_{TAT} = 0.4$ eV, $N_e = 2.8 \times 10^{19}$ cm^{-3}, and $\Delta V_{th} = 6$ V.

Temperature and trap depth are important factors influencing the TAT probability. Higher temperature and lower trap depth mean a larger TAT probability, which leads to faster erasing speed and degraded retention, as illustrated in Figs. 4 and 5, respectively. It can also be seen that the TAT effect is more sensitive at a temperature of around 300 K than at higher temperature.

Additionally, the attempt-to-escape frequency and first excited state energy of the trapped charge are two other critical parameters of TAT. A higher attempt-to-escape frequency ν_{TAT} and higher first excited state energy $q\Delta\Phi_{TAT}$ will lead to an improvement in erasing speed, as shown in Figs. 6 and 7, respectively.

The spatial distribution of trapped charges in the charge storage layer Si_3N_4 is critical for determining the performance of the TANOS device. We investigate uniform distribution and exponentially decreasing distribution with the same total number of charge traps. The results shown in Fig. 8 illustrate that the erasing speed is greatly affected by the spatial distribution of charge traps with or without TAT. It can be seen that more trapped charges close to the substrate side in the

Si_3N_4 correspond to a higher erasing speed.

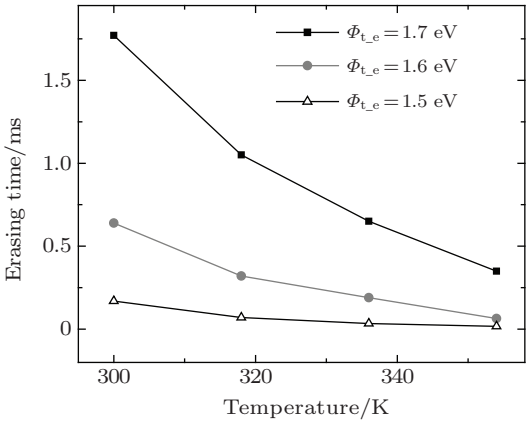


Fig. 4. The effects of temperature and trap depth on erasing time.

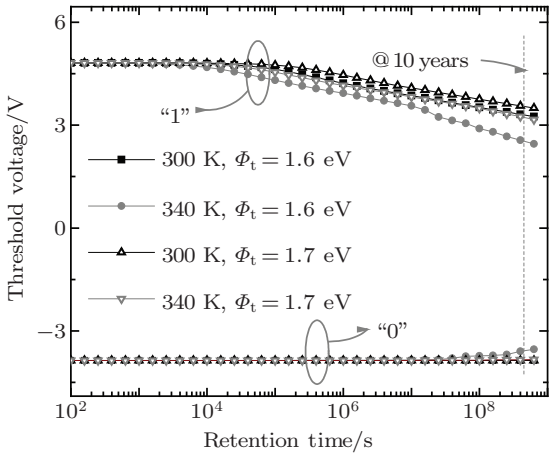


Fig. 5. The effects of temperature and trap depth on retention performance.

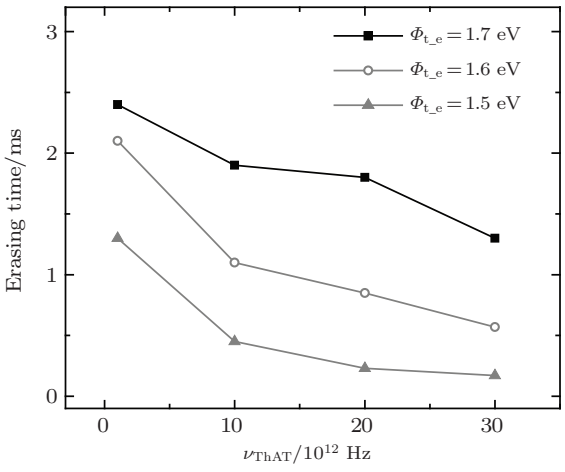


Fig. 6. The effects of attempt-to-escape frequency on erasing time. $V_g = -18$ V, $\Delta V_{th} = 6$ V.

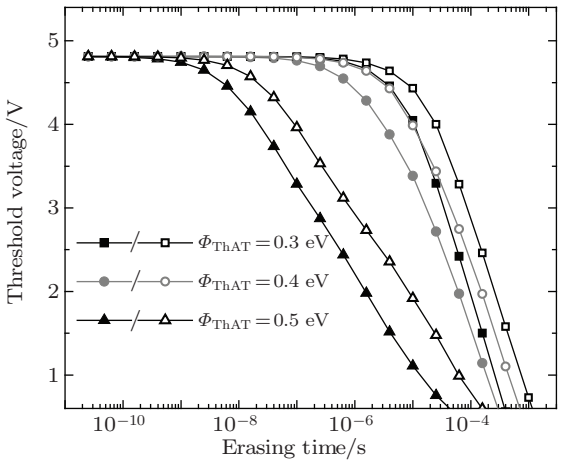


Fig. 7. The effects of first excited state on erasing time at $V_g = -18$ V (solid) and $V_g = 17$ V (open).

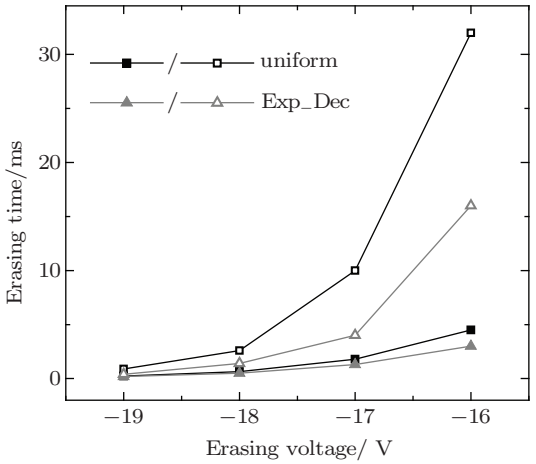


Fig. 8. The effect of the spatial distribution of the trapped charge in Si_3N_4. Solid curve: with TAT; open curve without TAT. $\Delta V_{th} = 6$ V.

4. Conclusion

As an indispensable detrapping mechanism, the TAT effect is investigated by our simulator, accompanied with other important models in the TANOS device. The results reveal that it greatly affects the detrapping probability, accelerates the erasing speed, and degrades the retention performance. Higher erasing/programming voltages and temperatures could weaken the effect of TAT, while the effect will be enhanced with a higher attempt-to-escape frequency, a higher first excited state, and a lower trap depth in Si_3N_4.

References

[1] ITRS 2007 *Emerging Research Devices* p. 5
[2] Schenk A and Heiser G 1997 *J. Appl. Phys.* **81** 7900

[3] Wu J, Register L F and Rosenbaum E 1999 *Proc. IPRS* p. 389
[4] McWhorter P J, Miller S L and Dellin T A 1990 *J. Appl. Phys.* **68** 1902
[5] Lee C H, Choi K I, Cho M K, Song Y H, Park K C and Kim K 2003 *International Electron Devices Meeting* p. 26.5.1
[6] Specht M, Reisinger H, Stadele M, Hofmann F, Gschwandtner A, Landgraf E, Luyken R J, Schulz T, Hartwich J, Dreeskornfeld L, Rosner W, Kretz J and Risch L 2003 *ESSDERC* p. 155
[7] Zheng Z W, Huo Z L, Zhu C X, Xu Z G, Liu J and Liu M 2011 *Chin. Phys.* B **20** 108501
[8] Xu G B and Xu Q X 2009 *Chin. Phys.* B **18** 768
[9] Ganichev S D, Ziemann E and Prettl W 1999 *Phys. Rev.* B **61** 361
[10] Maity R, Kundoo S and Chattopadhysy K K 2005 *Sol. Energy Mater. Sol. Cells* **86** 217
[11] Manzini S 1987 *J. Appl. Phys.* **52** 3278
[12] Song Y C, Du G, Xia Z L, Yang J F, Jing R, Han R Q, Lee K H and Liu X Y 2006 *Proc. ICSICT* p. 772
[13] Park Y, Choi J, Kang C, Lee C, Shin Y, Choi B, Kim J, Jeon S, Sel J, Park J, Choi K, Yoo T, Sim J and Kim K 2006 *Proc. IEDM* p. 29