Novel high-voltage power lateral MOSFET with adaptive buried electrodes*

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(Received 24 October 2011; revised manuscript received 8 December 2011)

A new high-voltage and low-specific on-resistance ($R_{on,sp}$) adaptive buried electrode (ABE) silicon-on-insulator (SOI) power lateral MOSFET and its analytical model of the electric fields are proposed. The MOSFET features are that the electrodes are in the buried oxide (BOX) layer, the negative drain voltage V_d is divided into many partial voltages and the output to the electrodes is in the buried oxide layer and the potentials on the electrodes change linearly from the drain to the source. Because the interface silicon layer potentials are lower than the neighboring electrode potentials, the electronic potential wells are formed above the electrode regions, and the hole potential wells are formed in the spacing of two neighbouring electrode regions. The interface hole concentration is much higher than the electron concentration through designing the buried layer electrode potentials. Based on the interface charge enhanced dielectric layer field theory, the electric field strength in the buried layer is enhanced. The vertical electric field E_I and the breakdown voltage (BV) of ABE SOI are 545 V/μm and −587 V in the 50 μm long drift region and the 1 μm thick dielectric layer, and a low $R_{on,sp}$ is obtained. Furthermore, the structure also alleviates the self-heating effect (SHE). The analytical model matches the simulation results.

Keywords: adaptive buried electrode, interface charge, breakdown voltage, enhanced dielectric layer field

PACS: 71.10.–w, 73.20.–r, 73.40.Qv, 77.22.Jp **DOI:** 10.1088/1674-1056/21/7/077101

1. Introduction

The silicon-on-insulator (SOI) device suffers from a low breakdown voltage (BV) and has a high specific on-resistance ($R_{on,sp}$). Some structures have been proposed to increase the BV values,[1−12] in which a charge on the interface of the buried layer has been introduced to realize high BV,[10−12] and low $R_{on,sp}$ values of SOI devices have been obtained.[12,13] Therefore, those SOI structures, which have been used to obtain a trade-off between BV and $R_{on,sp}$, are attractive. In this article, a structure with adaptive buried electrodes (ABEs) on SOI is proposed. Its BV is enhanced, owing to the modulation effect of the interface charge on the electric fields of the drift region and the buried layer. Our research results show that the new structure can not only enhance BV, but also reduce $R_{on,sp}$ and the self-heating effect (SHE).

2. Structure and mechanism

The cross-section of the ABE SOI power lateral MOSFET (pLDMOS) is shown in Fig. 1, where the electrodes are inserted uniformly into the buried layer, the partial voltages of V_d are output to the electrodes, and each electrode has a potential with the absolute value reducing linearly from the drain to the source. Due to the fact that the potential of the silicon layer on the top interface of the buried layer is lower than the neighboring electrode potential, the interface hole concentration is much higher than the electron concentration. The N_d and L_d are the doping concentration and the length of the drift region, respectively, t_I , t_S, and t_{sub} are the thicknesses of the buried layer, the silicon layer, and the substrate layer, respectively, and W is the spacing between the two neighboring electrodes.

The absolute value of the electrode potential in the buried oxide layer reduces linearly from the drain to the source. Therefore, the hole concentration on

*Project supported by the National Natural Science Foundation of China (Grant No. 60906038) and the Science Technology Foundation for Young Scientist of University of Electronic Science and Technology of China (Grant No. L08010301JX0830).

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the top interface of the buried dielectric layer increases linearly from the drain to the source. The holes are produced through changing the electrode potential, so the model of the electrode potential and the model of the holes are equivalent. We can extract the influence of the electrode potentials on the electric field and the BV through researching the interface hole concentrations on the electric field and the BV.

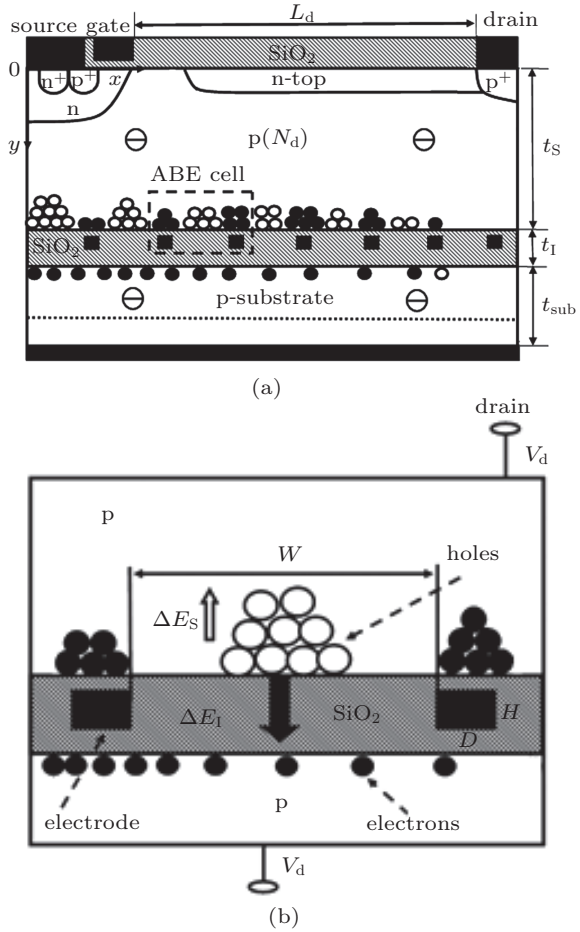


Fig. 1. Structure and mechanism of ABE SOI pLDMOS. Panel (a) shows the device structure, panel (b) shows the cell structure and the working mechanism of ABE SOI.

The expressions for the electric field and the BV will be obtained using an analytical model of pLDMOS. The coordinate origin in the drain is chosen for pLDMOS, and the x direction is from the drain to the source (this coordinate system is only used for the electrical equivalent model, the coordinate origin in the results and discussion is chosen to be in the source). Under the conditions of the electrical equivalent model, a high negative voltage V_S ($V_S = -V_d$) is applied to the source, while the drain and the substrate are grounded, $\sigma(x)$ is the interface charge distribution, $\sigma(L_d)$ is the maximum charge density under the source. The two-dimensional (2D) potential $\phi(x, y)$ in the drift region can be written as

$$\frac{\partial^2\phi(x,y)}{\partial x^2} + \frac{\partial^2\phi(x,y)}{\partial y^2} = \frac{qN_d}{\varepsilon_S}, \quad 0 \le x \le L_d, 0 \le y \le t_S. \tag{1}$$

The boundary conditions are

$$\frac{\partial\phi(x,y)}{\partial y}|_{y=0} = 0, \tag{2a}$$

$$\frac{\partial\phi(x,y)}{\partial y}|_{y=t_S} = \frac{q\sigma(x)}{\varepsilon_S} - \frac{\varepsilon_I\phi(x,t_S)}{\varepsilon_S t_I}, \tag{2b}$$

$$\phi(0,0) = 0, \phi(L_d,0) = V_S. \tag{2c}$$

The $\phi(x, y)$ can be written into a sum of two parts

$$\phi(x,y) = \omega(x,y) + \varphi(x,y), \quad 0 \le x \le L_d,\ 0 \le y \le t_S, \tag{3}$$

with $\omega(x, y)$ and $\varphi(x, y)$ being the contributions of V_S and the net charge in the drift region, respectively. From Eq. (1), it follows that

$$\frac{\partial^2\omega(x,y)}{\partial x^2} + \frac{\partial^2\omega(x,y)}{\partial y^2} = 0, \quad 0 \le x \le L_d,\ 0 \le y \le t_S, \tag{4}$$

The boundary conditions are

$$\omega(0,0) = 0, \quad \omega(L_d,0) = V_S, \tag{5a}$$

$$\left.\frac{\partial\omega(x,y)}{\partial y}\right|_{y=0} = 0, \tag{5b}$$

$$\left.\frac{\partial\omega(x,y)}{\partial y}\right|_{y=t_S} = -\frac{\varepsilon_I\omega(x,t_S)}{\varepsilon_S t_I}. \tag{5c}$$

The $\omega(x,y)$ can be expanded in the Taylor series along the y direction as

$$\omega(x,y) \cong \omega(x,0) + \left.\frac{\partial\omega(x,y)}{\partial y}\right|_{y=0} y + \left.\frac{\partial^2\omega(x,y)}{\partial y^2}\right|_{y=0} \frac{y^2}{2}. \tag{6}$$

From Eq. (6), the relationship between the surface potential of silicon and the interface potential of the buried layer is derived as

$$\left.\frac{\partial^2\omega(x,y)}{\partial y^2}\right|_{y=0} = -\frac{\omega(x,0)}{t^2}, \quad 0 \le x \le L_d,\ 0 \le y \le t_S, \tag{7}$$

where

$$t = \sqrt{\frac{1}{2}t_S^2 + \frac{\varepsilon_S}{\varepsilon_I}t_S t_I}$$

is the characteristic thickness of the SOI device. From Eqs. (6) and (7), the electric potential $\omega(x,y)$ can be obtained as

$$\omega(x,y) = \omega(x,0)\left(1 - \frac{y^2}{2t^2}\right),$$

$$0 \le x \le L_{\rm d},\ 0 \le y \le t_{\rm S}. \tag{8}$$

By solving Eq. (11), the electric potential $\omega(x,0)$ is derived as

$$\omega(x,0) = \frac{V_{\rm S}}{\sinh(L_{\rm d}/t)} \sinh\left(\frac{x}{t}\right). \tag{9}$$

The same derivation for $\varphi(x,y)$ leads to

$$\frac{\partial^2 \varphi(x,y)}{\partial x^2} + \frac{\partial^2 \varphi(x,y)}{\partial y^2} = \frac{qN_{\rm d}}{\varepsilon_{\rm S}},$$
$$0 \le x \le L_{\rm d},\ 0 \le y \le t_{\rm S}. \tag{10}$$

The boundary conditions are

$$\varphi(0,0) = 0,\ \varphi(L_{\rm d},0) = 0, \tag{11a}$$
$$\left.\frac{\partial \varphi(x,y)}{\partial y}\right|_{y=0} = 0, \tag{11b}$$
$$\left.\frac{\partial \varphi(x,y)}{\partial y}\right|_{y=t_{\rm S}} = \frac{q\sigma(x)}{\varepsilon_{\rm S}} - \frac{\varepsilon_{\rm I}\varphi(x,t_{\rm S})}{\varepsilon_{\rm S} t_{\rm I}}, \tag{11c}$$

where $\sigma(x) = \sigma(L_{\rm d})x/L_{\rm d}$, $\sigma(L_{\rm d})$ is the hole's maximal concentration on the surface of the buried oxide layer under the source. The $\varphi(x,y)$ can be expanded in the Taylor series along the y direction as

$$\varphi(x,y) \cong \varphi(x,0) + \left.\frac{\partial \varphi(x,y)}{\partial y}\right|_{y=0} y + \left.\frac{\partial^2 \varphi(x,y)}{\partial y^2}\right|_{y=0} \frac{y^2}{2}. \tag{12}$$

Solving Eq. (10) yields

$$\varphi(x,0) = \frac{A}{2\sinh(L_{\rm d}/t)} {\rm e}^{x/t} - \frac{B}{2\sinh(L_{\rm d}/t)} {\rm e}^{-x/t} + \frac{t_{\rm I} q\sigma(L_{\rm d})}{L_{\rm d}\varepsilon_{\rm I}} t^2 - \frac{qN_{\rm d}}{\varepsilon_{\rm S}} t^2, \tag{13}$$

where

$$A = \frac{qN_{\rm d}}{\varepsilon_{\rm S}} t^2 \left[1 - {\rm e}^{L_{\rm d}/t} + 2\sinh\left(\frac{L_{\rm d}}{t}\right)\right] - \frac{t_{\rm I} q\sigma(L_{\rm d})}{\varepsilon_{\rm I}}, \tag{14}$$
$$B = \frac{qN_{\rm d}}{\varepsilon_{\rm S}} t^2 \left(1 - {\rm e}^{L_{\rm d}/t}\right) - \frac{t_{\rm I} q\sigma(L_{\rm d})}{\varepsilon_{\rm I}}. \tag{15}$$

Combining Eqs. (3), (9), and (13), we can obtain $\phi(x,0)$ as

$$\phi(x,0) = \varphi(x,0) + \frac{V_{\rm S}}{\sinh(L_{\rm d}/t)} \sinh\left(\frac{x}{t}\right). \tag{16}$$

Combining Eqs. (3), (6), and (12), we can derive $\phi(x,y)$ as

$$\phi(x,y) = \left(1 - \frac{y^2}{2t^2}\right)\phi(x,0) + \frac{y^2}{2}\frac{t_{\rm I} q\sigma(x)}{t^2 \varepsilon_{\rm I}},$$

$$0 \le x \le L_{\rm d},\ 0 \le y \le t_{\rm S}. \tag{17}$$

By solving Eq. (17), $E_x(x,0)$ is derived as

$$E_x(x,0) = -\frac{B + V_{\rm S}}{t\sinh(L_{\rm d}/t)} \cosh\left(\frac{x}{L}\right) - \frac{qN_{\rm d}}{\varepsilon_{\rm S}} t\, {\rm e}^{x/t} - \frac{t_{\rm I} q\sigma(L_{\rm d})}{L_{\rm d}\varepsilon_{\rm I}}. \tag{18}$$

From Eq. (17), the vertical electric field $E_y(x,y)$ can be expressed as

$$E_y(x,y) = -\frac{\partial \phi(x,y)}{\partial y} = \frac{y}{t^2}\phi(x,0) - \frac{y t_{\rm I} q\sigma(x)}{t^2 \varepsilon_{\rm I}}. \tag{19}$$

Based on Eq. (19), the silicon layer electric field $E_{\rm S}$ (under source) is expressed as

$$E_{\rm S} = E_y(L_{\rm d}, t_{\rm S}) = -\frac{\partial \phi(L_{\rm d}, t_{\rm S})}{\partial y}. \tag{20}$$

Combining Eqs. (15) and (20), we can express $E_{\rm S}$ as

$$E_{\rm S} = \frac{t_{\rm S}}{t^2}\left(V_{\rm S} - \frac{t_{\rm I} q\sigma(L_{\rm d})}{\varepsilon_{\rm I}}\right). \tag{21}$$

Combining Eqs. (3)–(21) and the interface Gaussian theory (under source), we can write the vertical electric field $E_{\rm I}$ as

$$E_{\rm I} = \frac{\varepsilon_{\rm S} E_{\rm S}}{\varepsilon_{\rm I}} + \frac{q\sigma(L_{\rm d})}{\varepsilon_{\rm I}}. \tag{22}$$

Based on Eqs. (21) and (22), $E_{\rm I}$ is derived as

$$E_{\rm I} = \frac{\varepsilon_{\rm S}}{\varepsilon_{\rm I}}\left[\frac{t_{\rm S}}{t^2}\left(V_{\rm S} - \frac{t_{\rm I} q\sigma(L_{\rm d})}{\varepsilon_{\rm I}}\right)\right] + \frac{q\sigma(L_{\rm d})}{\varepsilon_{\rm I}}. \tag{23}$$

From Eqs. (21) and (23), it follows that interface charge $\sigma(x)$ in the proposed ABE SOI can enhance $E_{\rm I}$ in comparison with the conventional SOI ($\sigma = 0$), and shielding the silicon layer electric field $E_{\rm S}$ can avoid the silicon layer premature breakdown. The reason for the enhanced $E_{\rm I}$ of the ABE SOI is shown in Eq. (24), that $(t_{\rm S}/t^2)\left[V_{\rm S} - t_{\rm I} q\sigma(L_{\rm d})/\varepsilon_{\rm I}\right]$ is less than the critical electric field of the silicon layer and its maximal value can only be the critical electric field of the conventional SOI, but $q\sigma(L_{\rm d})/\varepsilon_{\rm I}$ is determined by the interface charge $\sigma(x)$. For example, when the values of $\Delta\sigma(x)$ ($\Delta\sigma(x)$ is the change of $\sigma(x)$) are 5×10^{12} cm^{-2} and 1×10^{13} cm^{-2}, the values of $\Delta E_{\rm I}$ ($\Delta E_{\rm I}$ is the change of $E_{\rm I}$) are 232 V/μm and 464 V/μm, respectively. So $E_{\rm I}$ of the ABE SOI is determined mainly by the latter. These all will contribute to the high BV. Moreover, with $\sigma = 0$, equations (21) and (23) can be used for the conventional SOI.

3. Results and discussion

The 2D device simulations using the device parameters[14] specified in Table 1 for the proposed ABE SOI pLDMOS are performed to verify the device operation and the correctness of the model, where t_n is the thickness of the n-top layer, and N_{sub} is the p-substrate concentration.

Table 1. Device parameters used in the simulations, where Con. SOI stands for the conventional SOI.

Parameters	ABE SOI	Con. SOI
L_d/μm	20–80	20–80
t_S/μm	5	5
t_I/μm	1	1
t_n/μm	0.5	0.5
t_{sub}/μm	2	2
N_{sub}/cm^{-3}	2×10^{14}	2×10^{14}
W/μm	0–8	–

The adaptive charge concentration distribution for the ABE SOI pLDMOS at the device breakdown is shown in Fig. 2. Figure 2(a) shows the hole concentration on the top interface of the buried dielectric layer. Plentiful quasi-continuous holes are located on the top interface, the concentration increases linearly from the drain to the source, and the maximal concentration is 2.26×10^{18} cm^{-3}. Moreover, there is a maximal value of 4.56×10^{17} cm^{-3} existing on the top interface, but the electrons and the holes have opposite concentration trends on the top interface. Figure 2(b) shows the electron concentration on the bottom interface of the buried layer. As the electrode potential is modulated, resulting in the hole concentration distribution increasing linearly from the drain to the source, a maximal concentration of 2.69×10^{18} cm^{-3} is obtained. The charge concentrations distributed on the top and the bottom interfaces of the buried layers not only enhance the electric field strength but also modulate the drift field, so the BV is increased.

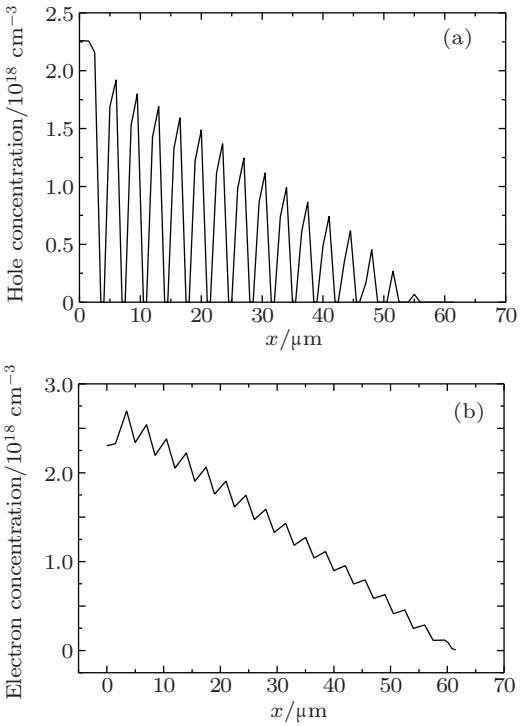


Fig. 2. Charge distributions for the ABE SOI pLDMOS at device breakdown voltage (t_S = 5 μm, t_I = 1 μm, L_d = 50 μm, D = H = 0.5 μm, W = 3 μm, N_d = 2.35×10^{15} cm^{-3}, N_{sub} = 2×10^{14} cm^{-3}). Panels (a) and (b) show hole concentration distributed on the top (y = 4.999 μm) interface of the buried dielectric layer and electron concentration distributed under the bottom (y = 6.001 μm) interface of the buried dielectric layer, respectively.

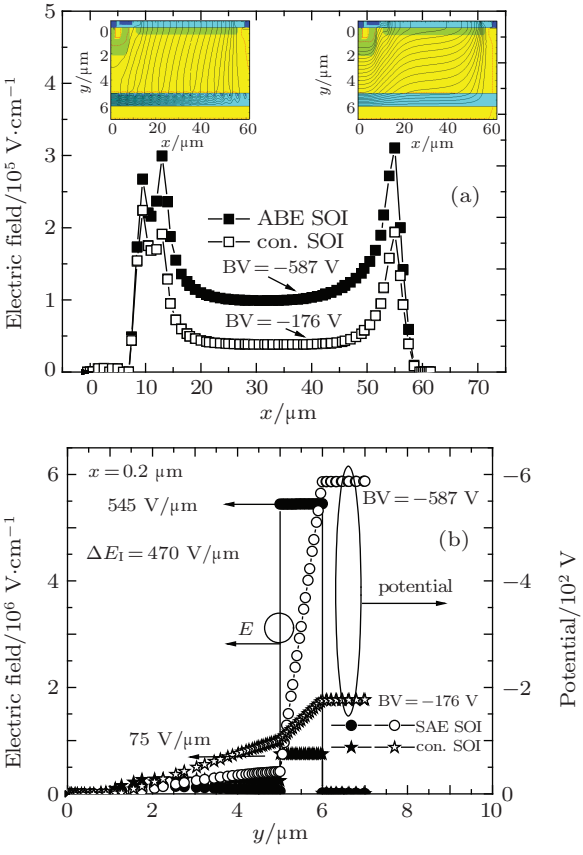


Fig. 3. (colour online) Equipotential contours, surface electric fields, vertical electric fields, and potential distributions at device breakdown voltage for ABE SOI pLDMOS and the conventional SOI (t_S = 5 μm, t_I = 1 μm, L_d = 50 μm, conventional SOI N_d = 8×10^{14} cm^{-3}, ABE N_d = 2.35×10^{15} cm^{-3}). (a) Surface electric field distribution and equipotential contour distributions (insets) under the source (y = 0.001 μm), (b) Vertical electric field and potential distributions at breakdown voltage under the source.

The equipotential contours, the surface electric fields ($y = 0.001$ μm), the vertical electric fields under the source for ABE SOI pLDMOS and the conventional SOI LDMOS at the breakdown voltage are compared in Fig. 3. A more optimized equipotential line distribution in the silicon layer for ABE SOI LDMOS is obtained due to the modulation effect of the high concentration ($> 2 \times 10^{18}$ cm^{-3}) holes on the top interface of the buried layer. Moreover, the surface electric field has a higher middle drift electric field, which is higher than that in the conventional SOI structure. The modulation of the high concentration holes leads to $E_{\rm I} = 75$ V/μm and $E_{\rm S} = 15$ V/μm of the conventional SOI increasing to $E_{\rm I} = 545$ V/μm and $E_{\rm S} = 5$ V/μm of the ABE SOI. The BV=−587 V is achieved with $t_{\rm S} = 5$ μm and $t_{\rm I} = 1$ μm in the simulation, while BV is only −176 V for the conventional SOI. Based on Eqs. (22) and (24), the calculation results of $E_{\rm I}$ and $E_{\rm S}$ are 558.5 V/μm and 11.26 V/μm, respectively, The analytical results match the simulation results, as shown in Fig. 3(b).[15] The charge accumulating ability of the new structure is obvious.

Figure 4 shows the influence of drift length on BV and $R_{\rm on,sp}$ for the ABE pLDMOS and nLDMOS. The voltage of the ABE SOI nLDMOS increases from 653 V to 1420 V with the increase in length $L_{\rm d}$ from 50 μm to 140 μm, while the voltage of the conventional SOI nLDMOS remains at about 293 V because of clamping by the vertical voltage. When $V_{\rm gs} = 20$ V, $R_{\rm on,sp}$ of ABE SOI nLDMOS and that of the conventional SOI nLDMOS are almost the same. When $L_{\rm d}$ is 60 μm, the values of $R_{\rm on,sp}$ are 0.209 Ω·cm^2 and 0.236 Ω·cm^2, respectively, and when $L_{\rm d}$ is 140 μm, the values are 1.176 Ω·cm^2 and 1.171 Ω·cm^2, respectively. As the buried electrodes have less effect on the concentration of drift region, the voltage of ABE SOI is increased not at the expense of enhancing $R_{\rm on,sp}$. The voltage of the ABE SOI pLDMOS varies from −318 V to −863 V with an increase in length $L_{\rm d}$ from 20 μm to 80 μm, while the voltage of the conventional SOI pLDMOS remains at about −176 V. When $V_{\rm gs} = -20$ V, $R_{\rm on,sp}$ of the ABE SOI pLDMOS markedly decreases compared with that of the conventional SOI pLDMOS. When $L_{\rm d}$ is 40 μm, the $R_{\rm on,sp}$ values of ABE SOI nLDMOS and the conventional SOI nLDMOS are 0.189 Ω·cm^2 and 0.924 Ω·cm^2, respectively, and when $L_{\rm d}$ is 60 μm, the values are 0.412 Ω·cm^2 and 2.01 Ω·cm^2, respectively. The p-type ABE can increase the voltage, at the same time, the concentration of the drift region of the ABE SOI pLDMOS is higher than that of the conventional SOI pLDMOS owing to the electrode-assisted depletion, the value of $R_{\rm on,sp}$ decreases obviously. The result shows that it is more advantageous to use the buried electrodes on pLDMOS than on nLDMOS.

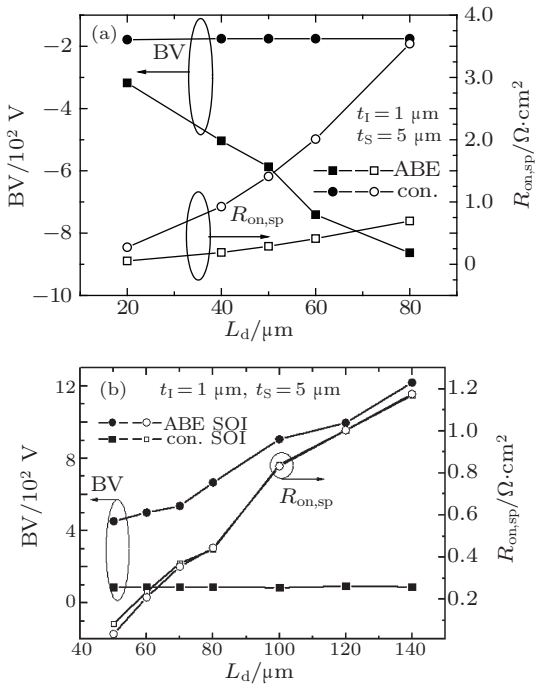


Fig. 4. Influences of the drift region lengths of (a) p- and (b) n-channel ABE SOI LDMOS on specific on-resistance $R_{\rm on,sp}$ and BV.

Figure 5 shows the influence of D, W, H, and $t_{\rm I}$ on BV for the ABE SOI pLDMOS. It can be seen from Fig. 5 that there is a steady BV of −587 V with D and H increasing from 0.1 μm to 1.2 μm, which fully shows that the electrode can be made into a point electrode, the width and the height of the ABE SOI electrode have little effect on the BV. When W varies from 1 μm to 8 μm, the BV is steady; when W is less than 4 μm, the BV decreases to −450 V and fast drops after W has been larger than 5 μm. This shows that there is a saturation value of W. If W is too large, the height of the potential well reduces, so the ability of banding charge is weakened. The voltage is not sensitive to the variation of the buried layer thickness, when the buried layer thickness increases from 1 μm to 3 μm, the voltage is unchanged and remains at −587 V. So the buried layer can be neither too thin nor too thick. A too thin buried layer results in a breakdown, and a too thick buried layer makes the process not easy to implement and leads to a poor thermal characteristic. This fully shows that this structure has a large control range and a strong ability to introduce charge. The ABE method has advantages over the method of

fixing charge into the buried layer of SOI LDMOS.[16]

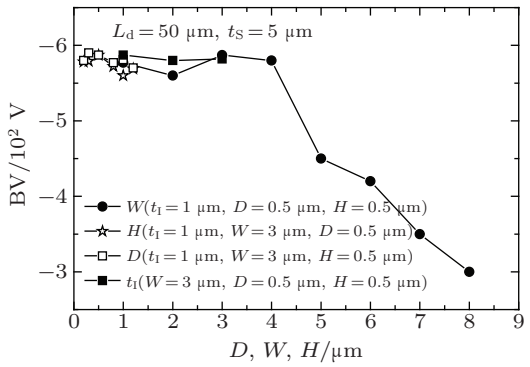


Fig. 5. Influence of device parameters on BV.

Figure 6 shows the thermal characteristics of the two devices. The temperature of the bottom of the substrate is maintained at 300 K, and the gate voltage (V_g) is −20 V for all simulations. When V_s is −40 V, the drain surface temperature of the ABE SOI is lower than that of the conventional SOI, and the maximal temperature T_{max} of the ABE SOI is 318.9 K, Three-dimensional (3D) temperature distributions of the two structures are shown in the insets of Fig. 6. It can be concluded that the proposed ABE SOI can enhance the breakdown voltage and keep the self-heating effect (SHE) at a lower value.

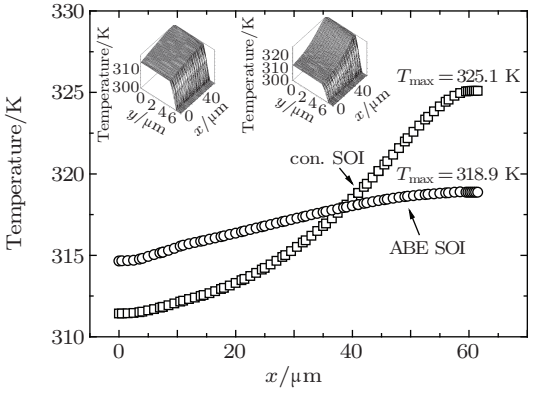


Fig. 6. Thermal characteristics ($L_d = 50$ μm, $t_S = 5$ μm, $t_I = 1$ μm, $V_g = -20$ V, $V_S = -40$ V). The insets show the 3D temperature distributions of the two structures.

4. Conclusion

An ABE SOI pLDMOS high voltage device structure is proposed. By changing the electrode potential linearly in the buried layer, the interface accumulation charge on the buried layer enhances the electric field and increases the breakdown voltage. Compared with the conventional SOI with $L_d = 50$ μm, $t_S = 5$ μm, $t_I = 1$ μm, the BV of the ABE SOI pLDMOS increases from −176 V of the conventional SOI LDMOS to −587 V, the electric field is enhanced from 75 V/μm to 545 V/μm, and $R_{on,sp}$ is reduced by 79.5% compared with that of the conventional SOI pLDMOS. The thermal characteristics are also improved. The improvements of BV, $R_{on,sp}$, and the thermal characteristics of the ABE SOI LDMOS make the proposed structure a very effective interface charge-mode enhanced dielectric layer field device.

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