A novel power UMOSFET with a variable K dielectric layer*

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A novel split-gate power UMOSFET with a variable K dielectric layer is proposed. This device shows a 36.2% reduction in the specific on-state resistance at a breakdown voltage of 115 V, as compared with the SGE-UMOS device. Numerical simulation results indicate that the proposed device features high performance with an improved figure of merit of $Q_{\rm g} \times R_{\rm ON}$ and $\rm BV^2/R_{ON}$, as compared with the previous power UMOSFET.

Keywords: specific on-resistance, power UMOSFET, split gate, variable K dielectric layer

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1. Introduction

The two most important characteristics of power metal–oxide semiconductor field-effect transistors (MOSFETs) are breakdown voltage (BV) and on-state resistance ($R_{\rm ON}$), but it is difficult to realize low specific $R_{\rm ON}$ and high BV simultaneously because these two parameters are interlinked: that one of them is improved can adversely affect the other. Of course, the switching characteristic is also an important property, and it is investigated preferentially in order to obtain high frequency and reduce the conduction loss and switching loss of power MOSFETs in high-frequency power switch applications. In response to these characteristics, the power MOSFETs experienced a period of prosperous rapid development. Research efforts on the various power MOSFETs[1−5] were made for different applications.

A number of device concepts have been proposed in order to improve the tradeoff between specific $R_{\rm ON}$ and BV. Of them, the most noticeable is the superjunction (SJ) effect. To overcome the difficulties of the p–n SJ structure in the practical fabrication process, such as ideal p–n doping matching and small column width for devices below 300 V,[6,7] a gradient oxide-bypassed (GOB) structure was proposed to maintain fabrication simplicity.[8,9] However, the deep trench polysilicon electrode in GOB does not contribute to the device in the ON-state, and the $R_{\rm ON}$ will increase with the increase in the deep trench polysilicon electrode area. Then, a gate-enhanced UMOSFET (GE-UMOS) is proposed to further reduce the $R_{\rm ON}$.[10] However, due to the trench polysilicon connecting to the gate, the parasitic capacitance of GE-UMOS is increased, which will increase the power switching loss,[11] so a gate-enhanced power UMOSFET with a split-gate (SGE-UMOS) structure is proposed, which is more efficient in terms of silicon usage than the GOB-UMOS. At the given BV, SGE-UMOS with a floating trench polysilicon could reduce $R_{\rm ON}$ but not increase the parasitic capacitor, as compared with the GOB-UMOS and GE-UMOS devices.[12]

In addition, through simulations, the SGE-UMOSFET structure has been proven to have better performance than both the SJ and GOB structures. However, due to the difficulties in forming a desired oxide slope, future research on SGE-UMOSFET device realization is required. In this letter, a split-gate enhanced-power UMOSFET with variable K dielectric layer (VKSGE-UMOS) is proposed to further reduce $R_{\rm ON}$ but not increase the parasitic capacitor, as compared with SGE-UMOS devices.

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2. Device structure and operation concept

Figure 1(a) shows a schematic cross-section view of the proposed VKSGE-UMOS structure. In this device, the variable K dielectric layer thickness and the deep trench width are uniform, which replace the gradient oxide-bypassed structures in the GOB-UMOS and SGE-UMOS to reduce the difficulty of the fabrication process, with the electric field distribution in the drift region remaining uniform. Due to the MOS sidewall in the drift region, lateral depletion exists and a lateral field is inserted into the drift region, which is similar to that of the p–n SJ devices. Such field insertion results in the pinch-off of the depletion in the drift region, which modulates the electric field profile in the drift region to enable a higher breakdown voltage for the higher doping device in the drift region.[8] Additionally, the width of the VKSGE-UMOS drift region is the same as that of the SGE-UMOS, but the variable K dielectric layer thickness and the deep trench width is reduced, resulting in the N-type concentration increasing and the $R_{\rm ON}$ reducing for the given BV. Based on the above-mentioned features, the VKSGE-UMOS device will exhibit high performance with improved FOMs of $Q_{\rm g} \times R_{\rm ON}$ and $\mathrm{BV}^2/R_{\rm ON}$.

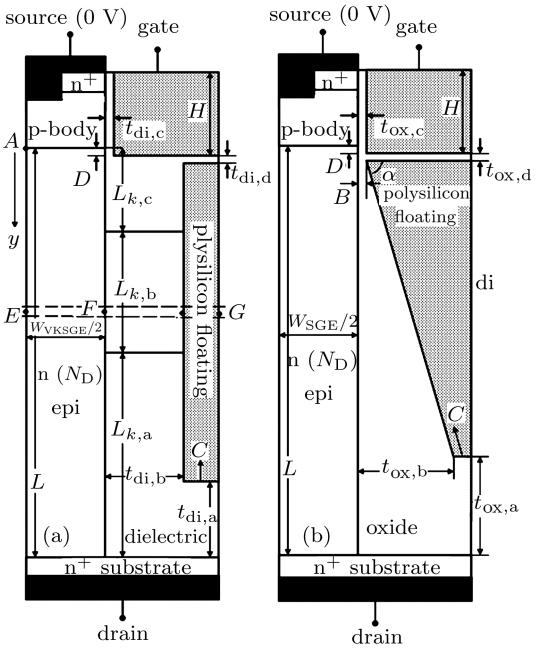


Fig. 1. Schematic cross-section views of (a) VKSGE-UMOS and (b) SGE-UMOS.

The performance of such a device depends on the value of K. The following assumptions are made to simplify the analysis and derive the optimal values.

Imposing the condition that the electric field and the vertical component are uniform in the drift region, and thus the x component of the electric field is also uniform, we obtain

$$\frac{\partial E_y}{\partial y} = 0, \quad \frac{\partial E_x}{\partial y} = 0. \tag{1}$$

We also assume that the drift region is fully depleted under the BV. For $L/w \gg 1$, we can then assume that the potential at any location in the drift region along the dielectric sidewall can be expressed by a linear function of the vertical distance from the p-body/n-drift region junction as

$$V(y) = E_y \times L(y). \tag{2}$$

The BV can be expressed as being linearly proportional to the drift region length, i.e.,

$$V_{\rm br} = E_y L. \tag{3}$$

Referring to Fig. 1(a), the potential difference between points E and G is given by

$$\begin{aligned} V(y) &= V_{AE} \\ &= V_{EF} + V_{FG} \\ &= V_{\rm si}(y) + V_{\rm di}(y) \\ &= E_x \left(\frac{w}{4} + \frac{\varepsilon_{\rm si}}{\varepsilon_{\rm di}} \cdot t_{\rm di} \right), \end{aligned} \tag{4}$$

where $V_{\rm si}(y)$ is the voltage drop across half the drift region at y, and $V_{\rm di}(y)$ is the voltage drop across the dielectric layer at y. Note that we have used the boundary condition at the dielectric–silicon interface. The lateral electric field produced by voltage drop across the dielectric helps to deplete the drift region.

Ignoring the $V_{\rm si}(y)$, and combining Eqs. (1)–(4), we obtain

$$\varepsilon_{\rm di} = \frac{E_x \cdot t_{\rm di}}{E_y} \cdot L \cdot \varepsilon_{\rm si} \cdot \frac{1}{L(y)}, \tag{5}$$

$\varepsilon_{\rm di}$ is approximately inversely proportional to $L(y)$.

Since the derivation is simplified, this equation is not suitable for the accurate K value calculation, but it shows the probable tendency of the variable K values.

To reduce the difficulty in the fabrication process, many kinds of dielectric materials cannot be chosen. So we divide the variable K dielectric layer into three layers, as shown in Fig. 1(a), where the K value of each layer should be a good tradeoff. The dielectric layer is vertically composed of three dielectric layers with different K values: the dielectric layer close to the gate side has the highest K value, while the dielectric layer close to the drain side has the lowest K value.

3. Simulation results and discussion

A cross section of the VKSGE-UMOS structure simulation for the proposed VKSGE-UMOS was performed to verify its operation. The structural parameters for the SGE-UMOS and VKSGE-UMOS are shown in Table 1. In this simulation work, several common dielectrics are used: $K_a = 3.9$, e.g. SiO_2; $K_b = 7.5$, e.g. Oxy nitride; $K_c = 12$, e.g. sapphire, or $HfSiO_4$.[13]

Table 1. The device parameters for the simulations.

Parameter	SGE	VKSGE
n^+ source doping/cm^{-3}	1×10^{19}	1×10^{19}
n^+ source junction depth/μm	0.3	0.3
p-body junction depth/μm	0.9	0.9
p-body peak doping (N_A)/cm^{-3}	1×10^{17}	1×10^{17}
Drift region thickness (L)/μm	5	5.9
Drift region width (W)/μm	0.8	0.8
H/μm	1.0	1.0
N_D/cm^{-3}	5.5×10^{16}	8.0×10^{16}
D/μm	0.1	0.1
($t_{ox,c}/t_{di,c}$)/μm	0.05	0.15
($t_{ox,d}/t_{di,d}$)/μm	0.1	0.1
($t_{ox,a}/t_{di,a}$) and ($t_{ox,b}/t_{di,b}$)/μm	0.9	0.5
C/μm	0	0.2
B/μm	0.05	—
$L_{k,a}/K_a$	—	3.4 μm/3.9
$L_{k,b}/K_b$	—	1.3 μm/7.5
$L_{k,c}/K_c$	—	1.2 μm/12

We used the ATLAS device simulation software[13] to perform the simulations. The Fermi–Dirac statistics and the band gap narrowing effect (BGN) model are employed. For low field bulk mobility, field-dependent motility (FLDMOB) is the concern, and the (CONMOB) model is used to account for the concentration-dependent motilities. The Shockley–Read–Hall recombination (SRH) effect is used for a fixed minority-carrier lifetime, and the electron and hole lifetimes, TAUN and TAUP, are specified as 1×10^{-7} s. The interface charge density is specified as 3×10^{10} cm^{-2}. Auger recombination describes a three-particle transition, therefore a mobile carrier is either captured or emitted.

Figure 2 shows the comparison between the drain-source current (I_{DS})–drain-source voltage (V_{DS}) characteristics of VKSGE-UMOS and SGE-UMOS. The breakdown voltage and the threshold voltage were measured to be 115 V and 2.60 V, respectively. The I_{DS} for VKSGE-UMOS shows a high current as compared with that for SGE-UMOS, which is attributed to the increase in the drift region doping concentration for the VKSGE-UMOS device. Figure 3 shows the approximate electric field distributions at the side of the drift region for SGE-UMOS and VKSGE-UMOS. The comparisons between the gate charging simulations and between the figures of merit (FOMs) ($R_{ON} \times Q_g$) are also shown in Fig. 4.

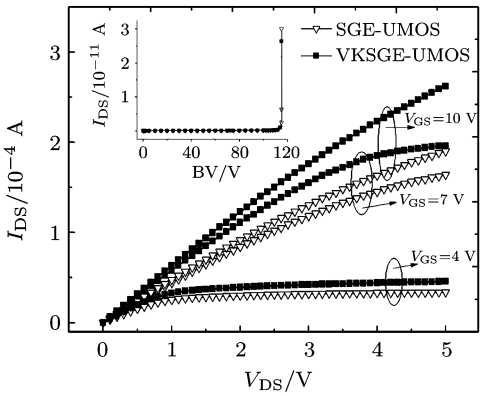


Fig. 2. The I_{DS}–V_{DS} characteristics of the SGE-UMOS and VKSGE-UMOS structures at different values of gate-source voltage (V_{GS}).

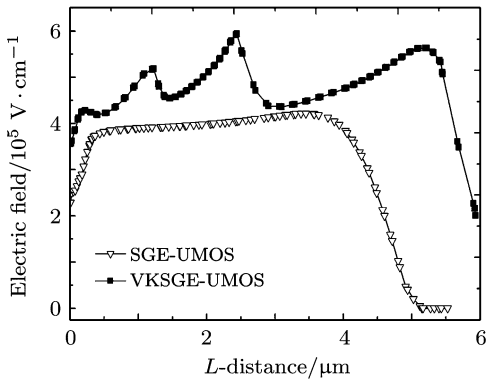


Fig. 3. Simulated electric field distributions at the side of the drift region for SGE-UMOS and VKSGE-UMOS.

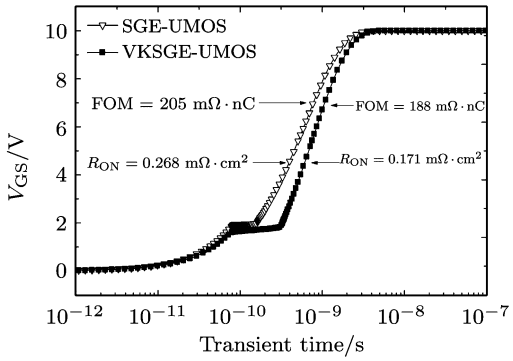


Fig. 4. Variations of V_{GS} and FOM ($R_{ON} \times Q_g$) with transient time for SGE-UMOS and VKSGE-UMOS.

To compare the characteristics of SGE-UMOS and VKSGE-UMOS, we adopt the FOMs of $V_{\rm BD}^2/R_{\rm ON}$ (FOM1) and $R_{\rm ON} \times Q_{\rm g}$ (FOM2). As BV = 115 V and $V_{\rm GS} = 10$ V, we can obtain $\rm FOM1_{SGE}$ (49.4 MW/cm^2) < $\rm FOM1_{VKSGE}$ (77.3 MW/cm^2) and $\rm FOM2_{SGE}$ (205 nC $\cdot$ mΩ) > $\rm FOM2_{VKSGE}$ (188 nC $\cdot$ mΩ), respectively. Here, the charge time of the gate is specified when $V_{\rm GS} = 7$ V. It indicates from the comparison that the VKSGE-UMOS has an improvement in both FOM1 and FOM2 compared with the SGE-UMOS device.

Table 2. Comparison of the performances between the devices.

Devices	BV /V	$R_{\rm on}$/m$\Omega\cdot$cm^2 at $V_{\rm gs} = 10$ V	FOM /(MW/cm^2)
LOCOS MOSFET[14]	119	0.298	47.5
SJ-UMOS[9,10]	115	0.490	27.0
OB-UMOS[9]	115	0.520	25.4
GOB-UMOS[8,12]	116	0.390	34.5
GE-UMOS[10,12]	116	0.273	49.3
SGE-UMOS[12]	115	0.268	49.4
VKSGE-UMOS (this work)	115	0.171	77.3

The performances of the proposed structure are compared with those of the other MOSFETs in Table 2 (for detailed information, interested readers can refer to Refs. [9] and [10]), showing that the proposed device features high performance with an improved figure of merit (FOM) of $\rm BV^2/R_{ON}$, as compared with the previous power UMOSFET.

4. Conclusion

In this paper, a split-gate enhanced-power UMOSFET with variable K dielectric layer (VKSGE-UMOS) is proposed and investigated numerically. This device has a uniform dielectric layer thickness and higher doping concentration in the drift region, which results in a further reduction of $R_{\rm ON}$ compared with that of SGE-UMOS with the same BV. In addition, the gate charging time of VKSGE-UMOS does not increase obviously. This indicates that the proposed device has a high performance and exhibits improved FOMs (both $Q_{\rm g} \times R_{\rm ON}$ and $\rm BV^2/R_{ON}$) compared with SGE-UMOS devices.

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