A low on-resistance triple RESURF SOI LDMOS with planar and trench gate integration*

Luo Xiao-Rong(罗小蓉)[a)b)†], Yao Guo-Liang(姚国亮)[a)], Zhang Zheng-Yuan(张正元)[b)], Jiang Yong-Heng(蒋永恒)[a)], Zhou Kun(周 坤)[a)], Wang Pei(王 沛)[a)], Wang Yuan-Gang(王元刚)[a)], Lei Tian-Fei(雷天飞)[a)], Zhang Yun-Xuan(张云轩)[a)], and Wei Jie(魏 杰)[a)]

[a)] *State Key Laboratory of Electronic Thin Films and Integrated Devices. University of Electronic Science and Technology of China, Chengdu* 610054, *China*

[b)] *No.* 24 *Research Institute of China Electronics Technology Group Corporation, Chongqing* 400060, *China*

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A low on-resistance ($R_{on,sp}$) integrable silicon-on-insulator (SOI) n-channel lateral double-diffused metal–oxide–semiconductor (LDMOS) is proposed and its mechanism is investigated by simulation. The LDMOS has two features: the integration of a planar gate and an extended trench gate (double gates (DGs)); and a buried P-layer in the N-drift region, which forms a triple reduced surface field (RESURF) (TR) structure. The triple RESURF not only modulates the electric field distribution, but also increases N-drift doping, resulting in a reduced specific on-resistance ($R_{on,sp}$) and an improved breakdown voltage (BV) in the off-state. The DGs form dual conduction channels and, moreover, the extended trench gate widens the vertical conduction area, both of which further reduce the $R_{on,sp}$. The BV and $R_{on,sp}$ are 328 V and 8.8 m$\Omega\cdot$cm^2, respectively, for a DG TR metal–oxide–semiconductor field-effect transistor (MOSFET) by simulation. Compared with a conventional SOI LDMOS, a DG TR MOSFET with the same dimensional device parameters as those of the DG TR MOSFET reduces $R_{on,sp}$ by 59% and increases BV by 6%. The extended trench gate synchronously acts as an isolation trench between the high-voltage device and low-voltage circuitry in a high-voltage integrated circuit, thereby saving the chip area and simplifying the fabrication processes.

Keywords: SOI, electric field, breakdown voltage, trench gate, specific on-resistance

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1. Introduction

Lateral double-diffused metal–oxide–semiconductor (LDMOS) field effect transistors are widely used in smart power integrated circuits (ICs) due to their ease of integration and drive. The on-resistance (R_{on}) increases with breakdown voltage (BV) as $R_{on} \propto BV^{2.5}$ in a conventional power LDMOS,[1] resulting in an increase in power loss. The reduced surface field (RESURF) technique is always employed to achieve the trade-off between R_{on} and BV.[2–6] Trench gate metal–oxide–semiconductor field-effect transistors (MOSFETs) further reduce the value of R_{on} because of the high channel density and the elimination of the junction field effect transistor (JFET) effect.[7–14] Two structures, in which the gate and the source or the gate and the drain were placed in one trench, were used to reduce the cell pitch and $R_{on,sp}$.[10,11] Unfortunately, these are good options only for MOSFETs with BV $<$ 100 V, owing to the complex fabrication process and weakened effect for devices with a higher BV. The purpose of this paper is (i) to realize a high BV, (ii) to minimize the on-state loss, and (iii) to isolate the low-voltage circuitry from high-voltage devices in power ICs.

Combining the RESURF technique with the merits of trench gate MOSFETs and LDMOSFETs as mentioned above, we propose a double gate (DG) triple RESURF (TR) SOI LDMOS, which integrates a trench gate and a planar gate. The DGs form dual conduction channels, thereby reducing the value of $R_{on,sp}$. Furthermore, the buried p-layer (BP) and the N-drift region form a triple RESURF, thereby increasing the N-drift doping and reshaping the electric field distribution. A reduced R_{on} and an improved BV are therefore obtained. The extended trench gate realizes the isolation in a high-voltage IC, with the DG TR MOSFET serving as its power device.

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†Corresponding author. E-mail: xrluo@uestc.edu.cn

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2. Device structure and mechanism

Figure 1 shows a schematic cross section of the DG TR MOSFET in an HVIC. It has a planar gate and a trench gate, which is extended to the buried oxide (BOX). The BP is built into the N-drift region, forming a triple RESURF and two parallel current paths. In the layout, the drain region and the trench gate are in the central and peripheral regions, respectively. For the DG TR MOSFET in the blocking state, the high potential from the drain is terminated within the trench gate. A P^+ grounded ring encircles the trench gate, acting as a bypass capacitance to avoid noise. The extended trench gate thus realizes the isolation between the high-voltage and low-voltage regions. In Fig. 1, $L_{\rm bp}$ is the length of the BP, D_1 is the distance of the top interface of the BP from the surface, and $t_{\rm S}$ is the thickness of the SOI layer. $N_{\rm d}$ is the doping concentration of the SOI layer, $t_{\rm I}$ is the thickness of the BOX, and $L_{\rm d}$ is the length of the drift region. Figure 1 shows the x and y directions.

In the on-state, the double gates and the BP layer form two parallel current paths, and the extended trench gate widens the conduction area; moreover, the triple RESURF increases the N-drift doping. All of these reduce the $R_{\rm on}$. In the blocking state, the additional PN junctions consisting of the BP and the N-drift region reshape the electric field, and the extended trench gate also acts as a gate field plate, both of which enhance the BV.

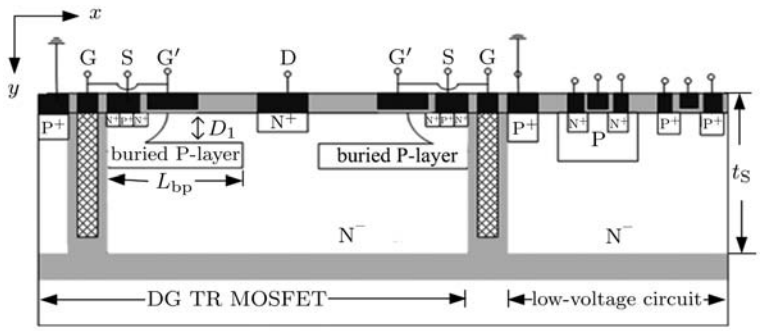


Fig. 1. Schematic cross section of the SOI DG TR LDMOS in an SOI HVIC.

3. Results and discussion

The device structures are investigated by simulation with MEDICI. The models used include CONSRH, AUGER, CONMOB, and FLDMOB, and they are general models for device simulation. Listed in Table 1 are the device materials and the same structural parameters for five types of devices. Figure 2 shows the current flowline contours for the DG TR, trench gate triple RESURF (TG TR), planar gate triple RESURF (PG TR), and double gate (DG) MOSFETs without the BP layer, and the conventional SOI (C-SOI) LDMOS at $V_{\rm GS} = 15$ V, $V_{\rm DS} = 0.5$ V with their own high figure-of-merit (FOM) (FOM = $\rm BV^2/R_{on,sp}$[15]) value. The dual current paths are formed above and below the BP layer, respectively, and the triple RESURF increases the $N_{\rm d}$, which both result in a reduction in the value of $R_{\rm on,sp}$. The BP increases the optimal $N_{\rm d}$ ($N_{\rm d,o}$) from 2.5×10^{15} cm^{-3} of the DG MOSFET to 8×10^{15} cm^{-3} of the DG TR MOSFET. The JEFT effect, caused by the BP, N-drift and p-body, is nevertheless adverse to the reduction in $R_{\rm on}$ for the PG TR and TG TR MOSFETs. Figure 3 shows their current density distributions at $x = 14$ μm. The DG TR MOSFET has the highest average current density and thus the lowest $R_{\rm on,sp}$, while the C-SOI LDMOS is just the opposite. For the TG TR, the optimal $N_{\rm d,o}$ is higher than that for the PG TR. Furthermore, the extended trench gate widens the current path, both of which cause a lower $R_{\rm on,sp}$ than that of the PG TR.

Table 1. The materials and the same structural parameters for DG TR, TG TR, PG TR, DG, and conventional SOI MOSFETs (unit: μm)

Material	$t_{\rm S}$	$t_{\rm I}$	Thickness of BP	$L_{\rm d}$	Cell pitch
SOI	6	2	1	18	25

In Fig. 4, the surface field distributions and the vertical field distributions are given with the same device parameters as those in Fig. 2. The surface field plates of the drain/source and planar gate modulate the surface field. For the DG TR, TG TR, and

PG TR devices, the BP layer enhances the vertical field strength under the BP layer, thereby enhancing the field strength in the buried oxide, as shown in Figs. 4(b) and 5, respectively. In particular, the extended trench gate acts as a field plate to enhance the bulk field at the source side, especially the lateral field. These field-reshaping effects are verified by comparing the equipotential contours of the dashed line rectangles in Figs. 5(a), 5(b), and 5(d) with those of Fig. 5(c), and Fig. 5(e).

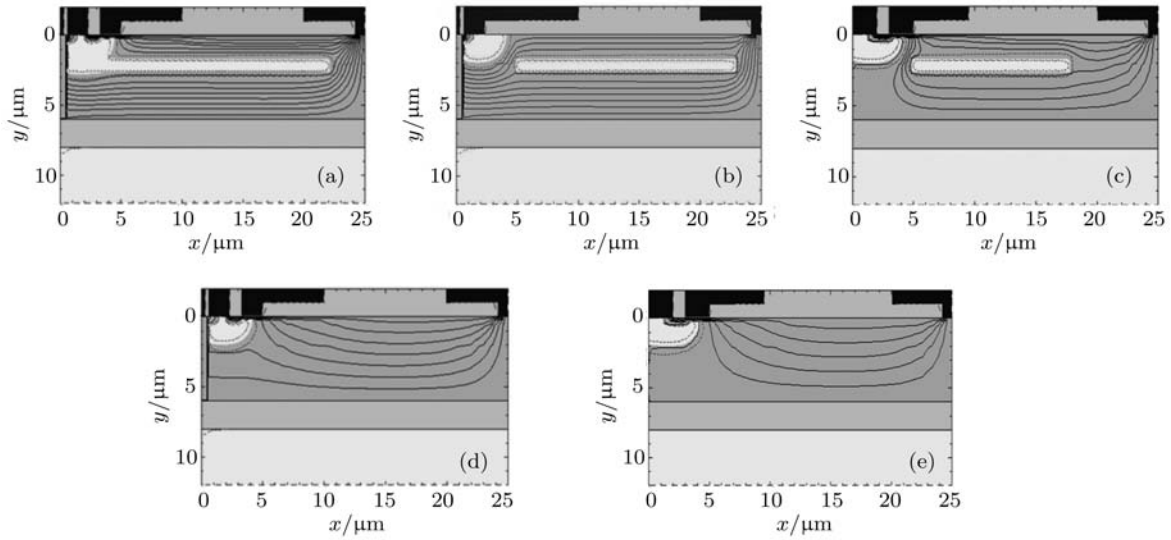


Fig. 2. The current flowline contours for (a) DG TR; (b) TG TR; (c) PG TR; (d) DG; and (e) C-SOI at their own optimal condition (i.e. high FOM value). The BP layer thickness is 1 μm. $V_{GS} = 15$ V, $V_{DS} = 0.5$ V, 10^{-6} A·μm^{-1}/contour.

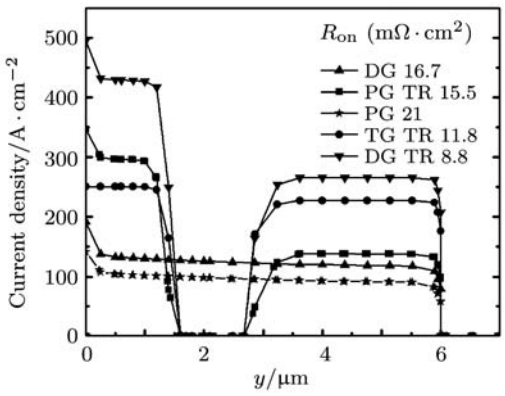


Fig. 3. The current densities in the y direction (x = 14 μm).

The influences of N_d on BV and $R_{on,sp}$, each as a function of D_1 and L_{bp}, are shown in Fig. 6. Figure 6(a) shows that the long BP ($L_{bp} > 8$ μm) effectively increases the $N_{d,o}$ and reduces the $R_{on,sp}$, maintaining a high BV. At $L_{bp} = 0$, the DG TR is a DG MOSFET, which has a low $N_{d,o}$ and high $R_{on,sp}$. Figure 6(c) shows the dependences of the maximum BV (BV_{max}) and $R_{on,sp}$ on L_{bp} and D_1 at their own optimal N_d. The trade-off between the BV and $R_{on,sp}$ is obtained at 18 μm$< L_{bp} <$ 24 μm with a 25 μm device length. Figures 6(b) and 6(c) show that D_1 has a slight influence on BV and R_{on} when 1.3 μm $< D_1 <$ 2.3 μm at $t_S = 6$ μm. Listed in Table 2 are the optimal values of N_d, $R_{on,sp}$, and BV for five devices, showing that the DG TR MOSFET has the highest performance.

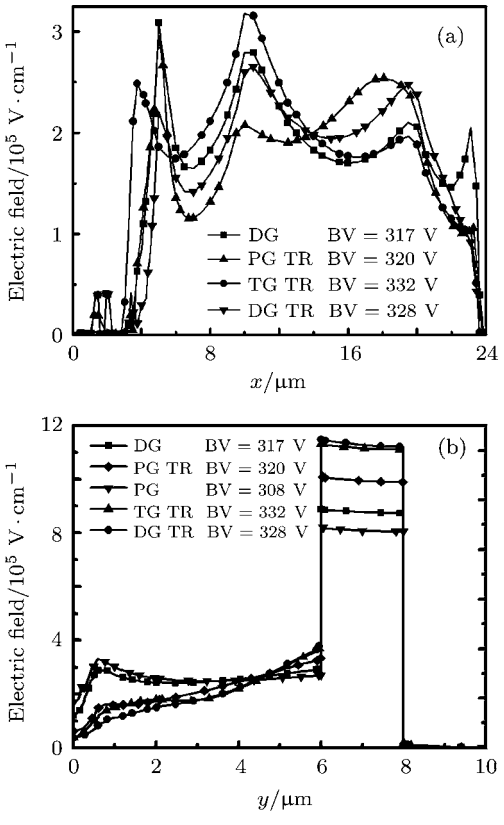


Fig. 4. Electric field distributions of (a) surface field and (b) vertical field in the y direction.

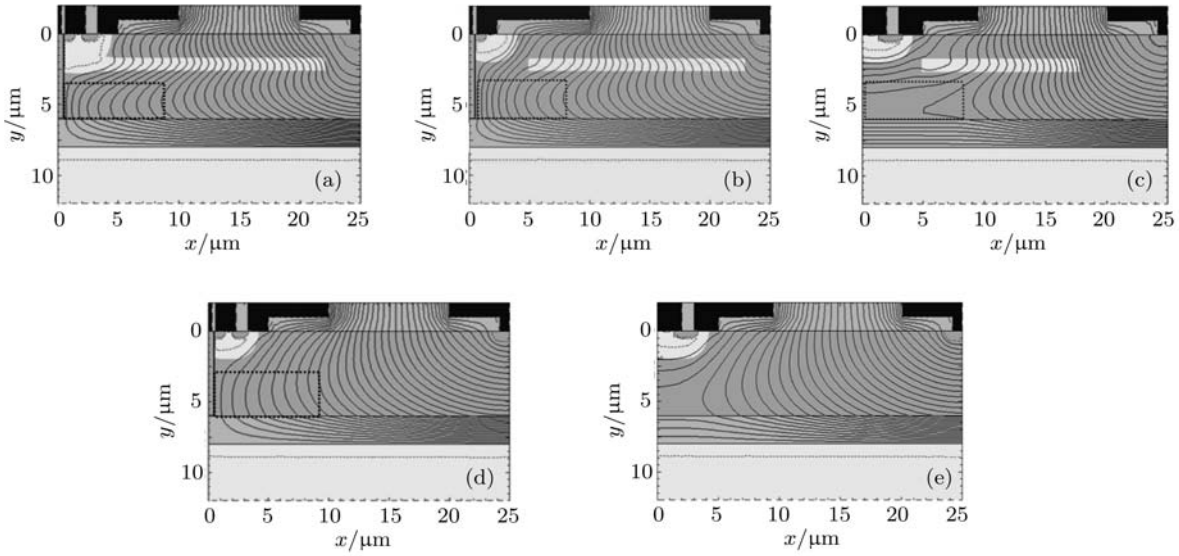


Fig. 5. Equipotential contours at breakdown for (a) DG TR (328 V), (b) TG TR (332 V), (c) PG TR (320 V), (d) DG (317 V), and (e) C-SOI (308 V), with the same device parameters as those in Fig. 2; the potential difference between adjacent equipotential lines is 10 V.

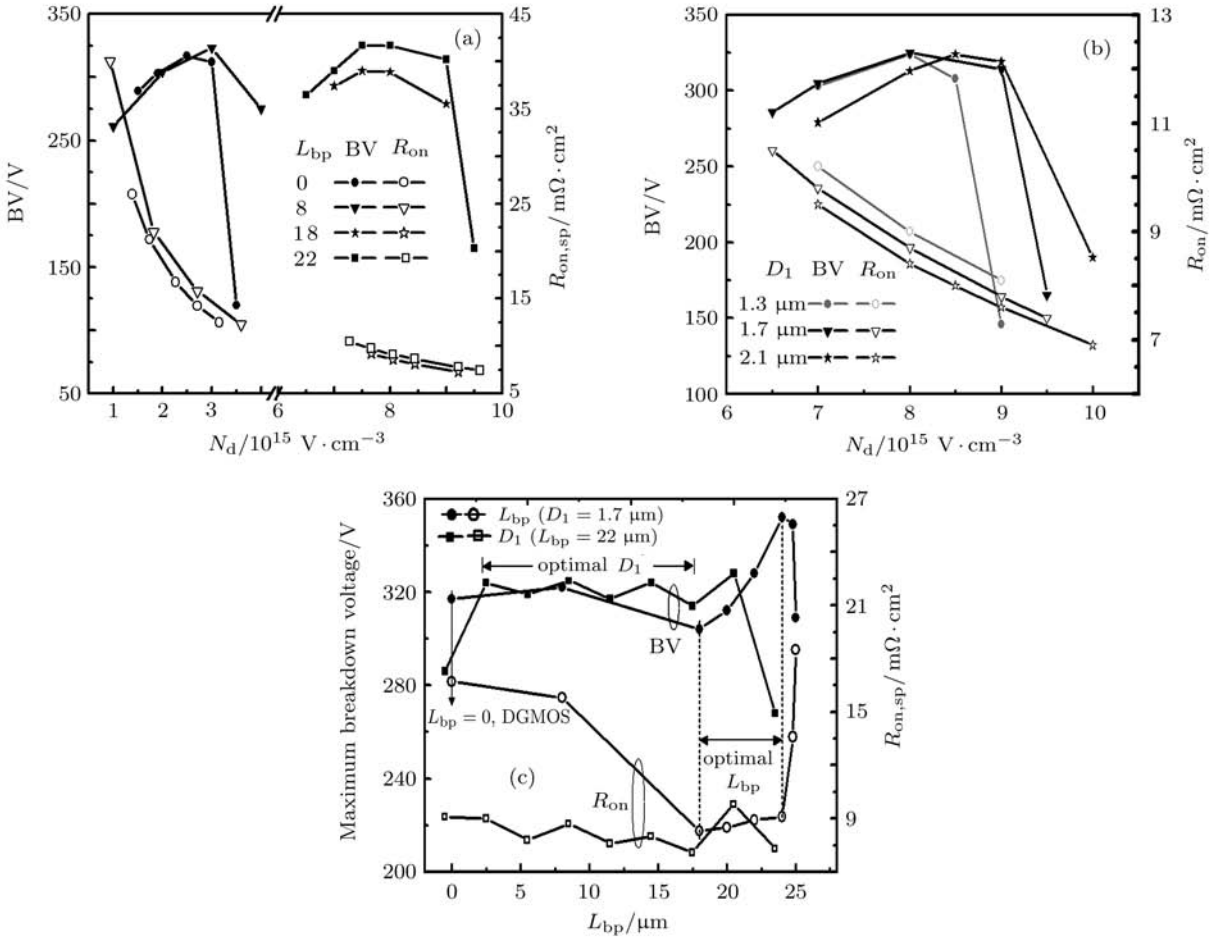


Fig. 6. Dependences of BV and $R_{on,sp}$ on (a) N_d, each as a function of L_{bp} ($D_1 = 1.7$ μm), (b) on N_d, each as a function of D_1 ($L_{bp} = 22$ μm), (c) on L_{bp} ($D_1 = 1.7$ μm) and D_1 ($L_{bp} = 22$ μm) with their own optimal values of N_d for the DG TR MOSFET.

Table 2. BV and $R_{\rm on,sp}$ for SOI MOSFETs (in the on-state, $V_{\rm GS} = 15$ V, $V_{\rm DS} = 0.5$ V).

Device type	$N_{\rm d,o}/10^{15}$ cm^{-3}	$R_{\rm on,sp}/{\rm m}\Omega\cdot{\rm cm}^2$	BV/V
DG TR	8	8.8	328
TG TR	7	11.8	332
PG TR	4.5	15.5	320
DG	2.5	16.7	317
Conventional SOI LDMOS	2	21.6	308

The key steps of one of the feasible fabrication methods for the DTDG SOI MOSFET include implantation followed by Si epitaxy to form the BP layer and N-drift region; p-well implantation, and annealing the p-well and BP layer; etching the Si trench and refilling polysilicon by *in-situ* doping; and forming source/drain regions and electrodes.

4. Conclusion

A low specific on-resistance integrable SOI n-channel LDMOS is proposed and investigated by simulation. The double gates reduce $R_{\rm on,sp}$, and the BP layer reduces $R_{\rm on,sp}$ and improves BV. Compared with conventional SOI LDMOSs, the DG TR MOSFET reduces $R_{\rm on,sp}$ by 59% and maintains a high BV. The extended trench gate synchronously acts as an isolation trench, thereby saving the chip area and simplifying the isolation process in power ICs.

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