Performance of La_2O_3/InAlN/GaN metal–oxide–semiconductor high electron mobility transistors*

Feng Qian(冯 倩)[a)b)†], Li Qian(李 倩)[a)b)], Xing Tao(邢 韬)[a)b)], Wang Qiang(王 强)[a)b)], Zhang Jin-Cheng(张进成)[a)b)], and Hao Yue(郝 跃)[a)b)]

[a)] *School of Microelectronics, Xidian University, Xi'an* 710071, *China*

[b)] *Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices, Xidian University, Xi'an* 710071, *China*

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We report on the performance of La_2O_3/InAlN/GaN metal–oxide–semiconductor high electron mobility transistors (MOSHEMTs) and InAlN/GaN high electron mobility transistors (HEMTs). The MOSHEMT presents a maximum drain current of 961 mA/mm at $V_{gs} = 4$ V and a maximum transconductance of 130 mS/mm compared with 710 mA/mm at $V_{gs} = 1$ V and 131 mS/mm for the HEMT device, while the gate leakage current in the reverse direction could be reduced by four orders of magnitude. Compared with the HEMT device of a similar geometry, MOSHEMT presents a large gate voltage swing and negligible current collapse.

Keywords: indium aluminum nitride, metal–oxide–semiconductor high electron mobility transistor, lanthanum oxide

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1. Introduction

InAlN/GaN-based high electron mobility transistors (HEMTs) can be superior when compared with more conventional AlGaN/GaN HMETs primarily because of the substantially higher polarization-induced two-dimensional electron gas (2DEG) density in the device channel and a possibility to grow a strain-free InAlN/GaN heterostructure.[1−4] On the other hand, it has been observed that a Schottky barrier height on an InAlN remains at only about 1 eV or less, similar to that in an AlGaN/GaN system, and the gate leakage at a high drain bias might even prevent the complete HEMT pinch off. Similarly, it was suggested that filling of the surface states in the gate–drain area of the InAlN/GaN HEMT by electrons emitted from the reverse-biased gate depleted the 2DEG, and led to transients known as the current collapse effect.[5,6]

Gate leakage current is an important factor that restricts the performance and the reliability of a conventional high-power AlGaN/GaN HEMT.[7] Thus, a thin dielectric oxide layer is often inserted between the gate metal and the AlGaN barrier layer, leading to the approach of the MOSHEMT.[8−15] The dielectric was also used to cover the bare surface between the HEMT contacts. Consequently, the AlGaN surface traps became passive and the current collapse reduction was obtained simultaneously with the gate insulation. On the other hand, by applying the gate insulation, the gate-to-channel separation increases, and a shift of V_T resulting from the reduction of a gate-to-source capacitance C_{GS} can be observed. The use of high-permittivity (high-k) insulating materials such as those already reported AlGaN/GaN(Al_2O_3($k_{ox} \sim 9$),[10] HfO_2($k_{ox} \sim$ 20–25)[11] or ZrO2($k_{ox} \sim$ 23–30)[11−14]) has eliminated these drawbacks.

La_2O_3, which has many advantages that were reported, such as its high dielectric constant ($\sim$ 27), its highly insulating properties and its large band gap ($\sim$ 6.0 eV), have been investigated as an FET gate dielectric in silicon.[16,17] In the present work, we present the electrical performance of an La_2O_3/InAlN/GaN MOSHEMT and an InAlN/GaN HEMT. We show an increase of the maximum drain current density by operating a high forward gate bias and a gate leakage current four orders of magnitude smaller than that of the HEMT. Moreover, a large gate voltage swing and negligible current collapse are also observed if compared with an InAlN/GaN Shottky barrier HEMT.

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†Corresponding author. E-mail: qfeng@mail.xidian.edu.cn

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2. Device fabrication

The $In_{0.18}Al_{0.82}N$/GaN lattice-matched heterojunction structure was grown on a 5-cm *c*-face sapphire substrate by metal–organic chemical vapour deposition (MOCVD). A 1-nm thick AlN spacer was located between the InAlN (12-nm thick) and the GaN (1.4 μm) to increase the 2DEG mobility. The measured room temperature, Hall mobility and sheet carrier concentration were 1303 $cm^2/V{\cdot}s$ and 1.4×10^{13} cm^{-2}, respectively.

Electrical isolation was performed by forming a mesa structure with a reactive ion beam etching with a chlorine gas. In order to form the source and drain Ohmic electrodes, Ti/Al/Ni/Au were deposited by electron beam evaporation and annealed by rapid thermal annealing at 830 °C for 30 s in ambient nitrogen gas. Then a 10-nm thick La_2O_3 layer as the gate insulator was sputtered on the InAlN surface, followed by a postdeposition anneal at 500 °C for 5 min to improve the quality of the as-deposited La_2O_3 film. The Ni/Au (200 Å/2000 Å) (1 Å=0.1 nm) serving as the gate metals were deposited using an electron-beam evaporator. The device had a gate length L_g of 1 μm, a gate width W_g of 100 μm, and the source-to-drain spacing was 6 μm.

3. Results and discussion

To characterize the properties of the La_2O_3 film, a metal–oxide–semiconductor (MOS) structure was also fabricated on the heavily Si-doped (n^+) GaN epilayer, which was grown on the sapphire substrate. The current–voltage characteristics of the MOS structure at room temperature were measured using an HP4156C semiconductor parameter analyzer as shown in Fig. 1. Under low voltage, the conduction mechanism of the Schottky emission conduction, following the conduction mechanism of Fowler–Nordheim was observed. If we define the breakdown voltage as the voltage at which the current density is larger than 10^{-7} A/cm^2, the breakdown filed is approximately 3.2 MV/cm.

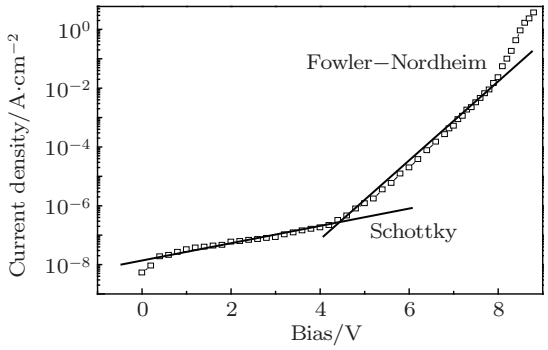


Fig. 1. The log *I–V* characteristics of La_2O_3 thin films.

Figure 2 presents the *C–V* measurements at 1 MHz on MOS-ring capacitors fabricated on the MOSHEMT structure with a diameter of 100 μm. At the site of 2DEG accumulation, a series-connected C_{ox} and C_{HEMT} capacitance equation is used to obtain the capacitance of an La_2O_3 insulator layer as follows:

$$\frac{1}{C_{total}} = \frac{1}{C_{ox}} + \frac{1}{C_{HEMT}},$$
$$C_{ox} = \varepsilon_0\varepsilon_{ox}A/d_{ox},$$
$$A = \pi \times 50 \times 50\ \mu m^2,$$

where C_{total} is the observed accumulation capacitance for the fabricated MOS-ring capacitance and C_{HEMT} represents the capacitance of the undoped InAlN Schottky layer. The capacitance of a 12-nm undoped InAlN Schottky layer (InAlN dielectric constant=8.5) is around 49.3 pF. Based on the measured accumulation capacitance of the fabricated MOS-ring capacitor, C_{total} is 27.1 pF. According to the above equation, the capacitance of La_2O_3 is calculated to be 60.2 pF. Thus, the dielectric constant of La_2O_3 is found to be 17.3. The increase in C_{total} observed at biases larger than 2 V is due to a charge spillover from the 2DEG channel, which brings some of the carriers closer to the surface, thus reducing the effective thickness of the barrier layer and increasing the value of the C_{total}. On the other hand, when we applied increasing voltage up from depletion to accumulation and reducing voltage down from accumulation to depletion, an obvious hysteresis phenomenon (about 0.4 V) is obtained, according to equation $\Delta Q = C\Delta V$, we obtain a trap density of about 6.4×10^{11} cm^{-2}, which indicates there are a lot of trap states at the La_2O_3/InAlN interface.

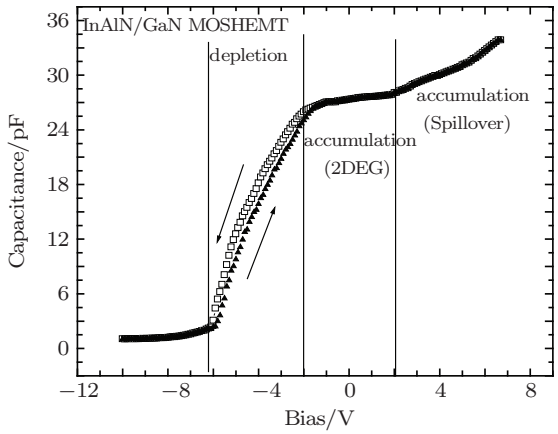


Fig. 2. The *C–V* curves measured at 1 MHz on MOS-ring capacitors.

Figure 3 shows a drastic reduction of the leakage current of the MOS structure compared with that of the Schottky barrier based structure, both at reverse bias and at forward bias. At $V_{gs} = -20$ V, the MOS gate leakage current is below 1×10^{-4} mA/mm, which is about four orders of magnitude lower than that of the SB HEMT. From the MOS I–V breakdown at 3.8 V, we roughly estimate the oxides electrical strength to be 3.8 MV/cm, which is consistent with the above experimental result.

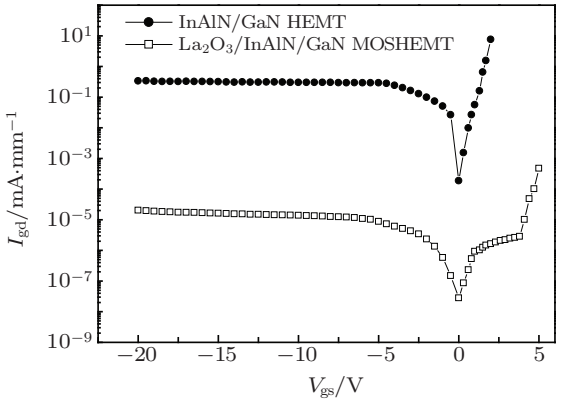


Fig. 3. Gate leakage currents of La_2O_3/InAlN/GaN MOSHEMT and InAlN/GaN HEMT.

Figure 4 shows the output characteristics of the La_2O_3/InAlN/GaN MOSHEMT and InAlN/GaN HEMT devices each with a gate length L_g of 1 μm, gate width W_g of 100 μm, and source-drain spacing of 6 μm. For the MOSHEMT device, the gate bias voltage is increased up from −6 V to +4 V in 2 V step and the maximum drain current is approximately 961 mA/mm when V_{gs} is +4 V. For the InAlN/GaN HEMT device, the gate bias voltage varies from −5 V to +1 V in 2 V step and the maximum drain current is approximately 710 mA/mm when V_{gs} is +1 V. The maximum drain current of the MOSHEMT with a gate dielectric of La_2O_3 is larger than that of InAlN/GaN HEMT. The pinch-off voltage and the peak transconductance (G_m) are −4.2 V and 131 mS/mm for InAlN/GaN HEMTs, and −6.0 V and 130 mS/mm for La_2O_3 MOSHEMT. The comparison of transfer characteristics between the MOSHEMT device and the HEMT device confirms that for the MOSHEMT device, despite its threshold voltage shifts after the gate insulation, the peak transconductance remains constant and a wide and uniform G_m distribution of the MOSHEMT is observed compared with that of the HEMT. We think there is an improvement on the intrinsic mobility of the HEMT due to a reduced surface depletion effect below the gate although the insertion of a high-k insulator, causing an effective modulation distance in the depletion region between the metal gate and the channel to increase.[18] When the gate voltage swing is defined as the value at the 10% drop of the maximum transconductance, the gate voltage swing is 4.7 V for the MOSHEMT and 2.4 V for thr InAlN/GaN HEMT. Compared with the Schottky-gate HEMT, the MOSHEMT has a larger gate voltage swing, thereby suggesting that it has better linear behaviour.

The threshold voltage of the MOSHEMT as a function of temperature was measured as shown in Fig. 5(a). The threshold voltage shows a decrease as temperature increases. However, the temperature change at $T \geq 150$ °C is significantly large ($\Delta V_{th} = -9.2$ mV/°C). Temperature dependence of the threshold voltage can be used to analyse the influence of trap on the performance of the MOSHEMT device. The threshold voltage is described as $V_{th} = \phi_b - \Delta E_C - (qn_{tot}d/2\varepsilon_r\varepsilon_0)$, where ϕ_b is the barrier height (i.e., the surface potential), ΔE_C is the conduction band discontinuity, d is the barrier–channel distance, and $\varepsilon_r\varepsilon_0$ is the dielectric constant. The total carrier density n_{tot} is a sum of the density of shallow carriers and the density of carrier traps, i.e., $n_{tot} = n_s + n_T$. The barrier height ϕ_b can be considered as a constant in the temperature range used. Temperature dependence of ΔE_C for the InAlN/GaN can be neglected, as the band gaps of the GaN and InAlN show nearly identical temperature dependence.[18] From the recent studies dealing with the transport properties of the InAlN/GaN heterostrucuture at higher temperatures it follows that the sheet charge density n_s is nearly constant in the temperature range between room temperature and 500 °C.[19] Thus the temperature dependence of the threshold voltage is given predominantly by thermal activation of the traps. The threshold voltage shift with temperature can be expressed as $\Delta V_{th} = qn_T d/2\varepsilon_r\varepsilon_0$. The trap density is evaluated using data shown in Fig. 5(a) under the assumption of $\varepsilon_r = 8.5$ and 17.3 for InAlN and La_2O_3 respectively. The result for the MOSHEMT is shown using an Arhenius plot in Fig. 5(b). The trap density increases with temperature and it is about 5.2×10^{11} cm^{-2} at room temperature, which is consistent with the C–V measurement results.

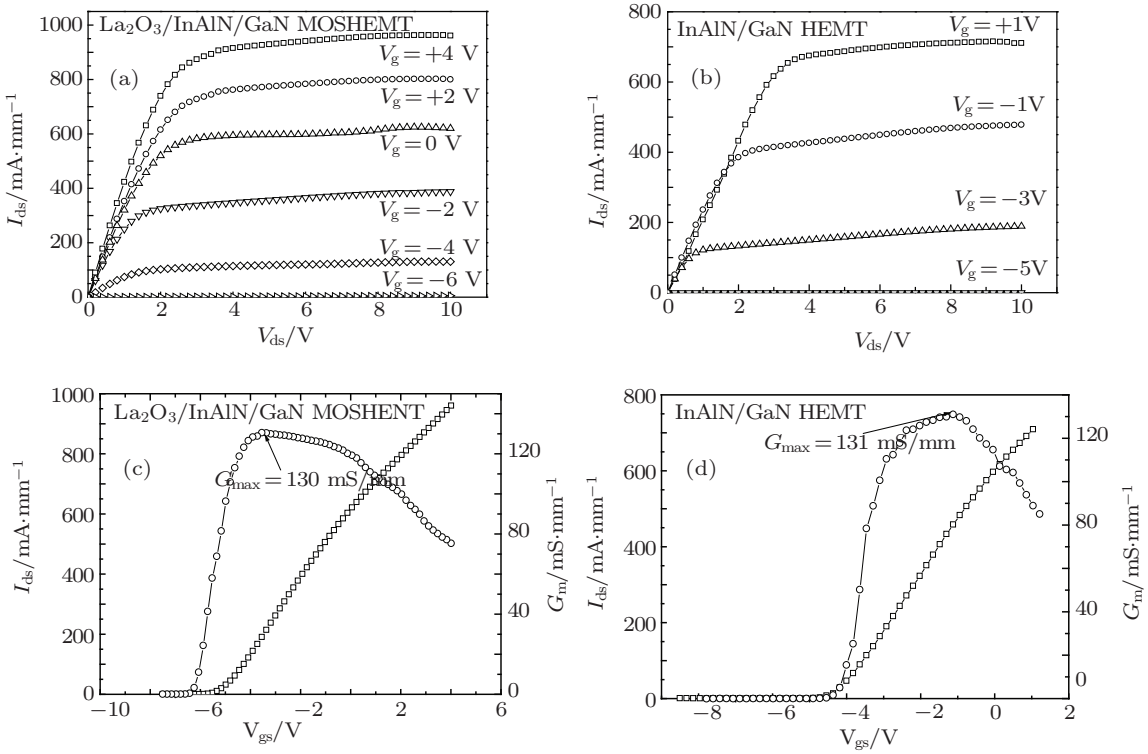


Fig. 4. Output characteristics of the La_2O_3/InAlN/GaN MOSHEMT (a) and the InAlN/GaN HEMT (b); transconductance characteristics of La_2O_3/InAlN/GaN MOSHEMT (c), and InAlN/GaN HEMT (d).

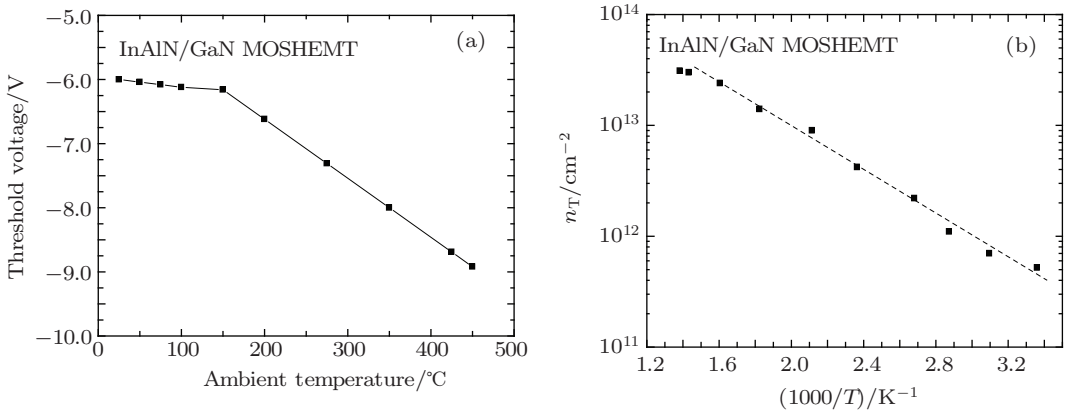


Fig. 5. Threshold voltage of the InAlN/GaN MOSHEMT versus ambient temperature (a), and trap density versus temperature evaluated from the threshold voltage shift for the InAlN/GaN MOSHEMT (b).

Current collapse is also characterized by gate pulsed measurement (also called gate-lag measurement). The pulse period and pulse width are 10 ms and 1 ms, respectively. The quiescent bias point is V_{ds} = 10 V and V_{gs} = −6 V for MOSHEMT and V_{gs} = −5 V for HEMT device, which keep the devices under off-state conditions and keep the Id between the source and the drain neglected and no hot electrons produced, but the electric field between the gate and the drain is very large. During the measurement, the drain bias was swept from 0 V to 10 V, and the gate electrode was pulsed from its quiescent value to V_{gs} voltage. For the HEMT device (Fig. 6(b)), current collapse phenomena are noticeable, leading to a 40% drain current discrepancy between the DC mode and the pulsed mode (for V_{ds} = 10 V and V_{gs} = 1 V). Due to no hot electrons, the current collapse cannot be induced by traps in the GaN buffer layer. As is well known, the spontaneous polarization effects lead to charge sheets of opposite polarity at the top and bottom surfaces of the InAlN layer in an InAlN/GaN heterostructure respectively. The existence of such a polarization dipole alone is not sufficient for a 2DEG to form in the GaN channel, so a positive sheet charge, acting as donor like traps, at the free InAlN surface must exist in order that a 2DEG is present in the GaN channel. So we suppose that the current collapse is induced by surface states on the InAlN surface. In order

to analyse the current collapse mechanism, we simulate the electric field distribution as shown in Fig. 7(a), where these appears to be a peak at the gate edge toward the drain electrode. During measurements, the device is in a deep depletion and the gate electrode is in the reverse bias condition and the current can be expressed as

$$J = A^* T^2 \exp\left(-\frac{qV_{\rm D} - q\Delta\phi}{k_0 T}\right) \times \left[\exp\left(-\frac{qV_{\rm dg}}{k_0 T}\right) - 1\right], \quad (1)$$

where A^* is Richardson constant, T is the absolute temperature, $\Delta\phi$ is the barrier variation induced by the tunnel effect and

$$q\Delta\Phi \approx \left[\frac{2q^3 N_{\rm D}}{\varepsilon}(V_{\rm D} - V_{\rm dg})\right]^{1/2}, \quad (2)$$

where $x_{\rm c}$ is the critical barrier thickness. Due to a lot of surface states at the free InAlN surface, electrons flowing from the gate to the drain are trapped by the surface state at the position of the gate edge toward the drain electrode, the number of trapped electrons in the period t can be expressed as

$$N = \frac{S\int_0^t J(t)\,{\rm d}\tau}{q} \times k, \quad (3)$$

where $S = L_{\rm g} \times W$ is the gate area, k is the number ratio of the trapped electrons to the total electrons, then the electron concentration on the InAlN surface is equal to

$$n = \frac{N}{L_{\rm gd} \cdot W \cdot d_{\rm t}}, \quad (4)$$

where $d_{\rm t}$ is the thickness of the surface trapping layer. According to Eq. (1), if $V_{\rm dg}$ is large to some extent, the gate reverse current will increase rapidly and then more electrons can be trapped by surface states and the surface potential becomes more negative, thereby depleting the channel of electrons and finally leading to the decrease of drain current (Fig. 7(b). For the MOSHEMT device (Fig. 6(a)), there is no significant current collapse observed in pulse curves and no $I_{\rm d}$ reduction of pulsed curves in the saturation region either. We consider that the La_2O_3 film can reduce the surface state density between the gate and drain, in addition, the La_2O_3 based insulated gate structure can reduce the gate leakage current remarkably (Fig. 3). Thus, the La_2O_3-based MOSHEMT structure and surface passivation are very effective for suppressing the current collapse.

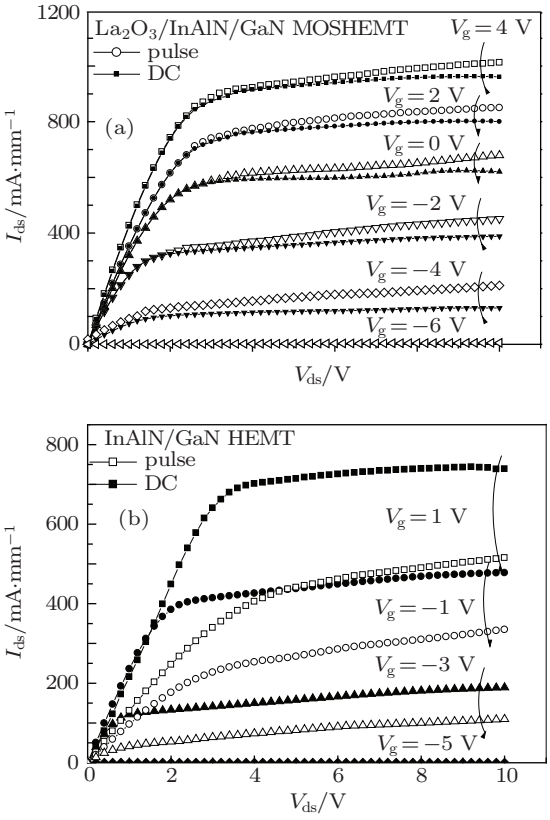


Fig. 6. The DC and pulsed I–V characteristics of the La_2O_3/InAlN/GaN MOSHEMT (a) and the InAlN/GaN HEMT (b).

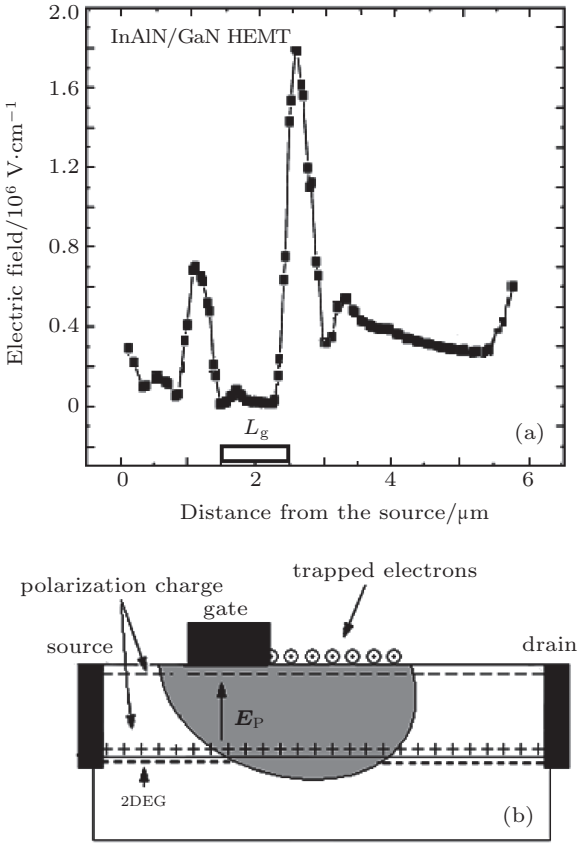


Fig. 7. Electric field distribution of the InAlN/GaN HEMT (a) and the electron trapped in surface state on the InAlN surface (b).

The high-frequency performances of these devices were characterized from 1 GHz to 40 GHz using a network analyzer (Fig. 8). The La_2O_3/InAlN/GaN MOSHEMT device is biased at $V_{ds} = 10$ V and $V_{gs} = -3.5$ V, the cut-off frequency (f_t) and unilateral gain cut-off frequency (f_{max}) are 10.9 GHz and 21.6 GHz respectively. For the InAlN/GaN HEMT device, the bias voltages are $V_{ds} = 10$ V and $V_{gs} = -1.1$ V, the cutoff frequency (f_t) and unilateral gain cut-off frequency (f_{max}) are 10.7 GHz and 22.2 GHz respectively.

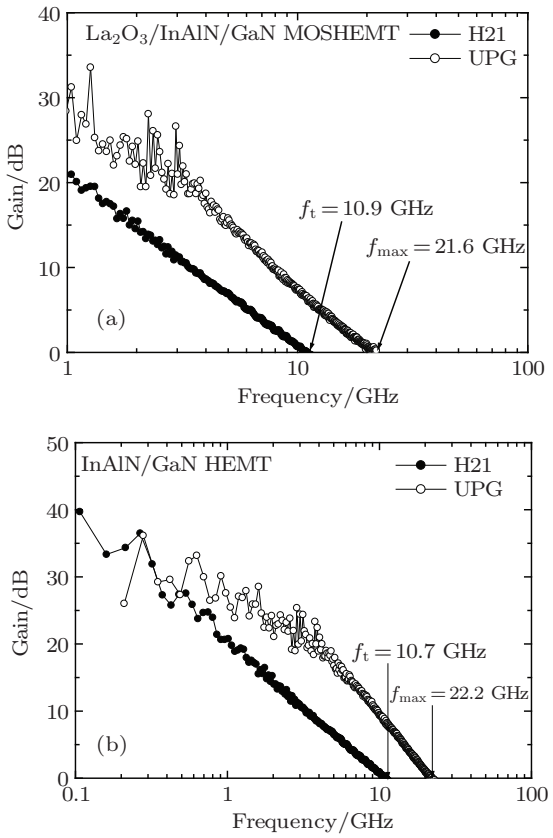


Fig. 8. The RF performances of the La_2O_3/InAlN/GaN MOSHEMT (a) and InAlN/GaN HEMT (b).

4. Conclusion

We have fabricated the La_2O_3/ InAlN/GaN MOSHEMTs and the InAlN/GaN HEMTs on the same wafer. For the MOSHEMT, we obtained a drain current of 961 mA/mm at $V_{gs} = 4$ V and $V_{ds} = 10$ V which is higher than 710 mA/mm at $V_{gs} = 1$ V and $V_{ds} = 10$ V for the HEMT. Furthermore, the gate leakage current is four orders of magnitude smaller than that of the HEMT, a large gate voltage swing, negligible current collapse, and almost equal peak transconductance were also achieved. These results demonstrate the large potential of the La_2O_3/InAlN/GaN MOSHEMT for high power and high frequency applications.

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