A GaAs planar Schottky varactor diode for left-handed nonlinear transmission line applications*

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The left-handed nonlinear transmission line (LH–NLTL) based on monolithic microwave integrated circuit (MMIC) technology possesses significant advantages such as wide frequency band, high operating frequency, high conversion efficiency, and applications in millimeter and submillimeter wave frequency multiplier. The planar Schottky varactor diode (PSVD) is a major limitation to the performance of the LH–NLTL frequency multiplier as a nonlinear component. The design and the fabrication of the diode for such an application are presented. An accurate large-signal model of the diode is proposed. A 16 GHz–39.6 GHz LH–NLTL frequency doubler using our large-signal model is reported for the first time. The measured maximum output powers of the 2nd harmonic are up to 8 dBm at 26.4 GHz, and above 0 dBm from 16 GHz to 39.6 GHz when the input power is 20 dBm. The application of the LH–NLTL frequency doubler furthermore validates the accuracy of the large-signal model of the PSVD.

Keywords: GaAs, planar Schottky varactor diode, left-handed nonlinear transmission lines, frequency doubler

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1. Introduction

Veselago[1] first proposed left-handed materials (LHMs) in 1968, which are materials with simultaneous negative permittivity (ε) and permeability (μ). Veselago theoretically illuminated the unique electromagnetic properties of LHMs such as the reversal of the Snell's law, the Doppler effect, the Vavilov Cerenkov effect, and supporting backward waves which are the waves with antiparallel group velocities and phase velocities. LHMs have received substantial attention in scientific and engineering communities due to their unique electromagnetic properties.[2−5] Subsequently, Kozyrev and van der Weide[6,7] introduced nonlinear transmission lines based on left-handed media, the unit cell consists of series varactors and shunt inductors, which is a dual conventional nonlinear transmission line. Compared with the dual conventional nonlinear transmission line (NLTL), the left-handed nonlinear transmission line (LH–NLTL) can effectively generate a harmonic that has a wide frequency band and a relatively high operating frequency. In view of the advantages, the LH–NLTLs have significant potential applications in highly efficient powerful frequency multipliers.[8]

Varactor diode is an important element in the LH–NLTL frequency multiplier as a nonlinear voltage-variable capacitor. Considering the sharp C–V characteristic and compatibility with the standard MMIC process, the planar Schottky varactor diode (PSVD) is an appropriate candidate for the application of the LH–NLTL frequency multiplier. In addition, the low series resistance of the PSVD can provide high operating frequency.

In this paper, a PSVD is fabricated based on monolithic microwave integrated circuit (MMIC) technology. A 16 GHz–39.6 GHz LH–NLTL frequency doubler is developed based on our large-signal model of the PSVD for the first time. The rest of the present paper is organized as follows. The structure and the design of the PSVD are discussed in Section 2. The fabrication of the PSVD is indicated in Section 3. The measurements and modeling of the PSVD are presented in Section 4. In Sections 5, the behaviours of the LH–NLTL frequency multiplier with PSVD are discussed. A brief conclusion is drawn in Section 6.

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2. Design of structure

A schematic diagram of the PSVD is shown in Fig. 1. The device consists of three layers: a GaAs barrier layer, a GaAs highly doped layer (n^+-type layer) and the GaAs semi-insulation substrate.

The Schottky contact is formed between the contact-metal and the GaAs barrier layer. The contact capacitance is approximately represented by

$$C_{\rm T} = A\sqrt{\varepsilon_s \varepsilon_0 q N_{\rm D}/2(V_{\rm D} + V_{\rm R})}, \qquad (1)$$

where A represents the area of the Schottky contact, ε_s the relative permittivity of GaAs, ε_0 the vacuum permittivity, q the charge of electron, $N_{\rm D}$ the n-type doping density of the barrier layer, $V_{\rm D}$ the contact electric-potential, and $V_{\rm R}$ the reverse bias voltage.

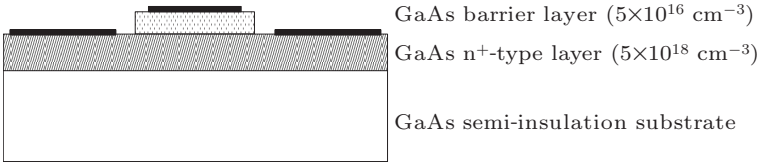


Fig. 1. Schematic diagram of the PSVD.

The contact capacitance ($C_{\rm T}$) is determined primarily by the doping density ($N_{\rm D}$) of the barrier layer. The characteristics of the capacitance versus reverse bias voltage for the 0.6 μm-thick barrier layers with different doping densities are simulated in silvaco (a TCAD tool). The doping density ($N_{\rm D}$) varies from 1×10^{15} cm^{-3} to 5×10^{17} cm^{-3}. The simulated results including the zero-bias capacitance (C_{j0}), the minimal capacitance ($C_{\rm min}$), the ratio of the zero-bias capacitance, and the minimal capacitance (capacitance-ratio) are shown in Table 1.

Table 1. Simulation results of barrier layers with different doping densities.

$N_{\rm D}$/cm^{-3}	C_{j0}/fF	$C_{\rm min}$/fF	Capacitance-ratio
1×10^{15}	0.2139	0.1946	1.1
5×10^{15}	0.2681	0.1948	1.38
1×10^{16}	0.364	0.1949	1.87
5×10^{16}	0.7903	0.1964	4
1×10^{17}	1.104	0.2435	4.53
5×10^{17}	2.405	0.5448	4.4

The capacitance ratio is big enough with the $N_{\rm D}$ being more than 5×10^{16} cm^{-3}. The higher $N_{\rm D}$ of the barrier layer brings higher zeao-bias capacitance, nevertheless the high $N_{\rm D}$ will increase the probability of the tunneling effect, and thus the leakage current. So, the value of 5×10^{16} cm^{-3} for $N_{\rm D}$ is chosen to ensure the high capacitance-ratio and low leakage current. The final thickness and doping density of the layers are shown in Table 2.

Table 2. Thicknesses and doping densities of the layers.

	Thickness/μm	Doping/cm^{-3}
Barrier layer	0.6	5×10^{16}
n^+-type layer	1	5×10^{18}

The 0.6 μm-thickness of the barrier layer is chosen to reduce the parasitic series resistance.[9] The doping density of the n^+-type layer is 5×10^{18} cm^{-3}, which is optimized for better Ohmic contact, and the

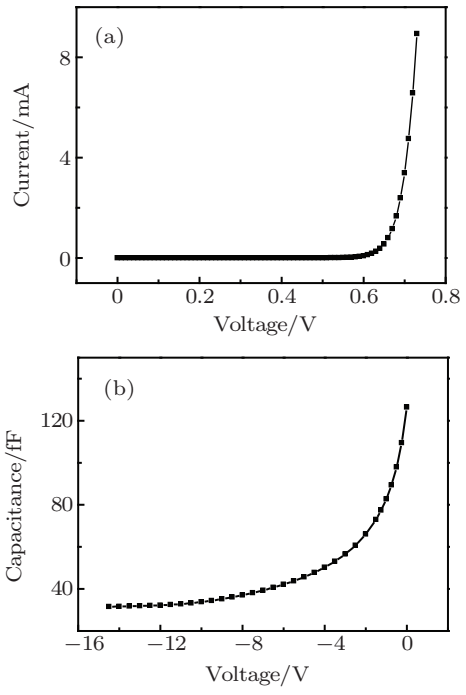


Fig. 2. Simulated characteristics of the forward current (a) and reverse capacitance (b) versus applied voltage of the PSVD.

1-μm thick n^+-type layer simultaneously provides a lower parasitical resistance and simpler process. The dc and ac characteristics of the device are simulated by silvaco, which is set to be a workfunction of 4.9 eV for the Schottky contact. The characteristics of the capacitance and the current versus applied voltage are simulated, the results are shown in Fig. 2.

3. Fabrication of device

The GaAs epilayers were grown by molecular beam epitaxy (MBE) on GaAs semi-insulating substrate, which consisted of 1-μm thick conductivity buried n^+-type layer and 0.6-μm-thick n-type barrier layer. The dopant in epilayers was silicon. To begin with, 0.7-μm thick mesa was formed from the barrier layer to the n^+-type layer by wet etching using the solution of $H_3PO_4/H_2O_2/H_2O$. The Ohmic contacts were then formed by lift-off of e-beam evaporated Ni/Ge/Au/Ge/Ni/Au followed by annealing. After annealing, the Schottky contacts were then formed by lift-off of e-beam evaporated Ti/Pt/Au. Using the solution of the $H_3PO_4/H_2O_2/H_2O$, a wet etching removed the GaAs materials from n^+-type layer to the substrate layer surrounding the Ohmic contact regions, thus isolating the devices. The whole surface of the wafer was then passivated by depositing 3000-Å thick silicon nitride. Using reactive ion etching, windows were opened over the metal contacts. Finally, the pads and fingers were electroplated to connect to Schottky or Ohmic contact metal.

The isolation between devices is formed by the mesa which was etched into a semi-insulating substrate layer. Low parasitical capacitance and resistance can be obtained. The photo of the device, which has a single finger and an anode area of 160 μm^2, is shown in Fig. 3.

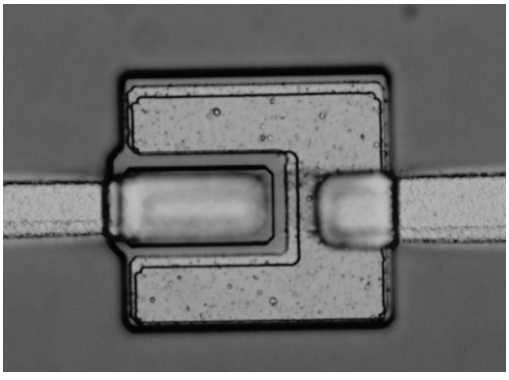


Fig. 3. Photo of the PSVD chip.

4. Measurement and modeling of PSVD

The dc characteristics of the PSVDs were measured using an HP 4155 semiconductor parameter analyzer. The comparison between the measured I–V characteristics and the simulated ones of the current biased voltages from −0.5 V to 0.75 V are shown in Fig. 4(a). I_s and n, which are 1.71×10^{-15} A and 1.05, respectively, are extracted from the experimental curve. The measured curve of the forward current is approximately the same as the simulated curve. The break-down characteristics of the diode are shown in Fig. 4(b). The measured break-down voltage of the PSVD is −17 V, which is an impressive result for a Schottky diode. The good break-down performance results from the thick n^+-type layer which forms a fine Shottky contact barrier and the reasonable process.

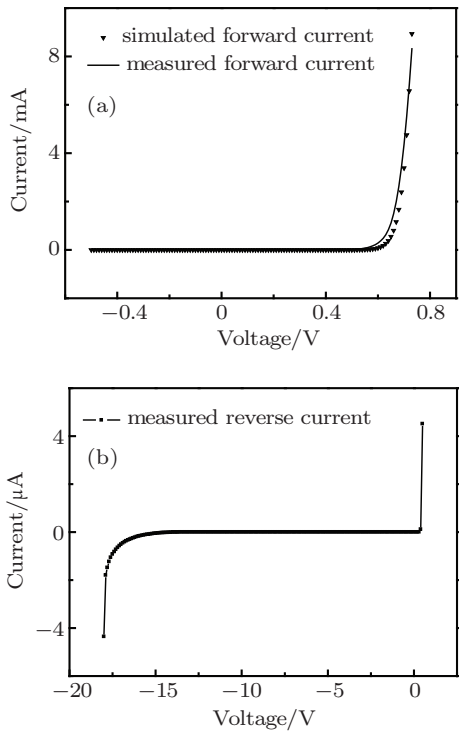


Fig. 4. Characteristics of the forward current (a) and the reverse current (b) of the PSVD.

The characteristics of the capacitance versus reverse applied voltage are measured using an Agilent 4284A precision LCR meter with a local oscillator voltage between −9.8 V and 0 V and an excitation frequency of 1 MHz. The comparison between measured characteristics of the reverse capacitance and the simulated results are shown in Fig. 5. It can be concluded that the measured capacitances biased at 0 V (C_{j0}) and −9.8 V ($C_{\min}$) are 130 fF and 50 fF respectively,

the ratio of the variable capacitance ($C_{\max}/C_{\min}$) is 2.6. The measured curve of the reverse capacitances exceeds the simulated one slightly. The deviation comes from the parasitic side-wall capacitances.

The S-parameters are measured using a probe station and an Agilent PNA E8363B automatic network analyzer between 0.1 GHz and 40 GHz. The device is biased at 11 different points from 0 V to −10 V in steps of 1 V. The real and the imaginary parts of the S_{11} and S_{12} de-embeded in advanced design system (ADS) are shown in Figs. 6(a)–6(d).

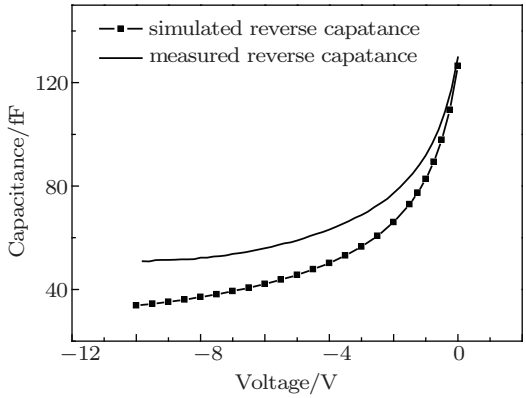


Fig. 5. Comparison between the curves of measured and simulated capacitances versus applied voltage.

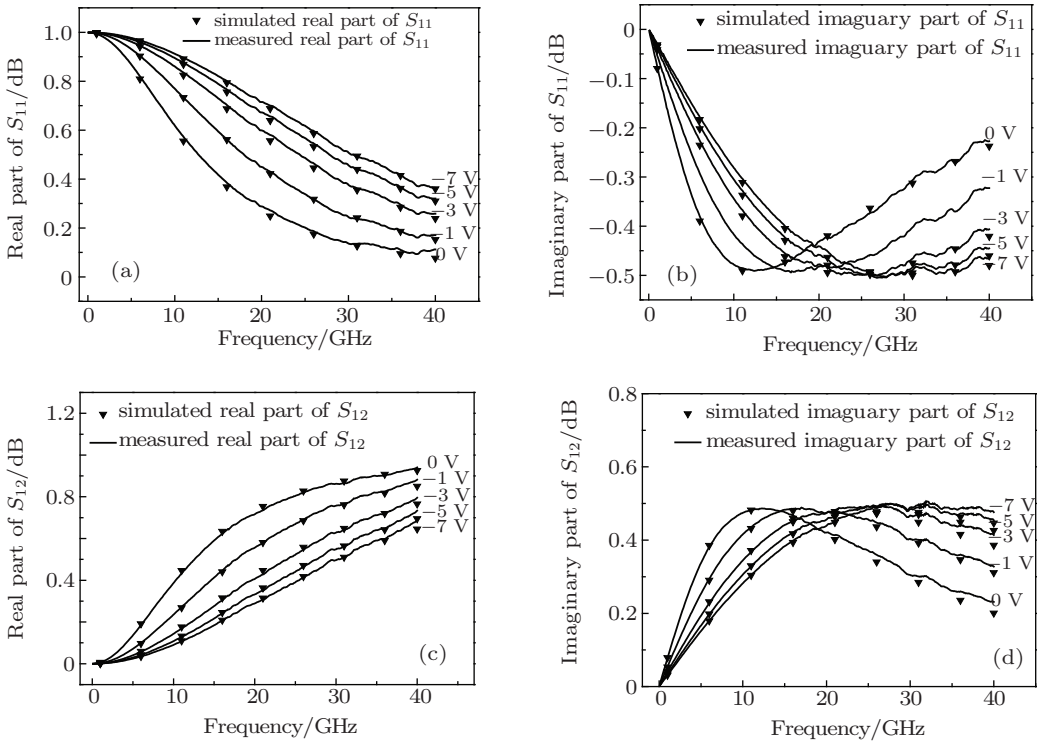


Fig. 6. Comparison between measured and simulated S-parameters of the PSVDs. Panel (a) is for the real part of the S_{11}, panel (b) for the imaginary part of the S_{11}, panel (c) for the real part of the S_{12} and panel (d) for the imaginary part of the S_{12}.

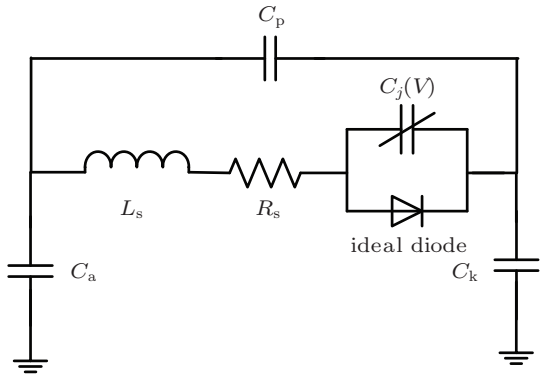


Fig. 7. Topology schematic of the model of PSVD.

The equivalent circuit of the PSVD is presented in Fig. 7.[10] The conduction and the capacitance of the junction are represented by ideal diode and $C_j(V)$ respectively. The ideal diode is effectively open circuit with reverse bias. The parasitic series resistance composed of the undepleted part of the barrier layer underneath the Schottky contact, the bulk resistance of n^+-type layer and the Ohmic contact resistance is represented by R_s. Here R_s is approximately considered to be bias-independent. The anode and the cathode pad parasitic capacitances with respect to ground are represented by C_a and C_k respectively. The par-

asitic capacitance between contacts is represented by $C_{\rm p}$. The parasitic series inductance of the pads and fingers is represented by $L_{\rm s}$. The $C_{\rm a}$, $C_{\rm k}$, $C_{\rm p}$, and $L_{\rm s}$ are essentially independent of bias.

The parameters $I_{\rm s}$ and n of the ideal diode confirmed by the measured I–V curves are 1.71×10^{-15} A and 1.05 respectively. The values of $R_{\rm s}$, $L_{\rm s}$, $C_{\rm a}$, $C_{\rm k}$, and $C_{\rm p}$ are extracted by fitting the simulated curves of S_{11} and S_{12} to the measured ones at zero bias. Having known the bias independent parameters, we can easily extract the $C_j(V)$ from the measured S-parameters at different bias voltages. The extracted results of the bias independent parameters are shown in Table 3. The extracted characteristics of the $C_j(V)$ are represented by a polynomial capacitance which is dependent on applied voltage.

Table 3. Extracted results of the bias independent parameters.

$L_{\rm s}$/nH	$R_{\rm s}/\Omega$	$C_{\rm p}$/fF	$C_{\rm a}$/fF	$C_{\rm k}$/fF
0.03	2.4	5	1	2

The model is simulated in ADS with frequencies from 0.1 GHz to 40 GHz in steps of 0.1 GHz, with bias voltage varied from 0 V to −10 V. The simulated S_{11} and S_{12} results are shown in Fig. 6, which is consistent with the measured data. The accurate large-signal model will be validated by the LH–NLTL circuit.

5. Design of LH–NLTL frequency multiplier

The equivalent circuit of LH–NLTL is shown in Fig. 8. The LH–NLTL consists of periodic shunt inductance and series nonlinear capacitance. Two constant capacitances are connected to the input and output ports to restrict dc signals. The value of shunt inductance is constant, and the series nonlinear capacitance is represented by a varactor, which is implemented by PSVDs in our paper.

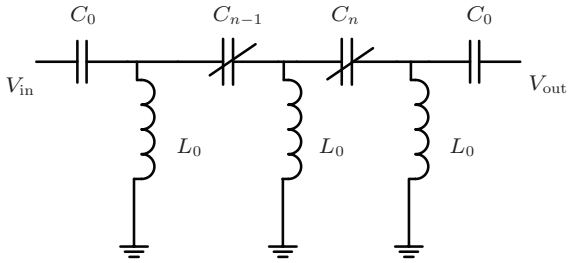


Fig. 8. Equivalent circuit of LH–NLTL.

A 16 GHz–39.6 GHz LH–NLTL frequency doubler based on the PSVDs is designed and fabricated. The schematic diagram of the doubler is shown in Fig. 9. The invariable capacitance C_0 and inductance L_0 are respectively 0.24 pF and 2.5 nH. The nonlinear capacitances are implemented by the PSVD discussed above. Its zero-bias capacitance is 130 fF, the ratio of the variable capacitance ($C_{\rm max}/C_{\rm min}$) is 2.6. The $R_{\rm d}$ which is the parasitic series resistance of the PSVD is 2.4 Ω.

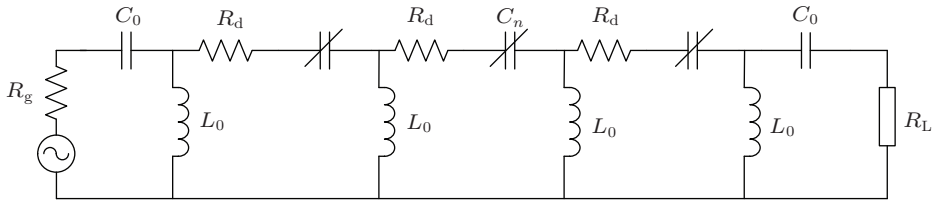


Fig. 9. Circuit schematic diagram of the 16 GHz–39.6 GHz LH–NLTL frequency doubler.

The S-parameters are measured with the network analyzer E8363B from 0.1 GHz to 40 GHz with a −17-dBm input signal. The simulated and measured values of S_{11} and S_{21} are shown in Fig. 10. The measured results of S_{11} and S_{21} are quite coincident with the curves of the simulation results. The coincidence validates the small-signal accuracy of the equivalent circuit model of the PSVD. Unlike the conventional NLTL, the amplitude of the S_{12} versus input frequency for the LH–NLTLs exhibit high-pass characteristics, which is more preferable for the application of the frequency multiplier in a high frequency range.[6]

The 2nd harmonic output power of the LH–NLTL

frequency doubler is measured by a 43-GHz frequency spectrum analyzer and probe station with 20-dBm input power from a sinusoidal signal generator. The frequency of the input signal is scanned from 4 GHz to 21.5 GHz. The test platform is calibrated by a vector network analyzer. The measured results of the 2nd harmonic output power are shown in Fig. 11 and compared with the simulated results. The measured maximal output power of the 2nd harmonic is up to 8 dBm at 26.4 GHz at times. The measured output power of the 2nd harmonic is above 0 dBm from 16 GHz to 39.6 GHz. The measured curve basically accords with the simulated curve except for one point, which is the lowest notch in the simulated curve. The notch point corresponds to the condition of the minimal second harmonic output power.[11] The disparity between the measured curve and simulated curve at the notch point comes from fact that the series inductor and shunt varactor were not ideal. The measurement of the harmonic furthermore validates the large-signal characteristics of the model of the PSVD.

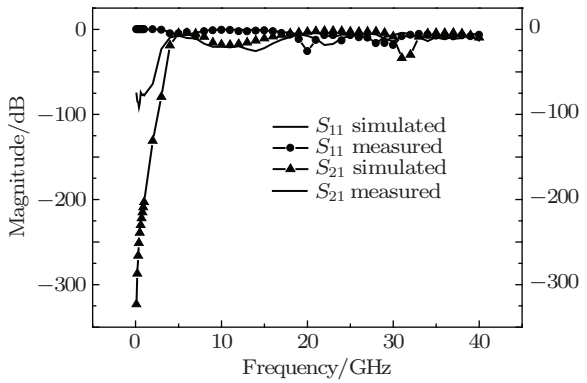


Fig. 10. Comparison between the simulated and the measured S-parameters of the LH–NLTL frequency doubler.

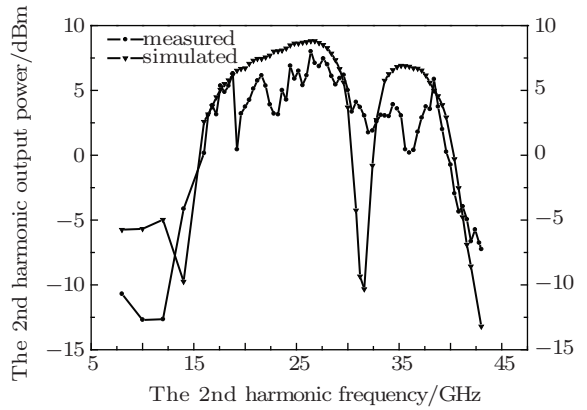


Fig. 11. Measured results of the 2nd harmonic output power.

6. Conclusions

LH–NLTL has high pass characteristics and possesses the advantages of a wide frequency band, a high operating frequency, a high conversion efficiency and applications in the millimeter and submillimeter wave frequency multiplier. A GaAs PSVD is fabricated as the nonlinear capacitance in LH–NLTL using the mesa isolation process. The zero bias capacitance and the variable capacitance ratio are measured to be 130 fF and 2.6. An accurate large-signal model of the PSVD is proposed to apply to the design of LH–NLTL. A 16 GHz–39.6 GHz LH–NLTL frequency doubler is designed. The measured maximal output powers of the 2nd harmonic are up to 8 dBm at 26.4 GHz, and above 0 dBm from 16 GHz to 39.6 GHz when the input power is 20 dBm. The GaAs PSVD which is designed and fabricated in our work is successfully applied to the design of the LH–NLTL frequency doubler. The measurement of the LH–NLTL frequency doubler at the same time validates the accuracy of the large-signal model of the PSVD.

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