Effects of microwave pulse-width damage on a bipolar transistor*

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This paper presents a theoretical study of the pulse-width effects on the damage process of a typical bipolar transistor caused by high power microwaves (HPMs) through the injection approach. The dependences of the microwave damage power, P, and the absorbed energy, E, required to cause the device failure on the pulse width τ are obtained in the nanosecond region by utilizing the curve fitting method. A comparison of the microwave pulse damage data and the existing dc pulse damage data for the same transistor is carried out. By means of a two-dimensional simulator, ISE-TCAD, the internal damage processes of the device caused by microwave voltage signals and dc pulse voltage signals are analyzed comparatively. The simulation results suggest that the temperature-rising positions of the device induced by the microwaves in the negative and positive half periods are different, while only one hot spot exists under the injection of dc pulses. The results demonstrate that the microwave damage power threshold and the absorbed energy must exceed the dc pulse power threshold and the absorbed energy, respectively. The dc pulse damage data may be useful as a lower bound for microwave pulse damage data.

Keywords: bipolar transistor, high power microwave, pulse width effects

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1. Introduction

Currently, there has been increasing interest in understanding the effects of electromagnetic interference (EMI) on electronic systems caused by high power microwaves (HPMs).[1−9] Such HPMs can produce high-amplitude current pulses and high-amplitude voltage pulses with a time duration of several nanoseconds or even tens of nanoseconds in electronic systems. In general, the semiconductor components that make up systems are most susceptible to damage by the induced transient.

Earlier studies on the HPM susceptibility of the integrated circuit and device focused on the statistical analysis of the threshold characteristics. Experimental investigations on the vulnerability of the electrified railway system from HPM source have shown that a low-noise amplifier (LNA) is vulnerable to permanent damage and its destruction threshold levels decrease with the time duration of microsecond pulses.[10] Experimental studies on the microwave vulnerability effect of CMOS inverters[11] and the integrated circuit[12] have shown that the injected pulse power threshold is inversely proportional to the pulse width. The microwave injected test of a radio link system demonstrated that the input transistor is vulnerable to damage and the pulse energy is directly proportional to the pulse width.[1] All the experimental investigations indicate that the study of pulse-width effects is one of the most important tasks in the research on the electromagnetic susceptibility of electronic systems. However, few attempts have been made to theoretically study HPM pulse-width effects. Specifically, there is a particular lack at the device failure level for microwave nanosecond pulses. At present, the investigations into semiconductor device degradation or failure focus on the effects induced by high-power dc pulses.[13−18] These investigations have provided useful information on the dc pulse power and energy required to cause semiconductor device degradation or failure as a function of the dc pulse duration. Unfortunately, few studies have been done on the comparison of the microwave pulse failure data with the existing dc pulse failure data, which may be useful in predicting the microwave power threshold and the absorbed energy required to cause device burnout in semicon-

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ductor devices of the same type.

In this paper, a two-dimensional (2-D) electro-thermal model of a typical bipolar transistor (BJT) is established with the device simulator ISE-TCAD. One of our objectives is to study the microwave pulse-width effects of a typical bipolar transistor in the nanosecond-pulse region by using the direct injection approach, and establish the relationships of the microwave damage power P and the damage energy E with the pulse width τ. Our second objective is to compare our microwave nanosecond pulse data with the existing dc nanosecond pulse data for the bipolar transistor, and make order-of-magnitude estimates of the microwave failure level as a function of pulse length for the same transistor.

2. Structure and model

2.1. Device structure

A schematic diagram of the typical silicon n^+-p-n-n^+ epitaxial planar transistor used in our calculations is illustrated in Fig. 1, and only half of the transistor with interdigitated structure is analyzed considering the geometrical symmetry. The bulk of the transistor is a 200-μm n^+ collector substrate, above which is a 2-μm n-type epitaxial collector region. The collector metallization is shown below the substrate. B, C, and E represent its base, collector, and emitter contacts, respectively. N^+ denotes the heavily doped regions of the n-type silicon, and P the p-type base region. The doping profile of the transistor is given in Fig. 2. The thermal electrode is specified at the bottom of the transistor where the lattice temperature is assumed to be a constant (T_0 = 300 K). The upper surface (along line $y = 0$) and the sidewall boundaries (along lines $x = 0$ and $x = 10$ μm) are thermally insulated from the environment, i.e.,

$$\partial T/\partial y|_{y=0} = 0, \tag{1}$$

$$\partial T/\partial x|_{x=0,10} = 0. \tag{2}$$

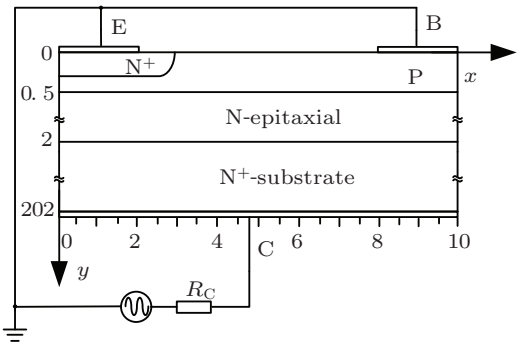


Fig. 1. The device structure of an n^+-p-n-n^+ transistor and a schematic diagram of the circuit used in the numerical simulations.

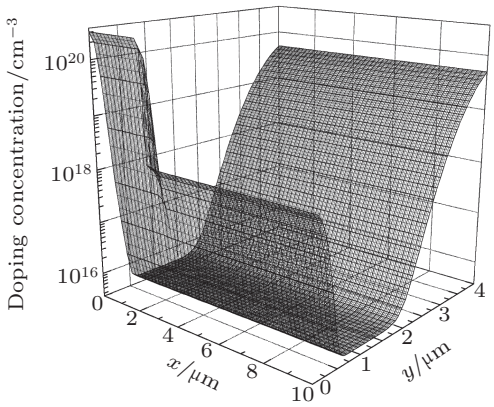


Fig. 2. Doping distribution for BJT (along line $x = 1$, for $y = [0, 4]$).

2.2. Numerical modeling

To investigate the pulse-width effects of the bipolar transistor, the advanced mixed mode device and circuit simulator ISE-DESSIS are employed, which compute the electrical behavior of the device by iteratively solving the Poisson equation and the current-continuity equations.[19] During the injection of microwaves, the presences of high current and high voltage cause a huge joule heat in the device regions, which may lead to a significant rise in temperature. Hence, we should take the electro-thermal effects into account to improve the calculation precision.[20] In this paper, the thermodynamic model is adopted assuming that the charge carriers are in thermal equilibrium with the lattice, and the three basic semiconductor equations should also account for thermal effects. To obtain a nonuniform temperature distribution, the internal self heating is taken into account by solving the heat flow equation

$$\begin{aligned} & c\frac{\partial T}{\partial t} - \nabla \cdot \kappa \nabla T \\ = & -\nabla \cdot [(P_{\rm n}T + \phi_{\rm n})\boldsymbol{J}_{\rm p} + (P_{\rm p}T + \phi_{\rm p})\boldsymbol{J}_{\rm p}] \\ & - \left(E_{\rm C} + \frac{3}{2}k_{\rm B}T\right)\nabla \cdot \boldsymbol{J}_{\rm n} \\ & - \left(E_{\rm V} - \frac{3}{2}k_{\rm B}T\right)\nabla \cdot \boldsymbol{J}_{\rm p} + qR(E_{\rm C} \\ & - E_{\rm V} + 3k_{\rm B}T), \end{aligned} \tag{3}$$

where c is the lattice heat capacity, T is the temperature, and κ is the thermal conductivity. $P_{\rm n}$ ($P_{\rm p}$) is the election (hole) absolute thermoelectric power, $\boldsymbol{J}_{\rm n}$ ($\boldsymbol{J}_{\rm p}$)

is the election (hole) current destiny, and E_C (E_V) is the conduction (valence) band energy, respectively. R denotes the recombination rate, and k_B denotes the Boltzmann constant. The different physical models used simultaneously in our simulations are the SRH, Auger and Avalanche for generation and recombination, the Masetti model for doping-dependent mobility, the Conwell–Weisskopf model for carrier–carrier scattering mobility, and the Canali model for high field saturation mobility. A more detailed description of the models can be specified in Ref. [19].

3. Results and discussion

3.1. HPM burnout power threshold versus pulse duration

A schematic representation of the simulation circuit is shown in Fig. 1. By using the two-dimensional device simulator, ISE-TCAD, device failure is indicated when the local lattice temperature reaches the melting point of silicon at 1688 K. In a previous paper we presented the damage effects and the mechanism of a bipolar transistor caused by microwaves, and found that the base-emitter junction is susceptible to damage and the device is damaged due to localized heat accumulation, which can melt the semiconductor material in a very small region of the junction.[21]

In this paper, the sinusoidal voltage signals with a frequency of 1 GHz are injected directly into the collector terminal with the emitter and the base connected to the ground. The pulse width is defined as the time duration of the injected signals before the BJT is burned out, and the damage power threshold as the maximum power during the damage process.[17,22] By changing the amplitude of the injected signals, we can control the pulse width precisely on a nanosecond scale. Based on the consideration above, the dependence of the power P required to damage the BJT on the pulse width τ is illustrated in Fig. 3. It indicates that the damage power threshold increases with the decrease in pulse width. Furthermore, there is a point of inflexion around 5 ns and the damage power threshold varies a little when the pulse width is larger than the inflexion point. Using the curve fitting method to fit the data points, it is found that the relationship of P with τ meets the following function:

$$P = 43.2\tau^{-0.94}. \quad (4)$$

As shown in Fig. 3, the correlation coefficient of Eq. (4) is 0.96, showing a high degree of fitting between the pulse width and the damage power threshold.

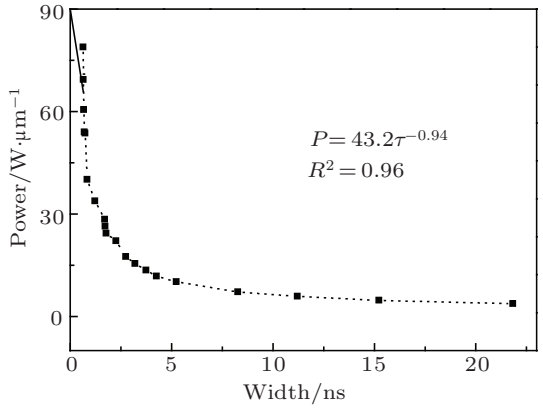


Fig. 3. HPM pulse failure power for BJT versus pulse width.

Up to now, a significant amount of work has been done in the area of high amplitude pulse-width effects on the semiconductors of electromagnetic pulse (EMP) radiation. Wunsch and Bell developed semi-empirical relationships using a linear heat flow analysis. They predicted a power per unit area versus time dependence of t^{-1} for sub-microsecond pulses, and $t^{-1/2}$ for microsecond pulses.[14] Tasca divided the device damage by the pulse width into three phases, including short pulse assuming the device is adiabatic, long pulse considering heat dissipation, and thermal equilibrium between the heat production and the thermal conduction, respectively.[18] The experimental investigations on the HPM pulse-width effects on the integrated circuit devices and equipment showed that the relationship between the pulse width and the damage power also fits the similar situation (see Fig. 4), which shows that the pulse width is shorter than 100 ns.[12] This indicates that the power (-0.94) of the equation in our simulation is slightly higher than that of the semi-empirical formula for nanosecond pulses. The semi-empirical formulas are obtained under the consideration that all of the power dissipated in the device occurs in the failure junction. However, the power dissipation exists mostly in the damaged base-emitter junction under the injection of microwaves, which will be studied in detail in the following chapter. The HPM damage power should be slightly higher than that in the ideal case for the same pulse width.

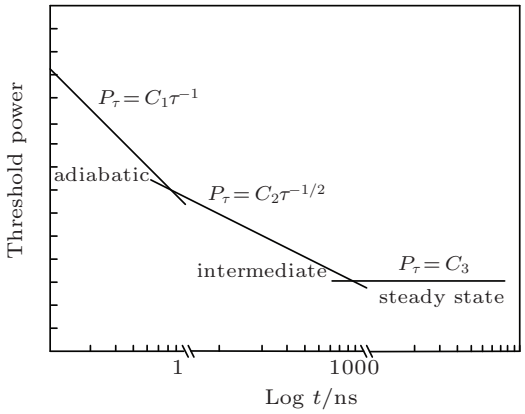


Fig. 4. Plot of damage power threshold as a function of pulse width for semiconductor devices. C_1, C_2, and C_3 are constants.

3.2. HPM and EMP burnout power threshold versus pulse duration

Several investigations into bipolar transistor failure effects and the mechanisms have been conducted with high-power dc pulses.[15−17] Researchers have studied the relation equation between the device damage power and the pulse width under different dc pulse voltages, which demonstrates that the empirical formula should be modified as follows:

$$P = 13.7\tau^{-1.4}, \tag{5}$$

where P is in units of W/μm, and τ in ns. Both the BJT structures used in Ref. [17] and the ones we represent are the same, except that the substrate of the device used in our paper is much thicker than that of the former. Since the power dissipation almost occurs in the epitaxial layer,[21] the effect of the thickness of the substrate on the damage power threshold can be ignored, which makes it meaningful to compare our HPM pulse susceptibility data with the dc pulse susceptibility data given by Ref. [17] for bipolar transistors. We note that our value C_1 (HPM) = 43.2 from the HPM nanosecond data is much higher than the value C_2 (EMP) = 13.7 from the dc nanosecond pulse data. The comparison above indicates that, for a special pulse duration, the microwave pulse power threshold must exceed the dc pulse power threshold to cause transistor failure.

Using the 2-D device simulator ISE-TCAD, we tried to discover the internal mechanism of the damage process of the bipolar transistor induced by two signals. A step voltage pulse with a rising time of 100 ps and a sinusoidal voltage signal with a frequency of 1 GHz, both of which have an amplitude of 50 V, are applied to the collector electrode, respectively, using the circuit in Fig. 1. The results are shown in Fig. 5, from which we can see that the transient temperature responses of the device under the impact of the two signals are quite different. The maximum temperature of the BJT injected by the dc pulse is linearly proportional to the duration time, while the maximum temperature of the device injected by the microwave signal increases gradually with the duration time.

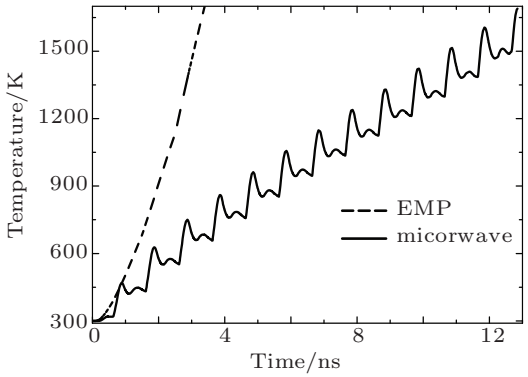


Fig. 5. Transient temperature responses of a BJT injected by a sinusoidal voltage signal and a dc pulse voltage signal.

Figure 6 shows the temperature-rising position of the device during the damage process caused by the dc pulse signal. It indicates that the hot spot that is located at the n^-–n^+ interface under the centre of the emitter is almost unchanged during the damage process until the lattice temperature reaches the melting point of silicon. However, under the injection of a microwave signal, the heating positions of the bipolar transistor for the positive and negative half periods are different (see Fig. 7). It is demonstrated that the temperature elevation occurs at the edge of the emitter region near the base in the negative half period (see Fig. 7(a)). In the positive half period, however, the heating positions are between the areas of the pn junction and the n^-–n^+ interface, and the temperature decreases at the edge of the emitter (see Fig. 7(b)). Since the power dissipation occurs mostly at the edge of the emitter, under the injection of microwave signals, the edge of the emitter near the base is damaged due to heat accumulation. It is concluded that the temperature elevation in the device is almost fixed to one place under the injection of dc pulse signal, while the hot spots change periodically under the injection of microwave signals. Part of the absorbed power is dissipated outside the damage position during the damage process induced by microwave signals. Therefore, the C_1 value of

the HPM signals is much higher than the C_2 value of the dc pulse signals for a special pulse width. Moreover, it can clearly be found that both of the damage power levels are within an order of magnitude. The comparison between the dc pulse damage power threshold and the HPM pulse damage power threshold for the typical bipolar transistor indicates that the dc nanosecond pulse data can be useful in predicting the burnout level of microwave nanosecond pulses for the same transistor.

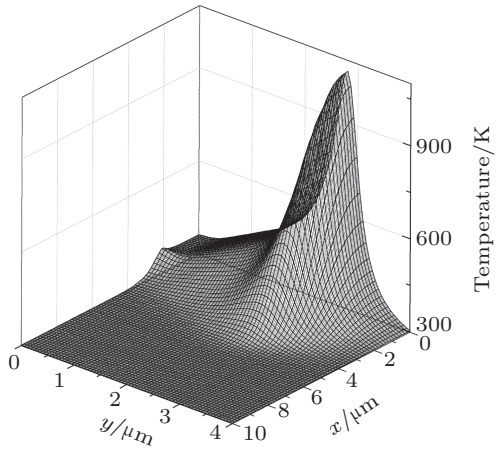


Fig. 6. Temperature distribution of the device under the injection of the square-wave voltage signal at $t = 2.1$ ns.

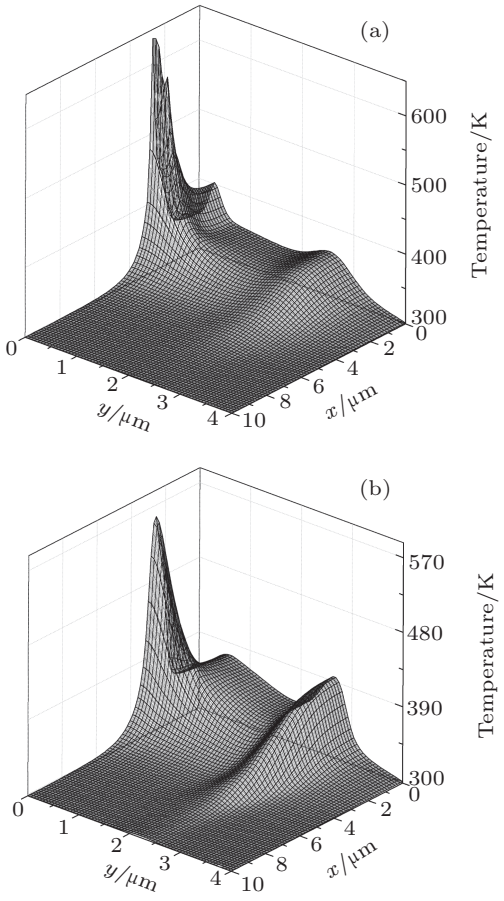


Fig. 7. Temperature distributions of the device under the injection of a sinusoidal voltage signal at (a) 1.75 ns and (b) 2.25 ns.

3.3. HPM absorbed energy versus pulse duration

Wunsch, Bell[14], and Tasca[18] developed empirical formulas regarding the dc pulse power required to cause degradation or failure in semiconductor junction devices to the nanosecond pulse duration (1–100 ns). We have

$$E_{\rm A} = LA\tau^0, \tag{6}$$

where $E_{\rm A}$ is the dc pulse burnout energy, and A and L are constants which depend on the BJT type. The formula definitely indicates that the absorbed energy $E_{\rm A}$ required to cause device degradation or failure does not depend upon the pulse duration τ. However, the experimental study of Brown on the threshold levels for damage to the transistors showed that the transistor absorbed energy exhibits a different response to dc nanosecond pulses (3–55 ns) by using a direct injection approach, and concluded that no one formula can yield accurate threshold levels for all device types.[13] A straight line with a slope of 0.16 gave the best least squares fit according to Brown's dc pulse data. In addition, the simulation results of the bipolar transistor caused by dc pulse signals also showed that the damage energy of the BJT is not a constant in the nanosecond scale.[15]

In this paper, the absorbed microwave energy is obtained by calculating the instantaneous voltage and current waveform as a function of time until the device lattice temperature approaches 1688 K. Figure 8 shows the dependence of the absorbed energy of the device on the pulse width. It indicates that the absorbed energy increases slowly with the pulse width. Adopting the curve fitting method to fit the data points, we find that the relationship between the absorbed energy and the pulse width meets the demand

$$E = 17.2\tau^{0.19}, \tag{7}$$

which has a high degree of fitting, up to 0.99.

There are two reasons for the tendency of the curve. Firstly, the energy absorbed at the damage position is dissipated in a small amount to surrounding regions over time. Secondly, and most importantly, in the positive half period, the heating spots are between the pn junction and the n^-–n^+ interface areas, which are not the damage positions, and the energy absorbed here increases with pulse duration.

As is shown in Fig. 8, the minimum value of the damage energy is about 16 nJ, which is about the same as the maximum value caused by the dc nanosecond pulses of the same transistor.[17] This result indicates that the microwave nanosecond pulse energy must exceed the dc nanosecond pulse energy to cause transistor failure, and that the dc nanosecond pulse failure data may be capable of being a lower bound for the microwave pulse failure data.

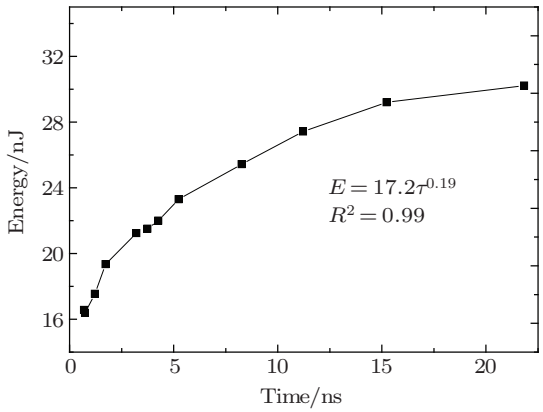


Fig. 8. Plot of damage energy as a function of pulse width.

4. Conclusion

ISE–TCAD simulations of bipolar transistor pulse-width effects due to high power microwave interference are performed in this paper. The results show that the absorbed energy required to cause device failure is not a constant for nanosecond pulses due to the variation of the hot spots in the microwave damage process. Moreover, it is demonstrated that the shorter the pulse width is, the more power threshold but less absorbed energy is needed to damage the device. The comparison of the microwave pulse damage data with the existing dc pulse damage data for the bipolar transistor indicates that, for nanosecond pulses, the damage power and the damage energy of the device caused by microwaves must exceed that caused by dc pulses, which may be useful for making an order-of-magnitude estimate of the microwave failure levels for semiconductor devices of the same type. If the failure levels of the semiconductor components are understood, the factor of an HPM environment can be taken into consideration in the circuit design and the selection of proper components.

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