The influence and explanation of fringing-induced barrier lowering on sub-100 nm MOSFETs with high-k gate dielectrics*

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The fringing-induced barrier lowering (FIBL) effect of sub-100 nm MOSFETs with high-k gate dielectrics is investigated using a two-dimensional device simulator. An equivalent capacitance theory is proposed to explain the physics mechanism of the FIBL effect. The FIBL effect is enhanced and the short channel performance is degraded with increasing capacitance. Based on equivalent capacitance theory, the influences of channel length, junction depth, gate/lightly doped drain (LDD) overlap length, spacer material and spacer width on FIBL is thoroughly investigated. A stack gate dielectric is presented to suppress the FIBL effect.

Keywords: high-k gate dielectric, fringing-induced barrier lowering, stack gate dielectric, MOSFET

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1. Introduction

As MOSFET size continues to scale down to sub-100 nm, the thickness of SiO_2 is reduced to keep a sufficient current driving capability. However, when the thickness of SiO_2 is thinner than 1.5 nm, the direct tunneling current increases dramatically, which becomes a main limiting factor in complementary metal oxide semiconductor (CMOS) technology.[1] High-k materials as alternative dielectrics are widely studied, and have larger physical thicknesses to prevent direct tunneling.[2] Unfortunately, a side effect called fringing-induced barrier lowering (FIBL) becomes a serious threat to reliability when the thickness of the gate dielectric is comparable to the channel length.[3] With the increase in the physical thickness of the gate dielectric, the electric field lines originating from the bottom of the gate electrode and terminating on the source and drain region increase.[4] These electric lines form an electrical field originating at the drain, penetrating into the channel through the high-k dielectric and suppressing the barrier height from the source to the channel.[5] This causes lower threshold voltage, worse sub-threshold swing and increased off-state current.[6] In this paper, the off-state current is used to characterize the degradation of devices with high-k gate dielectrics.

Some research has been conducted to understand the effect of FIBL on the device and circuit performances of MOSFETs with high-k gate dielectrics.[7−10] FIBL is investigated using different device structures, such as the effective oxide thickness, the gate length, the junction depth, and the spacer width. However, these studies have not explained the physical mechanism of the FIBL effect thoroughly. Mohaoatra *et al.*[11] proposed an equivalent electrical distance theory to describe the FIBL effect, but the influence of the spacer on the device characteristics has not been included.

In the present paper, an equivalent capacitance theory is proposed to explain the physics mechanism of MOSFETs with high-k gate dielectrics. For the first time, the equivalent capacitance is used to describe the influence of the FIBL effect. By analysing the factors affecting the capacitance, the physics behind the FIBL effect can be explained. The influence of structure parameters on FIBL is investigated using the two-dimensional device simulator ISE–TCAD. The effect of the gate dielectric stack on device performance is also presented.

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2. Device structure and parameters

nMOSFETs with a lightly doped drain (LDD) structure are used in this study. A spacer layer with heavily doped source/drain extensions is deposited. Figure 1 shows a cross-section view of the device structure. The process and structure parameters are shown in Table 1.

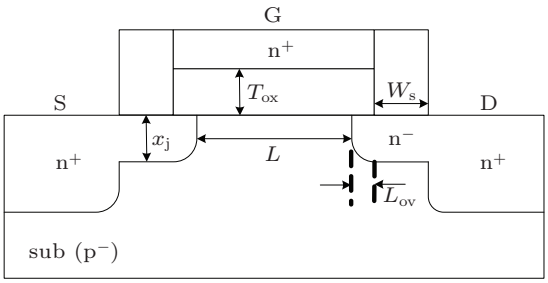


Fig. 1. Schematic cross-section of nMOSFETs with an LDD structure.

Table 1. The process and structure parameters of the nMOSFETs.

Parameters	Values
n^+ poly-Si doping concentration/10^{20} cm^{-3}	1
n^+ source/drain doping concentration/10^{20} cm^{-3}	1
n^- LDD regions doping concentration/10^{19} cm^{-3}	1
p^- substrate doping concentration/10^{18} cm^{-3}	4
channel length L/nm	32
channel width W/μm	1
equivalent gate dielectric thickness T_{ox}/nm	1
spacer width W_s/nm	40
LDD junction depth x_j/nm	15
gate/LDD overlap length L_{ov}/nm	9

In the ISE-TCAD simulation, DopingDep, HighFieldSat and Enormal are used as the mobility models. Band gap narrowing is used as the band gap model. The source contact and substrate contact are connected to the ground.

3. Physics mechanism of the FIBL effect

In this paper, the dielectric permittivity of the gate varies from 3.9 (SiO_2) to 80 (TiO_2). In order to keep the same gate oxide capacitance, the equivalent thickness of the high-k gate dielectric is given as

$$T_k = \frac{k \times T_{ox}}{3.9}, \tag{1}$$

where k is the permittivity of the high-k gate dielectric and T_{ox} is the equivalent thickness of SiO_2.

Figure 2 shows a schematic of the coupling paths from the drain and gate electrodes through different paths to a point near the source in the channel. The coupling paths are introduced to indicate the electric field line path terminating the channel region. The source and the substrate are grounded, the coupling effects from the source and substrate can be ignored. Here, we define an equivalent coupling capacitance C_{cp}, which can be used to describe the coupling effect between the gate/drain and the channel region. With increasing capacitance, the gate/drain electrode is closely coupled to the channel, and the influence of the gate/drain on the channel is enhanced. C_{cp} is expressed as

$$C_{cp} = a \times \frac{\varepsilon_{in} \times S_{cp}}{T_{phy}}, \tag{2}$$

with

$$S_{cp} = W \times L_{eff}, \tag{3}$$

where a is the fitting parameter between 0 and 1; ε_{in} is the permittivity of the dielectric between the equivalent capacitance plates; S_{cp} is the area of the equivalent capacitance plates; T_{phy} is the physical distance between the two electrodes of the equivalent capacitance; L_{eff} is the length of the equivalent capacitance plate; and W is the channel width, a constant equal to 1 μm. Therefore, the equivalent capacitance is shown as follows:

$$C_{cp} \propto \frac{\varepsilon_{in} \times L_{eff}}{T_{phy}}, \tag{4}$$

where L_{eff} is the channel length ($L_{eff} = L$), ε_{in} is the gate dielectric permittivity ($\varepsilon_{in} = k$), and T_{phy} is the thickness of the high-k gate dielectric ($T_{phy} = T_k$), which can be obtained from Eq. (1). Thus, the equivalent coupling capacitance from the gate electrode to the channel is constant. It is concluded that the FIBL effect induced by the high-k gate dielectric is determined mainly by the coupling effect from the drain electrode to the channel region.

The drain electrode is coupled to the channel region through the substrate, gate and spacer. Here, we define three coupling paths from the drain electrode to the channel region. They are path I (through the substrate), path II (through the gate) and path III, respectively. Path III is comprised of path III_g (through the gate) and path III_s (through the spacer). Based on the three coupling paths, the influences of the structure parameters (the channel length, junction depth, gate/LDD overlap length, spacer

width, spacer permittivity and gate stack scheme) on FIBL are investigated.

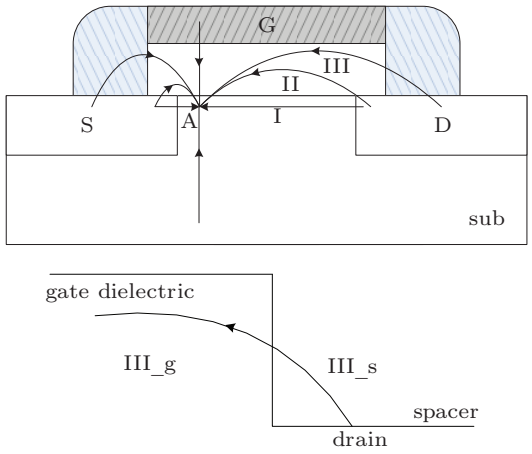


Fig. 2. Schematic of the different coupling paths.

4. Results and discussion

Figure 2 shows that the coupling through path I (through the substrate) is related to the channel length and the junction depth, which correspond to $T_{\rm phy}$ and $L_{\rm eff}$ in Eq. (4), respectively. When the channel length decreases or junction depth increases, the equivalent capacitance $C_{\rm cp}$ increases. Therefore, the coupling effect from the drain electrode to the channel increases, the FIBL effect increases and a large off-state current is obtained.

Figure 3 shows the dependences of off-state current $I_{\rm off}$ on channel length L for different gate dielectric constants. From the figure, it can be found that the off-state current performance degradation is bigger for short channel lengths. This is mainly due to the fact that the coupling effect from the drain through the substrate to the channel region increases with decreasing channel length, which corresponds to the $T_{\rm phy}$ in Eq. (4). The FIBL effect then becomes obvious, and a large off-state current is obtained. The coupling effect of the channel length affects not only path I, but also paths II and III. The coupling effect mechanism is the same. The coupling effect affects the physical distance $T_{\rm phy}$ between the two electrode plates of the equivalent capacitance, and the coupling effect increases for shorter channel lengths.

Figure 4 shows the dependences of the off-state current $I_{\rm off}$ on junction depth $x_{\rm j}$ for different gate dielectric constants. It can be seen from the figure that the off-state current increases with the increase in junction depth, which corresponds to $L_{\rm eff}$ in Eq. (4). This is consistent with the above theoretical analysis. From Fig. 2, it can be found that path I (through the substrate) is independent of gate dielectric constants. From both Figs. 3 and 4, we can see that for the same channel length and junction depth, $I_{\rm off}$ increases with the increase in gate dielectric permittivity. That is mainly due to the coupling effect of the drain electrode through paths II and III, which will be analysed in the following section.

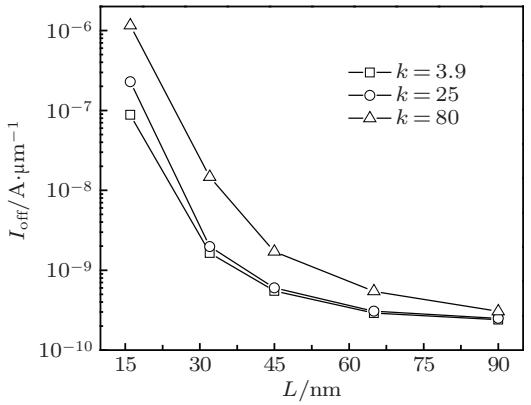


Fig. 3. Dependences of $I_{\rm off}$ on L for different gate dielectric constants.

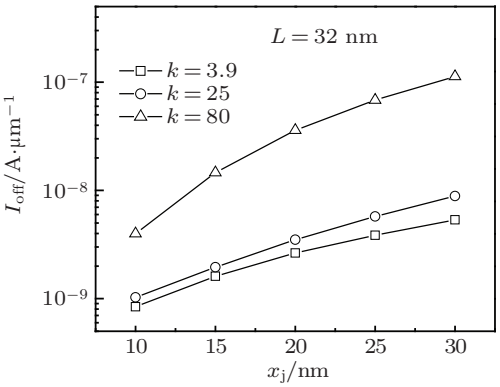


Fig. 4. Dependences of $I_{\rm off}$ on $x_{\rm j}$ for different gate dielectric constants.

The coupling through path II (through the gate) is related to the dielectric permittivity and gate/LDD overlap area, which correspond to $\varepsilon_{\rm in}$ and $L_{\rm eff}$ in Eq. (4), respectively. A smaller equivalent capacitance is obtained for shorter gate/LDD overlap length $L_{\rm ov}$ and smaller gate dielectric permittivity, and the coupling effect of the drain electrode on the channel through path II is decreased. Thus, the FIBL effect is suppressed and a small off-state current is obtained.

Figure 5 shows the dependences of the off-state current $I_{\rm off}$ on gate/LDD overlap length $L_{\rm ov}$ for different gate dielectric constants. The off-state current increases with the increase in gate/LDD overlap length and gate dielectric permittivity, which correspond to

$L_{\rm eff}$ and $\varepsilon_{\rm in}$ in Eq. (4), respectively. The coupling effect increases with the increase in equivalent capacitance. The FIBL effect is then enhanced, and a large off-state current is obtained. The figure accords well with the theoretical analysis.

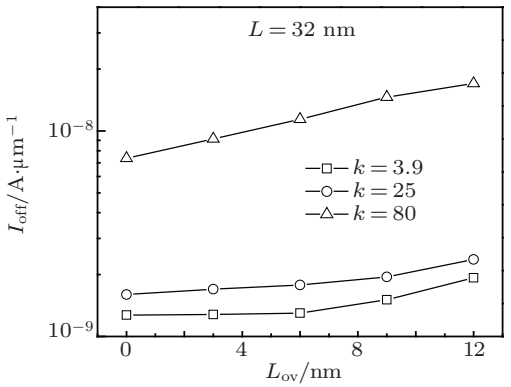


Fig. 5. Dependence of $I_{\rm off}$ on $L_{\rm ov}$ for different gate dielectric constants.

Coupling path III is composed of two parts, path III_s (through the spacer) and path III_g (through the gate). Path III_s is related to spacer width ($W_{\rm s}$) and spacer dielectric permittivity, which correspond to $L_{\rm eff}$ and $\varepsilon_{\rm in}$ in Eq. (4), respectively. Path III_g is related to the gate dielectric permittivity, which corresponds to the $\varepsilon_{\rm in}$ in Eq. (4). Thus, the coupling effect through path III can be equivalent to two capacitors in series, which correspond to path III_g and path III_s, respectively. The total capacitance increases. The coupling effect from the drain electrode to the channel then increases, and the FIBL effect and the off-state current increase.

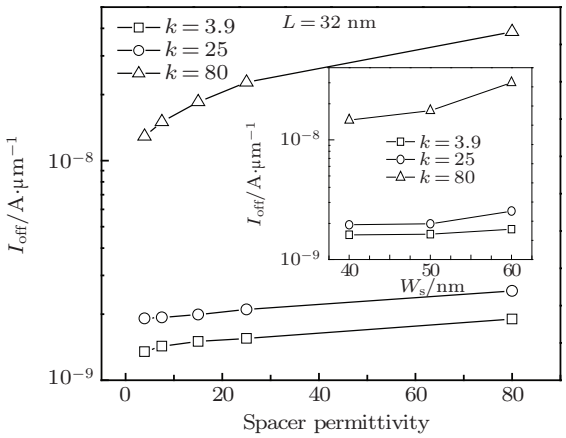


Fig. 6. Dependences of $I_{\rm off}$ on spacer permittivity and $W_{\rm s}$ for different gate dielectric constants.

Figure 6 shows the dependences of the off-state current $I_{\rm off}$ on spacer permittivity and spacer width $W_{\rm s}$ for different gate dielectric constants. The off-state current increases with the increases in spacer width and spacer dielectric permittivity. Because the coupling effect through the gate dielectric is enhanced by increasing $\varepsilon_{\rm in}$, the off-state current increases for larger gate dielectric permittivity.

Figure 7 shows simulated equipotential contours of a MOSFET with a stack gate structure. The interface material is SiO_2, and the thickness of the SiO_2 layer is 0.6 nm. The high-k material is TiO_2 and the equivalent thickness of TiO_2 is 0.4 nm. Figures 7(a) and 7 (b) are the bottom SiO_2 layer and the top SiO_2 layer, respectively. It can be observed that most of the fringing field lines originate from the drain region through the SiO_2 layer. This means that the coupling effect of the drain electrode to the channel is mainly through the SiO_2 layer. Small $\varepsilon_{\rm in}$ is obtained in Eq. (4), and the FIBL effect is suppressed. The $T_{\rm phy}$ value of the bottom SiO_2 layer is small compared with that of the top SiO_2 layer, which can suppress FIBL effect better.

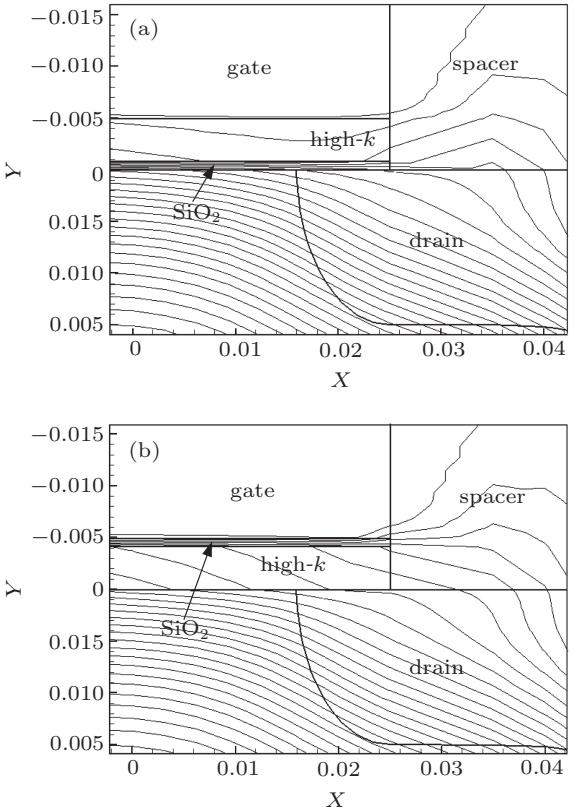


Fig. 7. Simulated equipotential contours of the MOSFET with a stack gate structure: (a) bottom SiO_2 layer, (b) top SiO_2 layer.

Figure 8 shows the dependences of the off-state current $I_{\rm off}$ and gate direct tunneling current $I_{\rm g}$ on the ratio of oxide thickness to effective dielectric thickness. We can see that the thinner SiO_2 layer induces a bigger off-state current. On the other hand, a thinner SiO_2 results in a thicker total effective dielectric layer,

which induces a smaller gate leakage current. Therefore, the ratio of oxide thickness to effective dielectric thickness needs to be optimized for the stack gate dielectric. There have been trade-off problems between the off-state current and the gate leakage current with increasing thickness of SiO_2. For nMOSFETs with a 32 nm channel length and a 1 nm equivalent oxide thickness, HfO_2 is used as the high-k dielectric material, and the oxide thickness is about 60 percent (marked by a dashed line in Fig. 8) of the effective thickness of the gate dielectric, which is a reasonable choice for the gate structure. We can obtain better characteristics of both the off-state current and the gate leakage current for this structure.

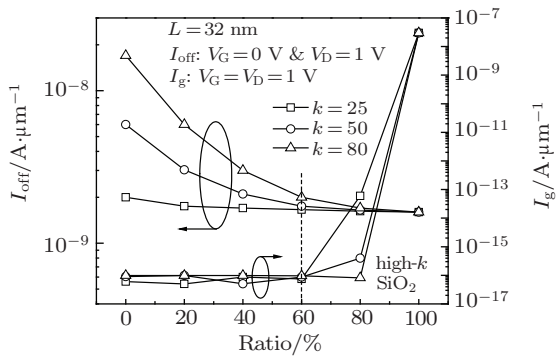


Fig. 8. Dependences of I_{off} and I_g on the ratio of oxide thickness to effective dielectric thickness.

5. Conclusion

A comprehensive analysis of FIBL in sub-100 nm MOSFETs with high-k gate dielectrics is investigated using two-dimensional numerical simulations. An equivalent coupling capacitance theory is proposed, which gives better insight into the physics of the FIBL phenomenon. The coupling effect of the drain electrode on the channel through different kinds of paths enhances the FIBL effect and induces a large off-state current, which can be controlled by combining a low-k spacer, short spacer width, low junction depth and small gate/LDD overlap length. The stack gate dielectric is shown to suppress the FIBL effect, in particular when the permittivity of the bottom layer is smaller than that of the top layer.

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