A threshold voltage analytical model for high-k gate dielectric MOSFETs with fully overlapped lightly doped drain structures*

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We investigate the influence of voltage drop across the lightly doped drain (LDD) region and the built-in potential on MOSFETs, and develop a threshold voltage model for high-k gate dielectric MOSFETs with fully overlapped LDD structures by solving the two-dimensional Poisson's equation in the silicon and gate dielectric layers. The model can predict the fringing-induced barrier lowering effect and the short channel effect. It is also valid for non-LDD MOSFETs. Based on this model, the relationship between threshold voltage roll-off and three parameters, channel length, drain voltage and gate dielectric permittivity, is investigated. Compared with the non-LDD MOSFET, the LDD MOSFET depends slightly on channel length, drain voltage, and gate dielectric permittivity. The model is verified at the end of the paper.

Keywords: threshold voltage, high-k gate dielectric, fringing-induced barrier lowering, short channel effect

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1. Introduction

With the development of semiconductor technology, the size of MOSFETs has been scaled down to sub-100 nm. The thickness of the gate oxide is below 1.5 nm, and such an ultra-thin gate oxide will introduce high direct tunneling gate leakage current.[1−3] To reduce the gate leakage current and standby power, high permittivity materials are needed to replace SiO_2 as the gate dielectric.[4−6] The traditional threshold voltage model is no longer applicable because of the influence of the short channel effect (SCE) and fringing-induced barrier lowering (FIBL) on the threshold voltage. So it is necessary to develop a new MOSFET threshold voltage model with high-k gate dielectrics. Several threshold voltage models have been proposed in Refs. [7]–[9]. However, these models are used only for non-LDD (lightly doped drain) MOSFETs, and cannot be applied to LDD MOSFETs. Therefore, a suitable threshold voltage model for a high-k gate dielectric MOSFET with an LDD structure is required.

In this paper, a threshold voltage analytical model of a high-k gate dielectric MOSFET with a fully overlapped LDD structure is proposed, in which the influences of the voltage drop in the LDD region and the small built-in potential are considered. The two-dimensional (2D) potential distribution is obtained by solving Poisson's equation in the silicon and gate dielectric layers. The effect of high-k gate dielectric on threshold voltage is discussed in detail over a wide range of permittivity.

2. Model derivation

We investigate Poisson's equation of potential distribution, and solve Poisson's equation to obtain the channel surface potential. A 2D threshold voltage model is presented.

The structure of a high-k gate dielectric nMOSFET with fully overlapped LDD structure is shown in Fig. 1, where L_{n-} is the length of the LDD region, X_j is the junction depth of the LDD region, T_{ox} is the thickness of the gate dielectric, and L is the channel

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length. The x axis is perpendicular to the channel direction and the y axis is along the lateral channel direction.

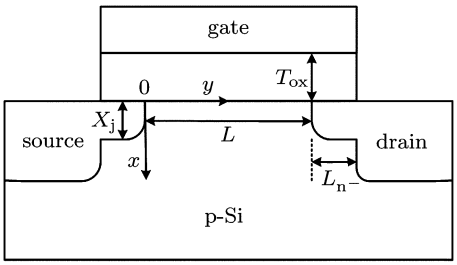


Fig. 1. Schematic diagram of an LDD nMOSFET.

For simplicity, the mobile carriers in the channel depletion region are neglected.[10] Thus, the 2D Poisson's equation in the channel and gate dielectric region can be written as

$$\frac{\partial^2\varphi(x,y)}{\partial x^2}+\frac{\partial^2\varphi(x,y)}{\partial y^2} = \begin{cases} 0, & -T_{ox}\le x\le 0,\quad 0\le y\le L,\\ \dfrac{qN_A}{k_{si}}, & 0\le x\le x_d,\quad 0\le y\le L, \end{cases} \tag{1}$$

where N_A is the doping concentration of the substrate, and x_d is the width of the depletion region in the substrate.

To solve Poisson's equation, the boundary conditions are shown as follows.

(i) At the gate/gate dielectric layer interface ($x=-T_{ox}$), the 2D surface potential distribution is obtained as

$$\varphi(-T_{ox},y)=V_g-V_{fb}, \tag{2}$$

where V_g is the gate voltage and V_{fb} is the flat-band voltage.

(ii) The electric flux (displacement) at the gate dielectric/substrate-Si layer interface ($x=0$) is continuous, and expressed as

$$\left.\frac{\partial\varphi(x,y)}{\partial x}\right|_{x=0}=\frac{k_{ox}}{k_{si}}\frac{\varphi(0,y)-V_g+V_{fb}}{T_{ox}}, \tag{3}$$

where k_{ox} and k_{si} are the pemittivities of the gate dielectrics and the substrate, respectively.

(iii) At the depletion edge ($x=x_d$), the boundary conditions are shown as follows:

$$\begin{cases} \varphi(x_d,y)=V_{bs},\\ \left.\dfrac{\partial\varphi(x,y)}{\partial x}\right|_{x=x_d}=0, \end{cases} \tag{4}$$

where V_{bs} is the substrate voltage. The substrate potential is taken to be the ground potential, i.e. $V_{bs}=0$.

Based on the boundary conditions of Eqs. (2)–(4), we use the variation method[11,12] to solve Poisson's equation, and the 2D surface potential distribution is obtained as

$$\varphi(x,y) = V_0(x)+[\varphi(x,0)-V_0(x)]\frac{\sinh[(L-y)/l]}{\sinh(L/l)} + [\varphi(x,L)-V_0(x)]\frac{\sinh(y/l)}{\sinh(L/l)}, \tag{5}$$

where $V_0(x)$ is the solution of the one-dimensional (1D) Poisson's equation for the long-channel MOSFET, and l is the characteristic length[7] as shown below:

$$l=\left[\frac{5k_{ox}T_{ox}/6+A+k_{si}x_d}{C_{ox}+5C_d/6}\right]^{1/2}, \tag{6}$$

where $C_{ox}=k_{ox}/T_{ox}$, $C_d=k_{si}/x_d$, $x_d=\sqrt{4k_{si}\varphi_f/qN_A}$, and $A=2(T_{ox}/x_d)+(4/3)(T_{ox}/x_d)^2$.

We now take the boundary conditions of the source and drain regions into account.

i) On the source side ($y=0$), the boundary condition can be written as

$$\varphi(x,0)=V_{bi}, \tag{7}$$

where V_{bi} is the built-in potential. For the LDD MOSFET, V_{bi} is the built-in potential of the n^--substrate junction instead of the n^+-substrate junction, which is expressed as

$$V_{bi}=\frac{kT}{q}\ln\frac{\overline{N_D}N_A}{n_i^2}, \tag{8}$$

where $\overline{N_D}$ is the average doping concentration in the LDD region that can be approximated as

$$\overline{N_D}=\frac{n_t}{x_j}, \tag{9}$$

with n_t being the total doping concentration in the LDD region, and obtained by the following equation:[13]

$$\begin{cases} n_t=\int_0^\infty N_p\exp\left[-\dfrac{1}{2}\left(\dfrac{x-x_p}{D_x}\right)^2\right]\mathrm{d}x,\\ D_x=\sqrt{\dfrac{x_j-x_p}{-2\ln(N_j/N_p)}}, \end{cases} \tag{10}$$

where N_p is the peak concentration; x_p is the peak position, generally defined as zero, which means that the peak concentration is in the surface of the substrate; x_j is the pn junction position, which is equal to the junction depth; and N_j is the doping concentration at the junction.

ii) On the drain side ($y = L$), the boundary condition is given by

$$\varphi(x, L) = V_{\rm bi} + V_{\rm ds}, \tag{11}$$

where $V_{\rm ds}$ is the drain voltage. For the n^+ region, the n^+-substrate junction can be approximated as an abrupt junction. The channel electric field drops to zero quickly. There will be no voltage drop in the n^+ region. For the n^- region, the voltage drop in the LDD region may not be neglected at higher drain bias. Therefore, the drain voltage $V_{\rm ds}$ can be replaced by the equivalent drain voltage $V_{\rm deff}$[14]

$$V_{\rm deff} = \frac{V_{\rm ds}}{1 + \alpha L_{\rm n^-}/L}, \tag{12}$$

where α is a fitting parameter between 0 and 1. For a given process, α can be determined from the LDD doping profile.[15] When the drain bias is smaller than 0.05 V, the voltage drop in the LDD region may be neglected.

Substituting $\varphi(x, 0)$ (Eq. (7)) and $\varphi(x, L)$ (Eq. (11)) into Eq. (5), the 2D surface potential distribution of LDD MOSFET is obtained as

$$\varphi(x, y) = V_0(x) + [V_{\rm bi} - V_0(x)]\frac{\sinh\left[(L-y)/l\right]}{\sinh(L/l)} + [V_{\rm bi} + V_{\rm ds} - V_0(x)]\frac{\sinh\left(y/l\right)}{\sinh(L/l)}. \tag{13}$$

Based on Eq. (13), the location y_0 of the minimum surface potential $\varphi_{\rm s\,min}$ in the channel can be determined by $\mathrm{d}\varphi(x, y)/\mathrm{d}y|_{x=T_{\rm ox}} = 0$ as

$$y_0 = \frac{l}{2}\ln\frac{[V_{\rm bi} - V_0(T_{\rm ox})]\,\mathrm{e}^{L/l} - [V_{\rm bi} - V_0(T_{\rm ox}) + V_{\rm ds}]}{[V_{\rm bi} - V_0(T_{\rm ox}) + V_{\rm ds}] - [V_{\rm bi} - V_0(T_{\rm ox})]\,\mathrm{e}^{-L/l}}. \tag{14}$$

Substituting Eq. (14) into Eq. (13), the minimum surface potential $\varphi_{\rm s\,min}$ can be obtained. To determine the threshold voltage, setting $\varphi_{\rm s\,min} = 2\varphi_{\rm f}(\varphi_{\rm f} = (kT/q)\ln(N_{\rm A}/n_{\rm i}))$, the corresponding $V_{\rm g}$ is defined as the threshold voltage $V_{\rm th}$, which is expressed as

$$V_{\rm th} = V_{\rm th0} - \frac{(V_{\rm bi} - 2\varphi_{\rm f})\dfrac{\sinh[(L-y_0)/l]}{\sinh(L/l)} + (V_{\rm bi} + V_{\rm ds} - 2\varphi_{\rm f})\dfrac{\sinh(y_0/l)}{\sinh(L/l)}}{1 - \dfrac{\sinh[(L-y_0)/l]}{\sinh(L/l)} - \dfrac{\sinh(y_0/l)}{\sinh(L/l)}}, \tag{15}$$

where $V_{\rm th0}$ is the classical threshold voltage of the long-channel MOSFET. The threshold voltage roll-off can be defined as

$$\Delta V_{\rm th} = V_{\rm th} - V_{\rm th0} = -\frac{(V_{\rm bi} - 2\varphi_{\rm f})\dfrac{\sinh[(L-y_0)/l]}{\sinh(L/l)} + (V_{\rm bi} + V_{\rm ds} - 2\varphi_{\rm f})\dfrac{\sinh(y_0/l)}{\sinh(L/l)}}{1 - \dfrac{\sinh[(L-y_0)/l]}{\sinh(L/l)} - \dfrac{\sinh(y_0/l)}{\sinh(L/l)}}. \tag{16}$$

3. Model verification and discussion

In Section 2, we can see that the location y_0 given by Eq. (14) and the minimum surface potential $\varphi_{\rm s\,min}$ are the key parameters of the threshold voltage. Figure 2 shows the surface potential distributions along the channel for different channel lengths. When the drain voltage is as low as zero, the surface potentials of the source and the drain are the built-in potential $V_{\rm bi}$, and the location y_0 of the minimum surface potential $\varphi_{\rm s\,min}$ is approximately equal to $L/2$. As the drain voltage increases, the surface potential of the source is almost unchanged, while the surface potential of the drain increases to $V_{\rm bi} + V_{\rm ds}$. Position y_0 is no longer in the middle of the channel, and it shifts to the source side ($y_0 < L/2$). The corresponding minimum surface potential $\varphi_{\rm s\,min}$ increases, which lowers the barrier height of source to channel, and a smaller threshold voltage is obtained. The influence of drain voltage on the threshold voltage is generally known

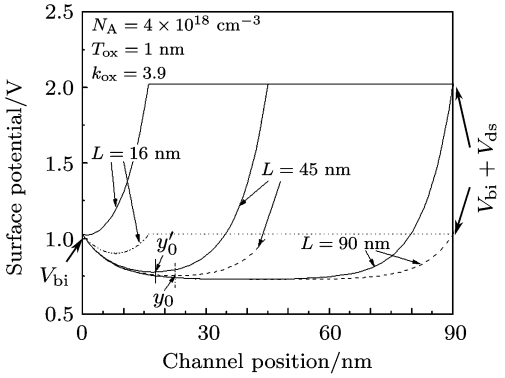


Fig. 2. Surface potential distribution for different channel lengths.

as the SCE. The SCE is obvious for shorter channel length.

In order to verify the accuracy of the model, the analytical results of the threshold voltage calculated from the model are compared with the numerical results obtained by the 2D device simulator ISE–TCAD. In the ISE–TCAD simulation, Dopingdep, Highfieldsat and Enormal are used as the mobility model and Bandgapnarrowing is used as the band gap model; the source contact and the substrate contact are connected to the ground. The device structure is the same as the structure shown in Fig. 1. The source and drain adopt Gauss doping, and the concrete process parameters are listed in Table 1.

Table 1. The process parameters of the device.

Parameters	Values
doping concentration of the substrate $N_{\rm A}/10^{18}{\rm cm}^{-3}$	4
length of the LDD region $L_{\rm n^-}$/nm	20
peak concentration of the LDD region $N_{\rm p}/10^{19}{\rm cm}^{-3}$	1
peak position of the LDD region $x_{\rm p}$/nm	0
junction depth of the LDD region $x_{\rm j}$/nm	15
doping concentration at the junction $N_{\rm j}/\ 10^{18}{\rm cm}^{-3}$	4

Figures 3 and 4 show the dependences of y_0 and $\varphi_{\rm s\,min}$ on channel length for different drain voltages, respectively. When drain voltage increases, y_0 decreases and $\varphi_{\rm s\,min}$ increases. It can be seen that y_0 and $\varphi_{\rm s\,min}$ derived from the model accord well with the ISE–TCAD simulation results, respectively.

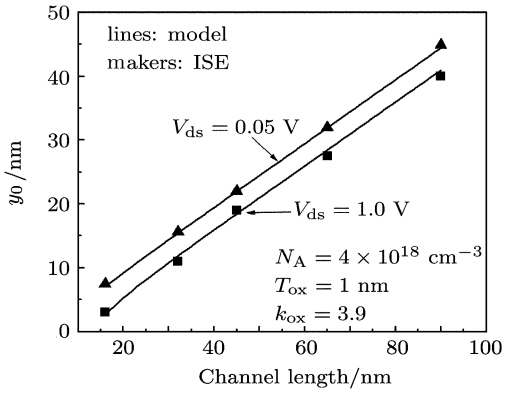


Fig. 3. Dependences of the location of minimum surface potential on channel length.

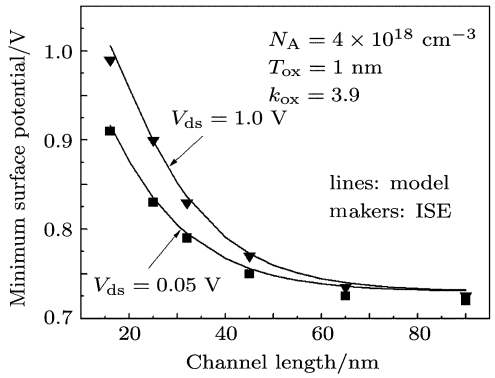


Fig. 4. Dependences of the minimum surface potential on channel length.

Figure 5 shows the influences of gate dielectric permittivity and channel length on threshold voltage roll-off. For shorter channel MOSFETs, the threshold voltage roll-off begins to increase obviously with increasing k. It increases greatly, especially for $k > 25$. For the same equivalent oxide thickness, the physical thickness of high-k gate dielectrics increases as

$$T_{\rm ox} = \frac{k_{{\rm high}-k}}{k_{\rm ox}} T_{\rm ox}^{\rm eq}, \tag{17}$$

where $T_{\rm ox}^{\rm eq}$ is the equivalent oxide thickness, $k_{{\rm high}-k}$ is the permittivity of the high-k material, and $k_{\rm ox}$ is the permittivity of SiO_2. As the physical thickness of the gate dielectric increases, the number of electric field lines originating from the bottom of the gate electrode and terminating on the source and drain regions increases. These electric field lines form an electric field from source to channel, and thereby decrease the barrier height between the channel and the source. A lower barrier height implies a lower threshold voltage. When the channel length increases, the influence of gate dielectric permittivity on the threshold voltage begins to decreases. It is generally known as FIBL. Figure 6 shows the potential distributions along the channel for different gate dielectric permittivities, which can help us to understand the FIBL effect better.

The proposed threshold voltage model is also valid for the non-LDD MOSFETs. By replacing the doping concentration of the LDD region in Eq. (8) with the doping concentration of the n^+ region, the built-in potential ($V_{\rm bi}$) of the n^+-substrate junction can be obtained. In this paper, the doping concentration of the n^+ region is 1×10^{20} cm^{-3}. As stated in

Section 2, the n^+-substrate junction can be approximated as an abrupt junction, so the channel electric field drops to zero quickly. This means that there is no voltage drop in the n^+ region ($V_{\rm deff} = V_{\rm ds}$). Substituting $V_{\rm bi}$ and $V_{\rm deff}$ into Eq. (11), one can obtain the threshold voltage of the non-LDD MOSFET.

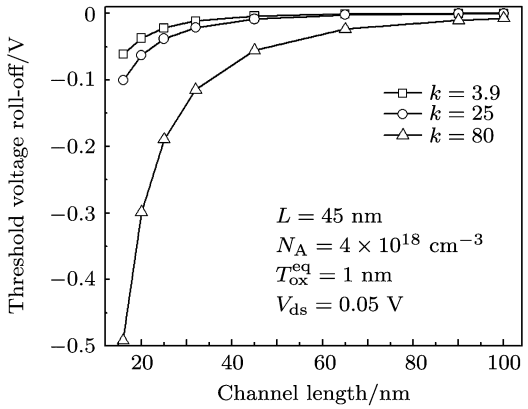


Fig. 5. The dependences of the threshold voltage roll-off on channel length with different gate dielectric permittivities.

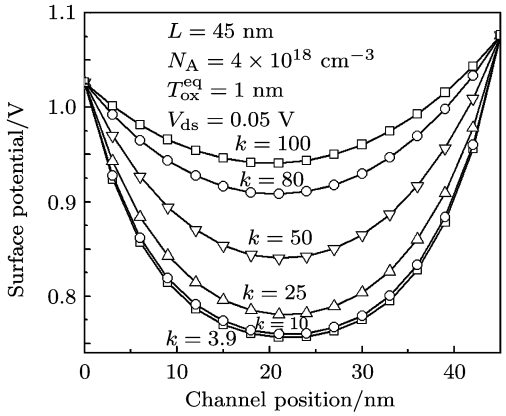


Fig. 6. Surface potential distributions for different gate dielectric permittivities.

Figures 7 and 8 show the dependences of threshold voltage roll-off on the drain voltage and gate dielectric permittivity, respectively. The process parameters of the LDD MOSFET are shown in Table 1. For the non-LDD MOSFET, the doping concentration of the n^+ region is 1×10^{20} cm^{-3}, the doping concentration of the substrate is 4×10^{18} cm^{-3}, the n^+-substrate junction depth is 30 nm, and the equivalent oxide thickness is 1 nm. For the given gate dielectric permittivity ($k = 3.9$), the threshold voltage roll-off increases as drain voltage decreases, as shown in Fig. 7. This is obvious for shorter channel length. The influence of drain voltage on the threshold voltage roll-off is small for the LDD MOSFET compared with that for the non-LDD MOSFET.

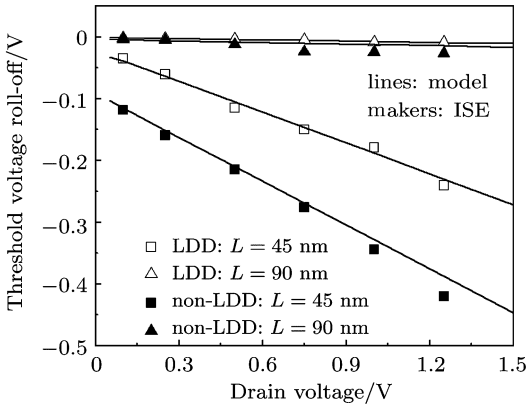


Fig. 7. Dependences of threshold voltage roll-off on drain voltage.

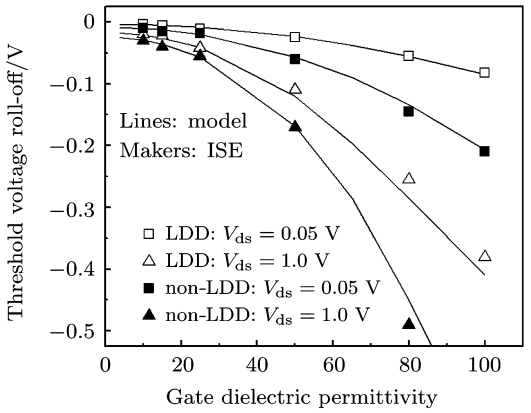


Fig. 8. Dependences of threshold voltage roll-off on gate dielectric permittivity.

For the given channel length ($L = 45$ nm), the threshold voltage roll-off increases as the gate dielectric permittivity increases, as shown in Fig. 8. When the drain voltage increases, the threshold voltage roll-off increases greatly. This shows the coupling effect of FIBL and SCE. However, for the LDD MOSFET, the influences of drain voltage and gate dielectric on the threshold voltage roll-off are smaller than those of the non-LDD MOSFET .

When the high-k material is used to replace SiO_2 as the gate dielectric, the fringing field effect is introduced and the SCE is enhanced greatly. These effects are the dominant factors that cause threshold voltage roll-off. Because the voltage drop in the LDD region and the value of $V_{\rm bi}$ for the LDD MOSFET are smaller than those for the non-LDD MOSFET, the LDD MOSFET has less threshold voltage drift.

4. Conclusion

In this paper, a threshold voltage analytical model for a high-k gate dielectric MOSFET with a fully overlapped LDD structure is developed by solving the 2D Poisson's equation. Based on this model, the influences of the FIBL effect and SCE on the threshold voltage are discussed. A comparison of threshold voltage roll-off between the LDD MOSFET and the non-LDD MOSFET indicates that the LDD MOSFET depends slightly on channel length, drain voltage and gate dielectric permittivity, and shows good resistance to the FIBL effect and SCE. The model has been verified by the ISE–TAD numerical simulation results.

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