Impact of back-gate bias on the hysteresis effect in partially depleted SOI MOSFETs*

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The hysteresis effect in the output characteristics, originating from the floating body effect, has been measured in partially depleted (PD) silicon-on-insulator (SOI) MOSFETs at different back-gate biases. $I_{\rm D}$ hysteresis has been developed to clarify the hysteresis characteristics. The fabricated devices show the positive and negative peaks in the $I_{\rm D}$ hysteresis. The experimental results show that the $I_{\rm D}$ hysteresis is sensitive to the back gate bias in 0.13-μm PD SOI MOSFETs and does not vary monotonously with the back-gate bias. Based on the steady-state Shockley–Read–Hall (SRH) recombination theory, we have successfully interpreted the impact of the back-gate bias on the hysteresis effect in PD SOI MOSFETs.

Keywords: floating body effect, hysteresis effect, back gate bias, partially depleted (PD) SOI

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1. Introduction

Silicon-on-insulator (SOI) technology has been used in deep-submicrometer scale owing to its perfect isolation.[1] It has many attractive features for the high-speed operation of digital applications, such as latch-up immunity, reduced parasitic source, drain capacitances, and ease of making shallow junction.[2] The improved frequency performance through reduced capacitance, higher drive current, and the reduction of interconnect length is a significant advantage of using SOI in analog applications.[3] However, the lack of contact with the body and the presence of bipolar give rise to a number of unique SOI effects. The main concern is the floating body effect (FBE) in the partially depleted (PD) SOI MOSFETs caused by impact ionization, which is known as the Kink effect.[2] As the gate oxide shrinks, the linear Kink effect (LKE) due to the direct tunneling mechanism can appear in the linear region of SOI MOSFETs.[4,5] The hysteresis effect due to the floating body effect in PD SOI MOSFETs can make the circuit design problematic. It has been reported that the dependence of the gate delay on SOI is a function of the switching history of a device in digital applications.[6,7] The hysteresis effects restrict the circuit design for analog applications.[8,9]

In general, the back-gate bias effect of the NMOSFET/SOI is much smaller than that of the NMOSFET/bulk-Si.[10] However, it has been shown that decreasing the box thickness has the advantage of decreasing the penetration of electric fields from the source/drain regions into the body via the box, thus enhancing the immunity to SCEs.[11,12] Decreasing the box thickness also has the advantages of improving the heat dissipation ability of the device.[13] and achieving a high BV.[14] However, as the box shrinks, the device characteristic is sensitive to the back-gate bias in PD SOI MOSFETs. The aim of this work is to elaborate the back-gate dependence of the hysteresis effect in the output characteristics for PD SOI MOSFETs.

2. Experiment

The PD SOI MOSFETs with partially depleted substrates were fabricated in a 0.13-μm SOI CMOS by using STI isolation and $CoSi_2$ silicide. The top silicon film and the buried oxide thickness for the device are 100 and 145 nm, respectively. The gate oxide with a thickness of 1.8 nm and the channel doping concentration is about 1×10^{18} cm^{-3}. The floating body

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(FB) devices and T-gate body (TB) contact MOSFETs were fabricated as references. The devices with a gate length (L) and width (W) both in the range of 0.13–10 μm were selected. All experimental curves were measured by using an Agilent B1500A semiconductor parameter analyzer, with the source of PD SOI MOSFETs grounded.

3. Theory of hysteresis effect in PD SOI MOSFETs

The $I_{\rm D}$ hysteresis has been developed to investigate the hysteresis characteristics of the drain current, which is defined as the difference of $I_{\rm D}$ for $V_{\rm D}$ forward sweep ($V_{\rm D}^{\rm f}$) and reverse sweep ($V_{\rm D}^{\rm r}$)[15,16]

$$I_{\rm D}\ \text{hysteresis} = I_{\rm D}(V_{\rm D}^{\rm f}) - I_{\rm D}(V_{\rm D}^{\rm r}).$$

Figure 1 shows the $I_{\rm D}$ hysteresis at different front gate voltages ($V_{\rm FG}$) in FB PD SOI n-MOSFETs with $W = 10$ μm and $L = 0.13$ μm. A positive peak at small $V_{\rm D}$ and a negative peak at large $V_{\rm D}$ can be clearly observed. This hysteresis behavior can also be observed in FB PD SOI p-MOSFETs.

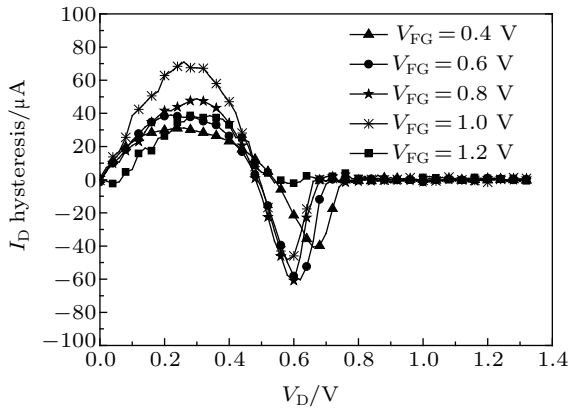


Fig. 1. $I_{\rm D}$ hysteresis versus $V_{\rm D}$ characteristics of FB PD SOI n-MOSFETs with $W = 10$ μm and $L = 0.13$ μm at different values of $V_{\rm FG}$, where the delay time is set as 0 s and the back gate is floating.

With the gate oxide scaling down, the gate to the body current ($I_{\rm GB}$) influences the floating body potential in PD SOI MOSFETs due to the direct tunneling mechanism.[17,18] Figure 2 shows the band diagram of the direct tunneling model, where $\phi_{\rm g} = E_{\rm g}/q$, $\phi_{\rm g}$ is the Fermi potential and $E_{\rm g}$ is the Fermi energy. It is proposed that the gate to the body current (IGB) consists of three components: electron tunneling from the conduction band (ECB), electron tunneling from the valence band (EVB), and hole tunneling from the valence band (HVB). When $|V_{\rm OX}| > \phi_{\rm g}$ ($V_{\rm OX}$ is the voltage on the gate oxide), the electron valence band (EVB) tunneling releases holes (electrons), which constitute $I_{\rm GB}$ in n-MOSFETs (p-MOSFETs). When $|V_{\rm OX}| < \phi_{\rm g}$, GIFBE arises from the anode hole injection (AHI) mechanism.[19,20] During the $V_{\rm D}$ forward sweep, there is no t sufficient time to release the holes caused by GIFBE at a drain voltage smaller than 0.1 V. The accumulation of these holes raises the body potential and further reduces the threshold voltage, resulting in the increase of the drain current at a drain voltage of 0.2 V. Therefore, the positive peak of $I_{\rm D}$ hysteresis can be observed at low $V_{\rm D}$ in Fig. 1.

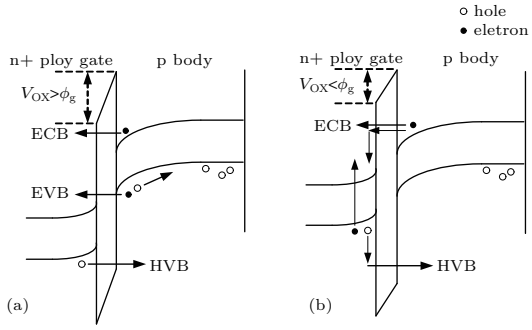


Fig. 2. Schematic band diagram of (a) the EVB tunneling model and (b) the anode hole injection model of PD SOI MOSFETs.

During the $V_{\rm D}$ reverse sweep, there is not sufficient time to release the holes caused by impact ionization at a drain voltage above 0.7 V. The hole accumulation raises the body potential and further reduces the threshold voltage, resulting in the increase of the drain current at a drain voltage of 0.6 V. Therefore, the negative peak of $I_{\rm D}$ hysteresis can be observed at high $V_{\rm D}$ in Fig. 1. To further verify the mechanism of hysteresis effect in PD SOI MOSFETs, we measured $I_{\rm D}$ hysteresis versus $V_{\rm D}$ characteristics under various delay times. As shown in Fig. 3, it is obvious that the hysteresis phenomenon disappears at a long delay time.

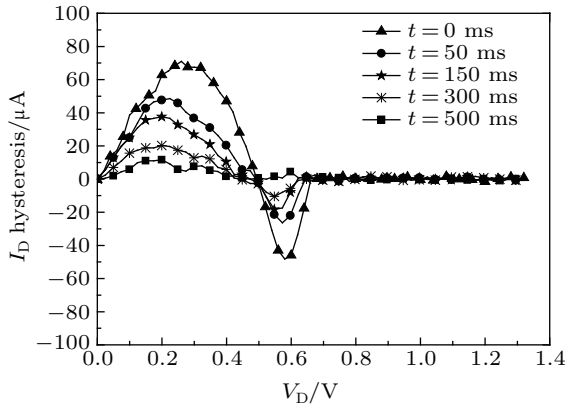


Fig. 3. $I_{\rm D}$ hysteresis versus $V_{\rm D}$ characteristics of FB PD SOI n-MOSFETs with $W = 10$ μm and $L = 0.13$ μm at various delay times, where the back gate is floating and $V_{\rm FG} = 1.0$ V.

4. Theory of hysteresis effect in PD SOI MOSFETs at various back-gate biases

4.1. Experiment results of hysteresis effect at various back-gate biases

Figure 4 shows $I_{\rm D}$ hysteresis characteristics of the FB PD SOI n-MOSFET with $W = 10$ μm and $L = 0.13$ μm at the back-gate voltage ($V_{\rm BG}$) smaller than 0 V, and $V_{\rm FG}$ =1.0 V. It can be clearly observed that the heights of both positive and negative peaks increase with $V_{\rm BG}$. This indicates that the hysteresis effect declines under negative back-gate bias.

Figure 5 shows the measured $I_{\rm D}$ hysteresis versus $V_{\rm D}$ characteristics at different values of $V_{\rm BG}$ ranging from 0 to 30 V. It is found that the $I_{\rm D}$ hysteresis is not monotonic with respect to the back-gate voltage when $V_{\rm BG} \geq 0$ V. For a back-gate voltage from 0 to 15 V, the $I_{\rm D}$ hysteresis decreases with the back-gate voltage. When $V_{\rm BG} \geq 15$ V, it is observed that the $I_{\rm D}$ hysteresis increases with the back gate voltage.

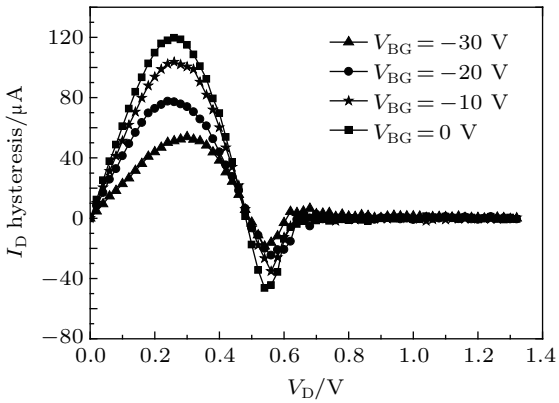


Fig. 4. $I_{\rm D}$ hysteresis versus $V_{\rm D}$ characteristics of FB PD SOI n-MOSFETs with $W = 10$ μm and $L = 0.13$ μm at $V_{\rm BG} \leq 0$ and $V_{\rm FG} = 1.0$ V.

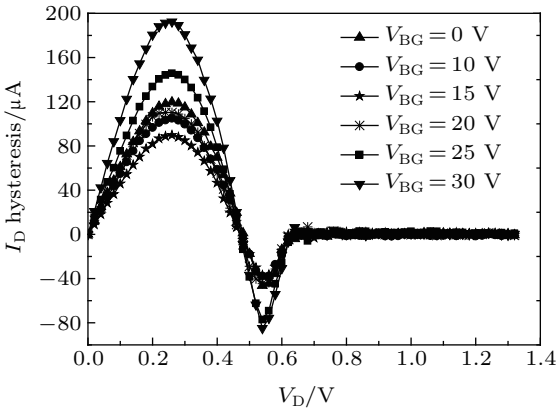


Fig. 5. $I_{\rm D}$ hysteresis versus $V_{\rm D}$ characteristics of FB PD SOI n-MOSFETs with $W = 10$ μm and $L = 0.13$ μm at $V_{\rm BG} > 0$ and $V_{\rm FG} = 1.0$ V.

To further describe the impact of back-gate bias on the hysteresis effect, we have measured the $I_{\rm D}$ hysteresis versus $V_{\rm BG}$ of the device under a fixed drain voltage. Figure 6 shows the $I_{\rm D}$ hysteresis as a function of $V_{\rm BG}$ for the FB PD SOI n-MOSFET with $W = 10$ μm and $L = 0.13$ μm, where $V_{\rm D} = 0.28$ V and $V_{\rm FG} = 1.0$ V. There are two extreme values in Fig. 6. For a back-gate voltage from −30 V to 0 V, the $I_{\rm D}$ hysteresis increases with $V_{\rm BG}$, and the maximum value appears at $V_{\rm BG} = 0$ V. When the back-gate voltage exceeds 0 V, the $I_{\rm D}$ hysteresis declines with $V_{\rm BG}$, and the minimum value is obtained at the back gate voltage around 15 V. Subsequently, the $I_{\rm D}$ hysteresis rapidly increases with $V_{\rm BG}$. As shown in Fig. 7, a similar result is obtained.

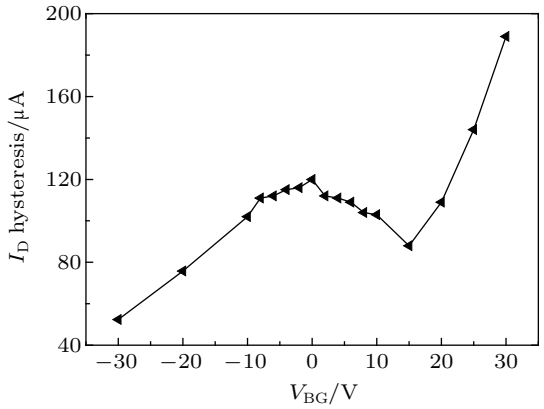


Fig. 6. $I_{\rm D}$ hysteresis versus $V_{\rm BG}$ characteristics of FB PD SOI n-MOSFETs with $W = 10$ μm and $L = 0.13$ μm at $V_{\rm D} = 0.28$ V and $V_{\rm FG} = 1.0$ V.

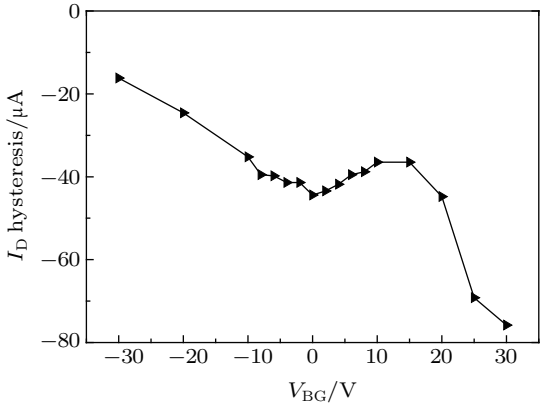


Fig. 7. $I_{\rm D}$ hysteresis versus $V_{\rm BG}$ characteristics of FB PD SOI n-MOSFETs with $W = 10$ μm and $L = 0.13$ μm at $V_{\rm D} = 0.56$ V and $V_{\rm FG} = 1.0$ V.

4.2. Mechanism of hysteresis effect in PD SOI MOSFETs at various back-gate biases

The determinants of the mechanism of the hysteresis effect are the accumulated carriers in the neu-

tral region. However, the accumulated carriers result from the equilibrium between the recombination of back interface states and the current through the body-to-source junction.

Firstly, we have to clarify the impact of back-gate bias on the recombination back interface states. The band diagram of the PD SOI n-MOSFET at different $V_{\rm BG}$ is plotted in Fig. 8. The back channel is accumulated by negative $V_{\rm BG}$, which assists the recombination of holes.[21] When $V_{\rm BG} \geq 0$ V, the back interface states under the depletion layer cannot assist the recombination of the injected holes.

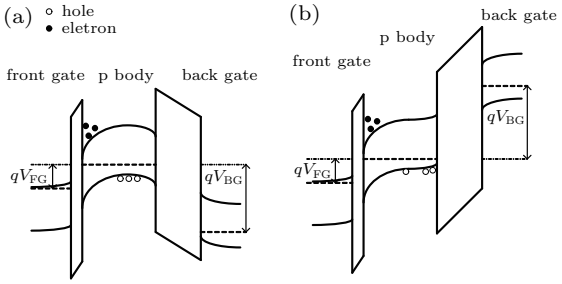


Fig. 8. Band diagram of the PD SOI n-MOSFET at different $V_{\rm BG}$. (a) $V_{\rm BG} > 0$, (b) $V_{\rm BG} < 0$.

Secondly, we have elaborated the impact of back-gate bias on the current through the body-to-source junction. To investigate the impact of the back-gate bias on the body-to-source junction, the measured body-to-source junction current ($I_{\rm BS}$) versus $V_{\rm BG}$ is shown in Fig. 9, where $V_B = 0.6$ V. The measurement is repeated several times by scanning the back gate from accumulation (−30 V) to inversion (30 V) while keeping the front gate voltage at 1.0 V. It can be clearly seen that the body-to-source current remains constant at the negative $V_{\rm BG}$. It is obvious that there is a positive current peak in the $I_{\rm BS}$–$V_{\rm BG}$ curve, as shown in Fig. 9. The current peak originates from the residue interface traps of the manufacturing process. When the forward bias is lower than the built-in voltage, the diffuse current is negligible compared with the recombination current due to the larger recombination rate.[22] The recombination of the injected excess minority carriers with the majority carriers at the Buried Si/SiO_2 interface is modulated by $V_{\rm BG}$,[23] and results in the current peak in the body-to-source junction I–V curve. The p/n$^+$ junction current peak can be interpreted by the steady-state Shockley–Read–Hall (SRH) recombination.[24,25]

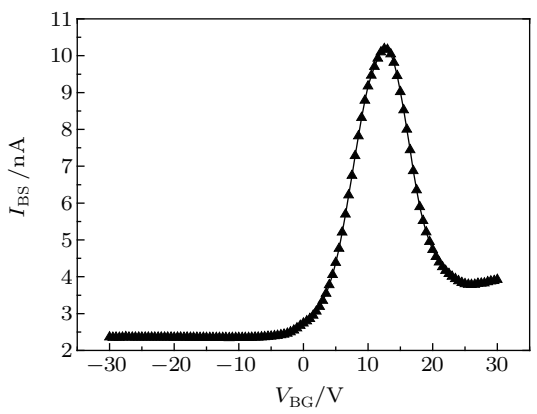


Fig. 9. $I_{\rm BS}$ versus $V_{\rm BG}$ characteristics of the TB PD SOI n-MOSFET with $W = 10$ μm and $L = 10$ μm, where the drain is floating, $V_{\rm FG} = 1.0$ V and $V_{\rm B} = 0.6$ V.

Figure 10 illustrates the cross-sectional view and the energy band diagram at the Si/SiO2 interface of a forward-biased body-source p/n$^+$ junction. Excess minority carriers are injected by the forward-biased body-source p/n$^+$ junction into the MOS-gated Si/SiO_2 interface which covers MOSFET's channel region (MCR) and body-source junction space-charge region (JSCR). The total barrier height is $V_{\rm B} = V_{\rm BI} - V_{\rm PN} - V_{\rm S}$, where the built-in potential of the p/n$^+$ junction $V_{\rm BI}$ is given by $V_{\rm BI} = (kT/q)\ln(N_{\rm Dn+}N_{\rm Ap}/n_i^2)$, $V_{\rm S}$ is the surface energy band bending, and $V_{\rm PN}$ is the forward bias voltage applied to the p/n$^+$ junction. The surface energy band bending in MCR is uniform at a fixed back gate voltage. The variation of surface energy band bending is needed to be taken into account in JSCR. For the interface trap over MCR between the body-drain and body-source JSCR, the steady-state recombination rate reaches a maximum at the back gate voltage denoted as $V_{\rm BG\text{-}peak}$, when $c_{\rm ns}N_{\rm S} = c_{\rm ps}P_{\rm S} = (c_{\rm ns}c_{\rm ps})^{1/2}n_{\rm i}\exp(qV_{\rm PN}/2kT)$.[26] Here $c_{\rm ns}$ and $c_{\rm ps}$ are the electron and hole capture rate coefficients at the interface trap, $N_{\rm S}$ and $P_{\rm S}$ are respectively the steady-state electron and hole concentration at the Si/SiO_2 interface, and $n_{\rm i}$ is the equilibrium intrinsic carrier concentration. Correspondingly, the recombination current reaches a peak, as shown in Fig. 9.

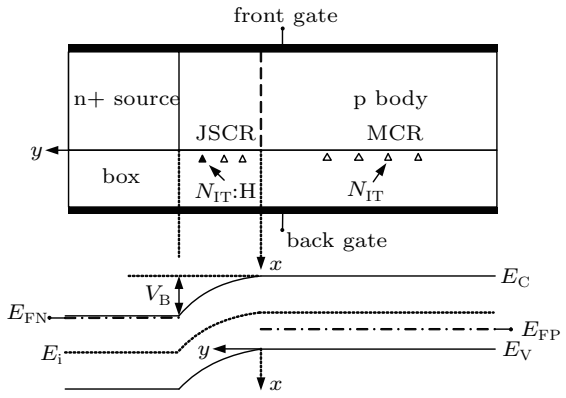


Fig. 10. Cross-sectional view of the two–dimensional energy band diagram of the body-source p/n$^+$ junction on the Si/SiO_2 interfacial plane. $N_{\rm IT}$ is the localized interface trap distribution, and $x = 0$.

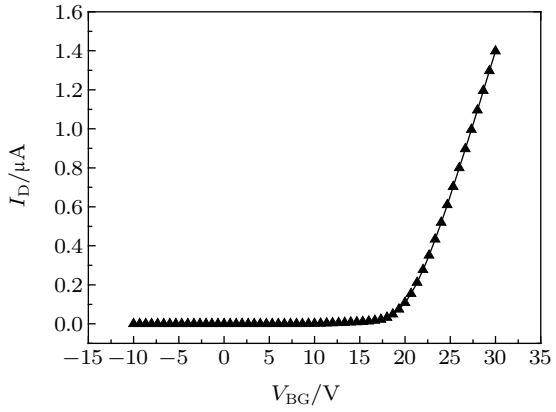


Fig. 11. Measured transfer characteristics for the back channel of the FB PD SOI n-MOSFET with $W = 10$ μm and $L = 0.13$ μm at $V_{FG} = 1.0$ V and $V_D = 1.0$ V.

The recombination current of the body-to-source junction is constant when $V_{BG} \leq 0$ V. However, the back channel is accumulated, which assists the recombination of holes. Therefore, the I_D hysteresis increases with the back-gate voltage when $V_{BG} \leq 0$ V. When $V_{BG} \geq 0$ V, the back interface states cannot assist the recombination of the injected holes. A current peak appears in the recombination current of the body-to-source junction. As a result, there is a peak of the I_D hysteresis when 0 V $\leq V_{BG} \leq$ 30 V. Moreover, the back channel will be in strong inversion, which deteriorates the hysteresis effect. The measured transfer characteristics of the back channel of the FB PD SOI n-MOSFET are shown in Fig. 11. The threshold voltage of the back channel at the drain current of 0.1 μA·W/L is measured to be 15 V. Therefore, the I_D hysteresis increases rapidly as the back gate voltage exceeds 15 V.

5. Conclusion

In this paper, we have demonstrated the hysteresis characteristics and its back gate dependence in PD SOI MOSFETs. Both positive and negative peaks are observed in the defined I_D hysteresis of FB PD SOI MOSFETs. The back channel is accumulated at $V_{BG} \leq 0$ V, which assists the recombination current of holes, leading to the increase of the I_D hysteresis with the back gate voltage. Since the recombination of injected excess minority carriers with the majority carriers at the buried Si/SiO_2 interface is modulated by V_{BG}, there is a positive peak in the recombination current of the body-to-source p/n^+ junction. Thus the I_D hysteresis is not monotonic with respect to V_{BG}. Moreover, because the back channel is in strong inversion, the I_D hysteresis increases rapidly as the back gate voltage exceeds 15 V.

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