A gate enhanced power U-shaped MOSFET integrated with a Schottky rectifier*

Wang Ying(王 颖)†, Jiao Wen-Li(焦文利), Hu Hai-Fan (胡海帆),
Liu Yun-Tao(刘云涛), and Cao Fei(曹 菲)

College of Information and Communication Engineering, Harbin Engineering University, Harbin 150001, *China*

(Received 22 September 2011; revised manuscript received 22 October 2011)

An accumulation gate enhanced power U-shaped metal-oxide-semiconductor field-effect-transistor (UMOSFET) integrated with a Schottky rectifier is proposed. In this device, a Schottky rectifier is integrated into each cell of the accumulation gate enhanced power UMOSFET. Specific on-resistances of 7.7 m$\Omega\cdot$ mm^2 and 6.5 m$\Omega\cdot$ mm^2 for the gate bias voltages of 5 V and 10 V are achieved, respectively, and the breakdown voltage is 61 V. The numerical simulation shows a 25% reduction in the reverse recovery time and about three orders of magnitude reduction in the leakage current as compared with the accumulation gate enhanced power UMOSFET.

Keywords: accumulation, Schottky source, reverse recovery time, leakage current

PACS: 61.82.Fk, 73.40.Qv, 78.40.Fy, 85.30.Fg **DOI:** 10.1088/1674-1056/21/5/056104

1. Introduction

The gate enhanced power U-shaped metal-oxide-semiconductor field-effect-transistor (GE-UMOS)[1] is a structure with ultralow on-resistance ($R_{\rm ON}$). The deep trench polysilicon electrode works as another gate electrode at the on state, so the electron current density is larger than that of the gradient oxide by-pass (GOB) structure.[2] The accumulation mode field effect transistor (ACCUFET) has been proposed to achieve a very low on-state resistance by utilizing the accumulation layer instead of the inversion layer for the MOS part in order to use the higher channel mobility.[3−6] More recently, the monolithic integration of the Schottky rectifiers has been proposed with superior turn-off speed characteristics.[7]

In this paper, we propose an accumulation gate enhanced power UMOSFET integrated with the Schottky rectifier structure (SAGE-UMOS). It has the advantages of both GE-UMOS and ACCUFET, and therefore the structure achieves an ultralow on-resistance and a high figure of merit of performance. Due to the application of the Schottky rectifier, a fast recovery speed can be realized.

The device structure described in this paper employs a cell-distributed Schottky rectifier, and thus achieves good reverse recovery characteristics while eliminating the p–n junction. The approach is to integrate a low leakage Schottky rectifier to the n-base region without compromising the performance of the accumulation gate enhanced power UMOSFET (AGE-UMOS). This improves the utilization of the wafer and makes the device very suitable for high frequency DC-DC converter applications.[8] Two-dimensional numerical simulations show a 25% reduction in the reverse recovery time and about three orders of magnitude reduction in the leakage current as compared with the AGE-UMOS. Simulation results for the proposed structure with different Schottky contact sizes in the cells are presented. By using the gate enhanced technique, a larger electron current density is generated by the polysilicon electrode working as a deep gate at the on state, so the on-resistance is much lower than that of the conventional ACCUFET.

2. Device structure and operation principle

The SAGE-UMOS structure described in this paper is shown in Fig. 1(a). In this structure, a recessed Schottky rectifier is integrated into each cell. Compared with the AGE-UMOS shown in Fig. 1(b), it not only reduces the reverse recovery time, but also lowers the leakage current. The accumulation channel devices rely on the current conduction via a surface accu-

*Project supported by the National Natural Science Foundation of China (Grant No. 60906048) and the Program for New Century Excellent Talents in University, China (Grant No. NCET-10-0052).

†Corresponding author. E-mail: wangying7711@yahoo.com

© 2012 Chinese Physical Society and IOP Publishing Ltd

mulation layer created along the oxide–semiconductor interface, and electrons from the N^+ source flow into the N-drift region through the accumulation layer created by the gate electrode. Due to the existence of the Schottky rectifier, a part of injected reverse recovery charge is eliminated through the Schottky rectifier, which enables a faster recovery. The n-base region between the trenches is not fully depleted at zero gate bias in the AGE-UMOS. When the Schottky rectifier is intergrated, the built-in potential of the Schottky rectifier creates a depletion region along the channel. The undepleted n-region area is reduced because of the application of the Schottky rectifier. As the leakage current is determined by the resistance of the undepleted n-region between source and drain, the leakage current can be greatly reduced.

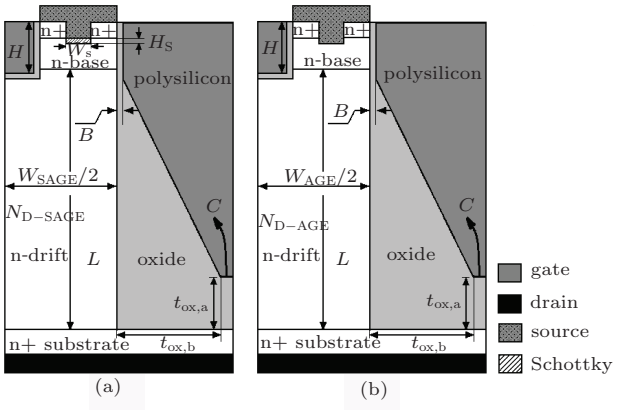


Fig. 1. Cross-sectional views of (a) SAGE-UMOS and (b) AGE-UMOS.

Table 1. Device parameters for the simulations (cell pitch=0.9 μm).

Parameter	SAGE-UMOS	AGE-UMOS
Drift region thickness L/μm	3	3
n^+ source doping/cm^{-3}	1×10^{19}	1×10^{19}
n^+ source junction depth/μm	0.4	0.4
n-base junction depth/μm	0.6	0.6
n-base peak doping N_A/cm^{-3}	1×10^{13}	1×10^{13}
Gate trench depth H/μm	1.5	1.5
Oxide thickness B/μm	0.05	0.05
Oxide thickness $t_{ox,a}$/μm	0.3	0.3
Oxide thickness $t_{ox,b}$/μm	0.3	0.3
Schottky depth H_S/μm	0.2	–
Schottky width W_S/μm	0.16	–
Oxide width C/μm	0	0

Two-dimensional numerical simulations of the AGE-UMOS and the SAGE-UMOS are performed for the case of 61 V breakdown voltage. The structural parameters are listed in Table 1.

3. Simulation results and discussion

The comparisons of reverse recovery waveform and leakage current between the AGE-UMOS and the SAGE-UMOS are shown in Fig. 2. It is clear that the integration of the cell-distributed Schottky rectifier is an effective approach to improving the switching behavior of the body diode. The reverse recovery time is 4.45×10^{-7} s and 3.32×10^{-7} s, respectively. The leakage current lowers by about three orders of magnitude as compared with that of the AGE-UMOS because of the application of the integrated Schottky rectifier. This is due to a reduction in the peak electric field at the surface caused by the depletion of the N-base region.

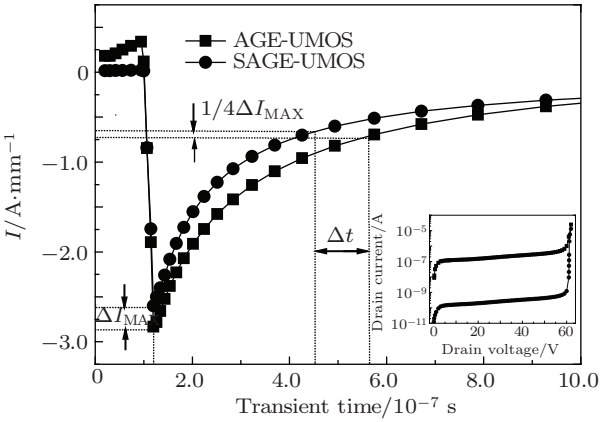


Fig. 2. Simulated body-diode reverse-recovery waveforms and leakage currents (inset) for the AGE-UMOS and the SAGE-UMOS.

The drift region doping density and thickness are chosen to support the required voltage in the off state. So the breakdown voltages and the I–V characteristics are essentially the same because of the similarity in their structures. In a power device, the substrate contribution (100 μm, 0.002 Ω·cm) is expected to add 20 μΩ·cm^2 to the device specific on-resistance.[4] For the SAGE-UMOS, specific on-resistances of 7.7 mΩ·mm^2 and 6.5 mΩ·mm^2 for gate bias voltages of 5 V and 10 V are achieved, respectively, including the substrate contribution, and with a breakdown voltage of 61 V. For the AGE-UMOS, the specific on-resistance and the breakdown voltage are definitely the same as those for the SAGE-UMOS.

The effects of the Schottky rectifier depth (H_S) on the turn-off characteristics are plotted in Fig. 3(a). These data indicate a reduction in the leakage current

as the rectifier is recessed beyond the N^+ source to the optimum depth of 0.5 μm. This is due to the reductions in the electron velocity and the electric field at the n-channel caused by the depletion of the N-base region. Any further increase in the Schottky depth beyond this optimum point results in an increase in the leakage current due to the increased leakage current over the Schottky barrier.

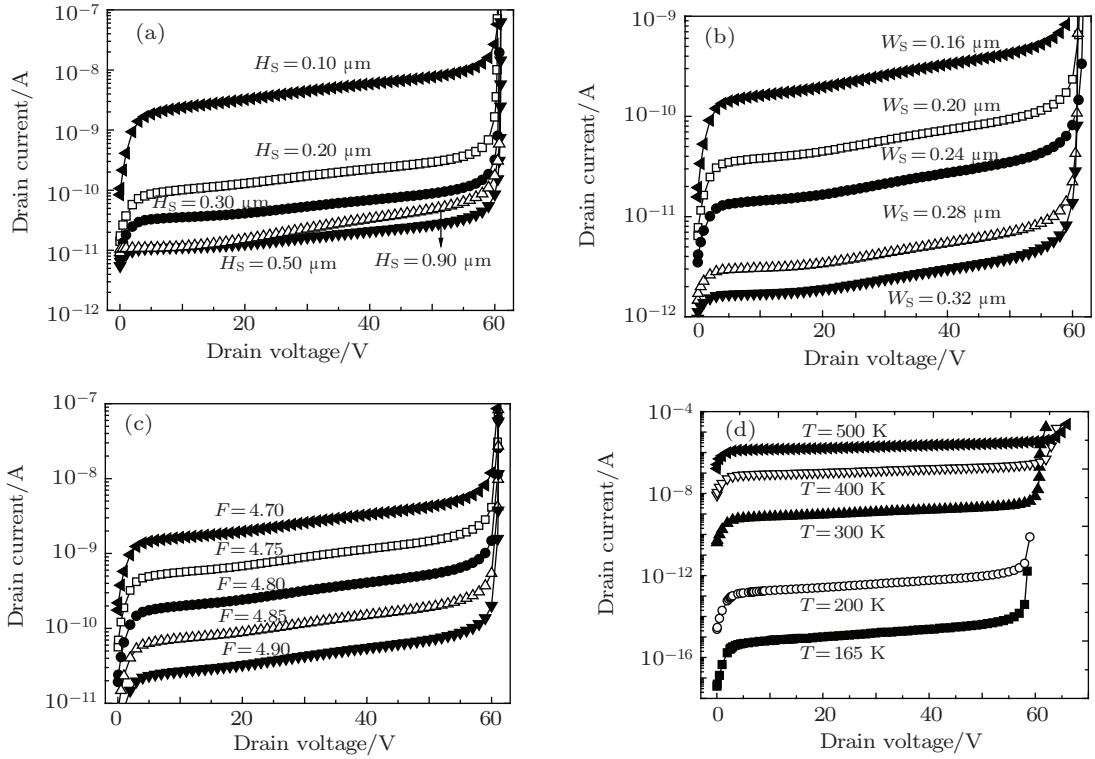


Fig. 3. (colour online) Leakage currents with different values of (a) H_S at $V_{GS} = 0$ V, Schottky workfunction of 4.81 eV, $W_S = 0.16$ μm, $T = 300$ K, (b) W_S at $V_{GS} = 0$ V, Schottky workfunction of 4.81 eV, $H_S = 0.2$ μm, $T = 300$ K, (c) Schottky workfunction F at $V_{GS} = 0$ V, $H_S = 0.2$ μm, $W_S = 0.16$ μm, $T = 300$ K, and (d) temperature T at $V_{GS} = 0$ V, $H_S = 0.1$ μm, $W_S = 0.16$ μm, Schottky workfunction of 4.81 eV.

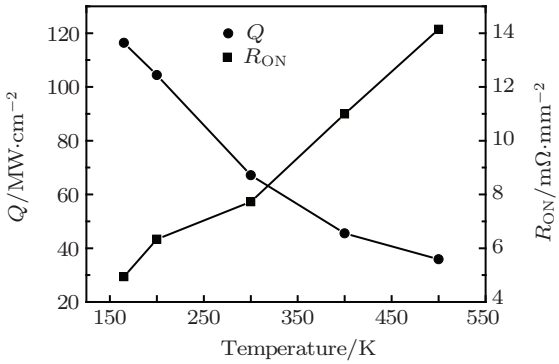


Fig. 4. Figure of merit and on-resistance versus temperature.

The leakage current can be reduced further by optimizing the width and the workfunction of the Schottky rectifier, as the leakage current is influenced not only by the Schottky depth, but also by the absolute width of the Schottky rectifier, as shown in Fig. 3(b). The Schottky barrier height has the same effect on the leakage current because of the creation of a larger potential barrier between the recessed Schottky rectifier and the gate trench. So a higher work function is favorable for the reduction of the leakage current, as shown in Fig. 3(c). Without the p–n junction, the proposed structure does not need the regular MOSFET preparation technology of forming p–n junction by high temperature diffusion,[9] so the device is more suitable for the low temperature process, which is beneficial to the formation of a better oxide layer, thereby better controlling the geometric structure. Due to the fact that the threshold voltage of the Schottky rectifier has a negative temperature coefficient, the electron concentration in the current flow path reduces with the decreasing temperature, thus leading to a lower leakage current (Fig. 3(d)) and a higher quality factor (Q) without affecting the other characteristics (Fig. 4). The quality factor is equal to the ratio of the square of the breakdown voltage to the on-resistance.[10] So the higher the value of Q, the better the performance.

Table 2. Comparision of performances among ACCUFET, VDMOS, and UMOSFET, the on-resistance is calculated at $V_{GS} = 10$ V.

Device	BV/V	R_{ON}/mΩ·cm^2	FOM/MW·cm^{-2}
Conventional ACCUFET[3]	25	0.11	5.95
Conventional VDMOS[11]	82	0.88	7.64
Conventional UMOSFET[12]	37	0.09	15.2
TPSOI VDMOS[10]	123.4	0.96	15.8
FLI-MOSFET[11]	61	0.42	8.86
LOCOS UMOS[13]	73	0.6	8.88
GE-UMOS[1]	141	0.42	47.3
SAGE-UMOS (this work)	61	0.065	57.2

The performance of the proposed structure is compared with those of the other MOSFET structures in Table 2. Except for the parameters of breakdown voltage (BV) and R_{ON}, the figures of merit (FOMs) are also provided. The comparison in Table 2 shows that the performance of the SAGE-UMOS is the best.

4. Conclusion

The SAGE-UMOS is proposed and demonstrated to be effective in improving the recovery speed and reducing the drain–source leakage current compared with the AGE-UMOS. The simulation results show a 25% reduction in the reverse recovery time and about three orders of magnitude reduction in the leakage current at the same device dimensions. By varying the parameters of the Schottky rectifier electrode and the MOSFET temperature, a further reduction in the leakage current until approaching the value of the p–n junction transistor can be obtained. In conclusion, this improved structure is expected to provide a fast recovery speed and improve the leakage current.

References

[1] Wang Y, Hu H F, Jiao W L and Cheng C 2010 *IEEE Electron Device Lett.* **31** 338

[2] Chen Y, Liang Y C and Samudra 2007 *IEEE Trans. Power Electronics* **22** 1303

[3] Baliga B J, Syau T and Venkatraman P 1992 *IEEE Electron Device Lett.* **13** 427

[4] Syau T, Venkatraman P and Baliga B J 1994 *IEEE Trans. Electron Devices* **41** 800

[5] Ueno K, Konishi K, Fujisawa Y, Sakai N, Ryoukai K and Seki Y 1998 *Proc. ISPSD* 325

[6] Tang X Y, Zhang Y M and Zhang Y M 2009 *Chin. Phys.* B **58** 495

[7] Thapar N 2006 (US patent) 7400014 [2005-07-15]

[8] Xu C, Sin J K O, Kang B W, Feng C G, Wu Y and Liu X M 2003 *IEEE Trans. Electron Devices* **50** 1422

[9] Wu L J, Hu S D, Luo X R, Zhang B and Li Z J 2011 *Chin. Phys.* B **20** 107101

[10] Ye H, Su W, Zhang B and Li Z J 2009 *Microelectronics & Electronics* 137

[11] Alves S, Morancho S, Reynes F and Lopes L M 2003 *Proc. ISPSD* 308

[12] Ono S, Kawaguchi Y and Naagawa A 2003 *ISPSD* 28

[13] Wang H, Xu H P E, Ng W T, Fukumoto K, Ishikawa A, Furukawa Y, Imai H, Naito T, Sato N, Sakai K, Tamura S and Takasuka K 2008 *IEEE Trans. Electron Devices* **29** 1239