A novel superjunction MOSFET with improved ruggedness under unclamped inductive switching*

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The ruggedness of a superjunction metal–oxide semiconductor field-effect transistor (MOSFET) under unclamped inductive switching conditions is improved by optimizing the avalanche current path. Inserting a P-island with relatively high doping concentration into the P-column, the avalanche breakdown point is localized. In addition, a trench type P+ contact is designed to shorten the current path. As a consequence, the avalanche current path is located away from the N+ source/P-body junction and the activation of the parasitic transistor can be effectively avoided. To verify the proposed structural mechanism, a two-dimensional (2D) numerical simulation is performed to describe its static and on-state avalanche behaviours, and a method of mixed-mode device and circuit simulation is used to predict its performances under realistic unclamped inductive switching. Simulation shows that the proposed structure can endure a remarkably higher avalanche energy compared with a conventional superjunction MOSFET.

Keywords: avalanche current path, unclamped inductive switching, superjunction, MOSFET

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1. Introduction

Power metal–oxide semiconductor field-effect transistors (MOSFETs) are widely used as switches in power electronic systems. Not only are they required to have low conduction and switching losses, they should also be rugged enough under high electrical stress conditions. An unclamped inductive switching (UIS) has been considered as an extremely severe condition for a power MOSFET because all of the energy stored in the inductor during the on-state is dumped into the MOSFET when it is turned off.[1] Therefore, the UIS test is usually used to evaluate device ruggedness in terms of the maximum avalanche energy in a single pulse ($E_{\rm AS}$) that the device can endure prior to destructive breakdown.[2] The failure of a power MOSFET during a UIS test is due mainly to the activation of the parasitic bipolar transistor (BJT), which increases the current and raises the junction temperature, and eventually forces the device into thermal runaway condition.[3]

In order to suppress the activation of the parasitic BJT in a MOSFET, several methods have been reported.[2,4,5] One way is to reduce the resistance of the P-body beneath the N+ source using high-energy boron implantation or deep diffusion.[4] The other is to divert the avalanche current direction from the edge to the bottom of the P-body by employing a split-well structure[5] or a segmented trench body contact.[2] The first kind of method has been widely used so far to improve device $E_{\rm AS}$. However, the second kind is intriguing since the forward bias of the parasitic BJT base/emitter junction can be completely avoided in theory.

The superjunction (SJ) structure has been proposed to reduce power MOSFET on-state resistance and conduction loss.[6−12] By implementing the charge compensation principle, it breaks the "silicon limit" of power MOSFETs. From the application viewpoint, the device reliability is a critical criterion. Improving the robustness of SJ-MOSFETs, especially under UIS conditions, has become one of the most important issues for researchers.[13] In the present paper, we propose a novel structure with an optimized avalanche current path (OACP), which can improve the $E_{\rm AS}$ by changing the avalanche current path. The avalanche current is located away from the N+ source/P-body

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junction and triggering of the parasitic BJT can be effectively avoided.

To verify the OACP-SJ mechanism, a two-dimensional (2D) numerical simulation is performed to describe its static and on-state avalanche behaviours. To predict the E_{AS} of the OACP-SJ under realistic UIS conditions, we investigate its performances in a UIS test circuit with a method of mixed-mode device and circuit simulation. Since the OACP-SJ has a higher maximum E_{AS} than a conventional SJ-MOSFET, it provides an attractive idea to improve the reliability of SJ-MOSFETs.

2. Device structure and process

The proposed OACP-SJ structure is shown in Fig. 1(a) comparing a conventional SJ structure in Fig. 1(b). Also shown are the inherent parasitic devices in the structures. The BJT consists of a N+ source (emitter), a P-body (base), and a N– drift region (collector). R_b represents the P-body resistance connected to the BJT base terminal. Although only one BJT and one resistor are shown in the plot, the structure should be regarded as a series-connected network of BJTs and resistors starting from the channel region and ending at the P+ contact. The BJT closest to the MOS channel experiences the largest base resistance and will be the first one to turn on in the presence of an avalanche current.[1]

In a conventional SJ-MOSFET, the avalanche current generally passes through the P-body underneath the N+ source to the P+ contact, and creates a voltage drop across R_b. When this voltage drop approaches the built-in potential of the N+ source/P-body junction, the parasitic BJT will be triggered. The avalanche current path in our structure, in contrast, is changed by inserting a P-island with a relatively high doping concentration into the P-column. Meanwhile, a trench-type P+ contact is designed to shorten the current path. Consequently the avalanche current path is located away from the N+/P-body junction and, therefore, the parasitic BJT is more difficult to activate.

The process of an OACP-SJ MOSFET is similar to a conventional SJ MOSFET; no additional mask is needed. In order to obtain the OACP structure, a window is open in the passivation layer over the P+ region. Then reactive ion etching (RIE) is implemented as a silicon etcher. Following the trench formation is a two-step ion implantation with different energies and doses. The P-island is accomplished by the high energy and low dose, and the P+ Ohmic contact region by the low energy and high dose. Finally, the N+ source and P+ contact are fabricated by metallization.

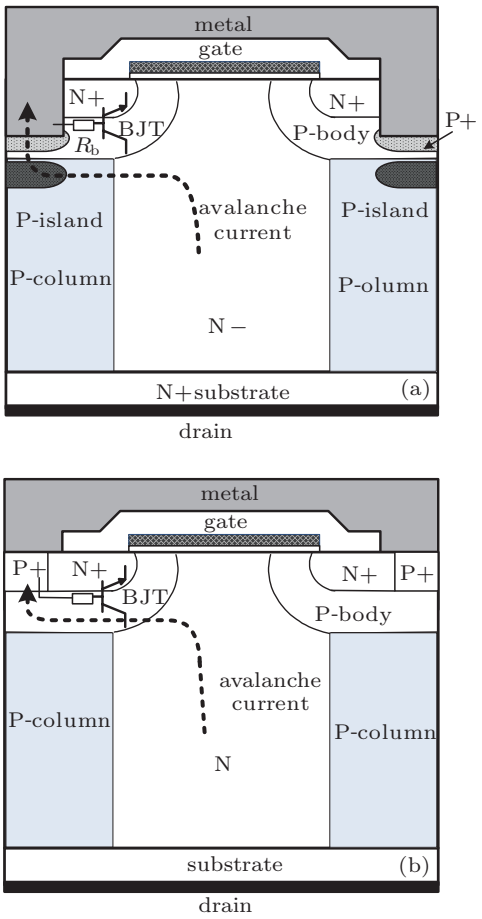


Fig. 1. Schematic cross-section views of the proposed OACP-SJ MOSFET (a) and the conventional SJ MOSFET (b).

3. Simulation and discussion

3.1. Static avalanche breakdown and current path

To verify the proposed structural mechanism, a 2D numerical simulation is performed by using the MEDICI package. The 2D structures in Fig. 1 were divided into non-uniform triangular grids, and then the fundamental semiconductor equations were solved on the nodes.[14] Thus the electrical characteristics of the devices can be obtained. The physical parameters used in the simulations are listed in Table 1. The OACP-SJ and the conventional SJ have the same N-epi and P-body doping concentrations. As a P-island with a relatively high doping concentration is introduced, the P-column doping concentration of the OACP-SJ is slightly lower than that of the conventional SJ in order to maintain charge balance.

Table 1. Main device parameters of the conventional SJ-MOSFET and the proposed OACP-SJ MOSFET.

Parameters	OACP-SJ MOSFET	conventional SJ-MOSFET
N-epi thickness/μm	7.0	7.0
N-epi doping concentration/cm^{-3}	1×10^{16}	1×10^{16}
P-column doping concentration/cm^{-3}	2.8×10^{16}	3.0×10^{16}
P-column width/μm	0.8×2	0.8×2
P-island doping concentration/cm^{-3}	8×10^{18}	–
P-island width/μm	0.6×2	–
Cell size/μm	5.0	5.0

As shown in Fig. 2, when their gate-source voltage (V_{gs}) values are equal to zero, the first breakdown (avalanche breakdown) voltages of the conventional SJ and the OACP-SJ with the same N-epi doping concentration are 133 V (point A) and 121 V (point C), respectively. The OACP-SJ has a slight degeneration of the static avalanche breakdown voltage, because the SJ structure is strictly based on the charge compensation principle, and the presence of the P-island inevitably has a negative effect on the charge balance.[15,16] The first breakdown voltage determines the device operating range and is nondestructive. However, the second breakdown is destructive, so a rugged power MOSFET is expected to have a high second breakdown voltage. The second breakdown (snap-back point on the I–V curves) voltage of the OACP-SJ (point D) is higher than that of the conventional SJ (point B). Therefore, the proposed structure has an improved robustness when $V_{gs} = 0$.

For the conventional SJ, the avalanche breakdown appears at the edge of the P-body, which is shown in Fig. 3. The avalanche current flows through the P-body underneath the N+ source and reaches the P+ contact area. The avalanche current path in the OACP-SJ corresponding to point C is shown in Fig. 4(a). The current, passing through the P-island, goes into the grooved P+ contact area directly. The reason why the avalanche current path can be changed is that an electric field peak is introduced by the P-island into the OACP-SJ depletion region. As shown in Figs. 4(b) and 4(c), the maximal electric field and the maximal impact ionization rate are at the P-islands. Therefore, avalanche breakdown occurs at the P-island, and the carriers will follow the shortest path to the P+ contact. The P-island doping concentration should be optimized. If the doping concentration is insufficient, an adequate electric field peak cannot be achieved and thus the avalanche breakdown point cannot be located at the P-island; however, if the doping concentration is excessive, the avalanche breakdown voltage will be sharply dragged down.

Since the P-island has a relatively high doping concentration and the current path to the contact is shortened, it is more difficult for the parasitic BJT in the OACP-SJ to activate. The device current distributions corresponding to the second breakdown are shown in Fig. 5. In those cases, the currents flowing into the source contact are no longer carried purely by the holes generated by the avalanche breakdown. The currents provided by the parasitic NPN transistors also play a role here.

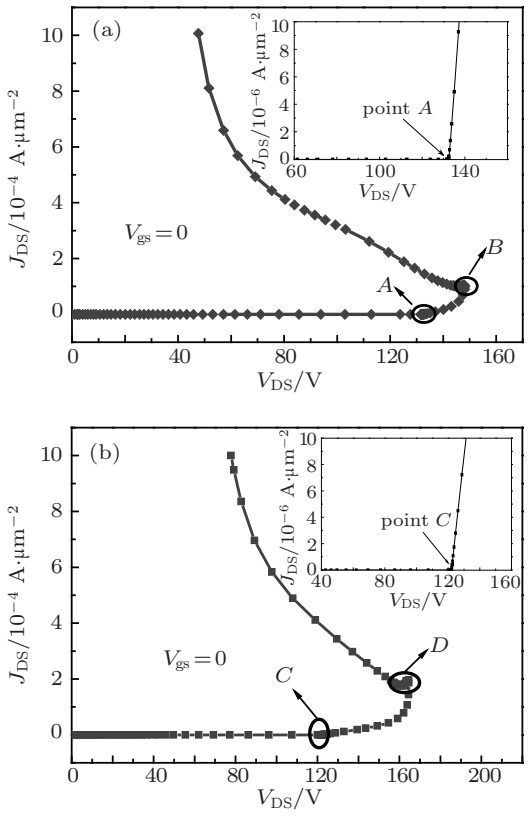
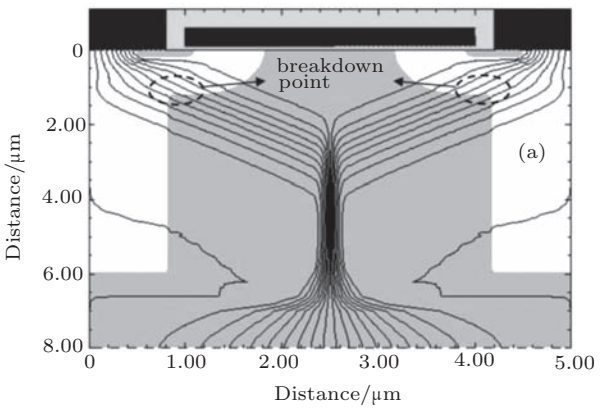
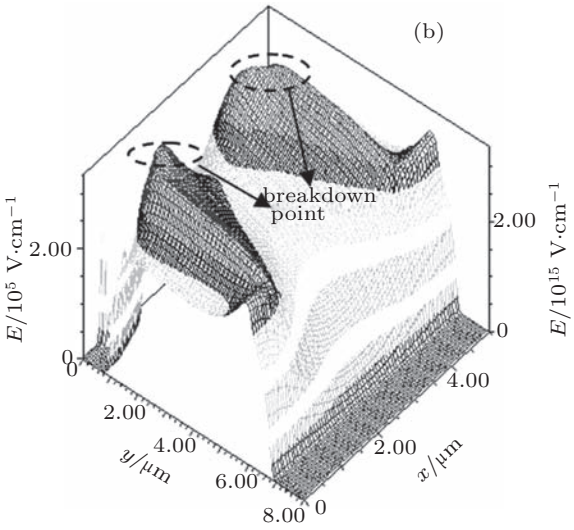


Fig. 2. Simulated forward I–V curves of the conventional SJ (a) and the OACP-SJ (b) when $V_{gs} = 0$. Points A and C correspond to the first breakdown; points B and D correspond to the second breakdown.





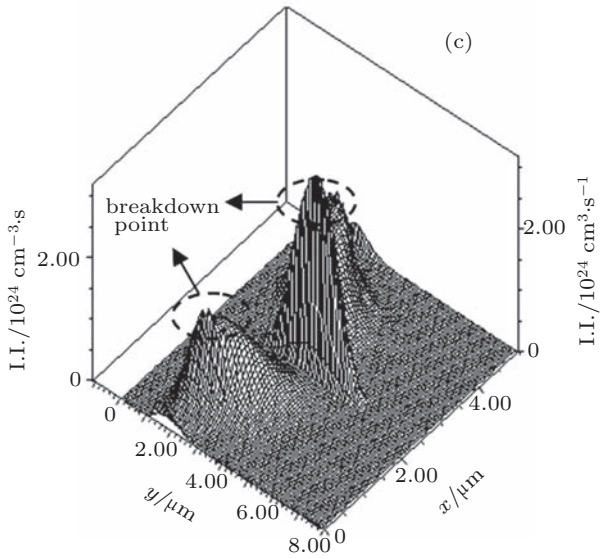
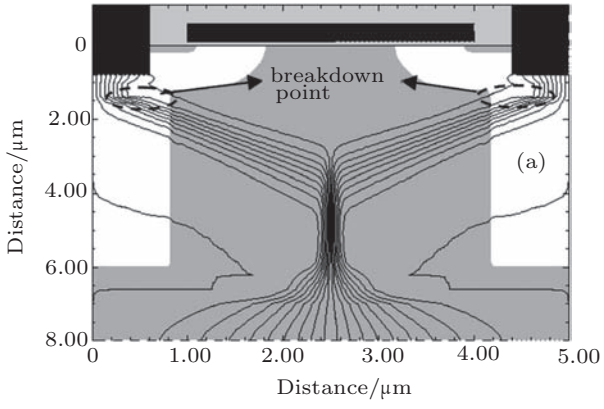
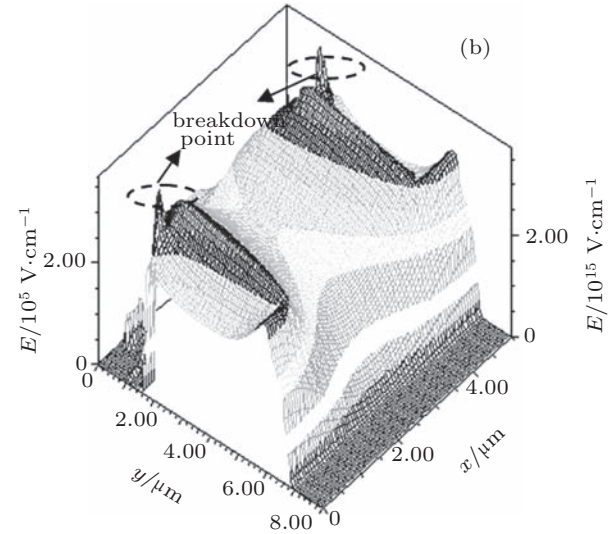


Fig. 3. (a) Avalanche current of the conventional SJ MOSFET corresponding to point A in Fig. 2; (b) electric field distribution of the conventional SJ corresponding to point A; (c) impact ionization (I.I.) rate distribution of the conventional SJ corresponding to point A.





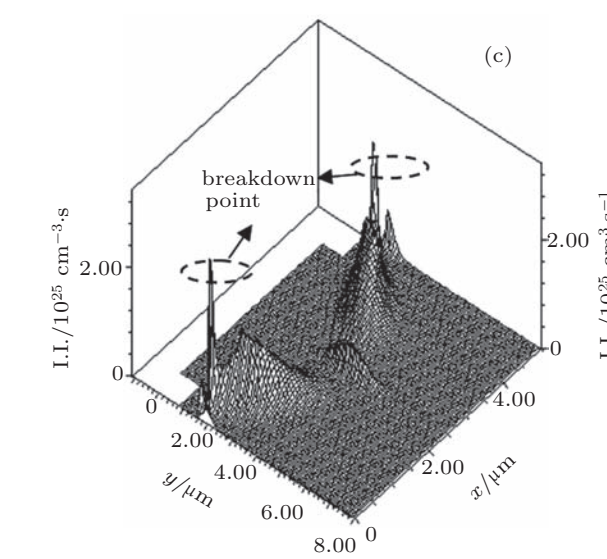


Fig. 4. (a) Avalanche current of the OACP-SJ corresponding to point C in Fig. 2; (b) electric field distribution of the OACP-SJ corresponding to point C; (c) impact ionization rate distribution of the OACP-SJ corresponding to point C.

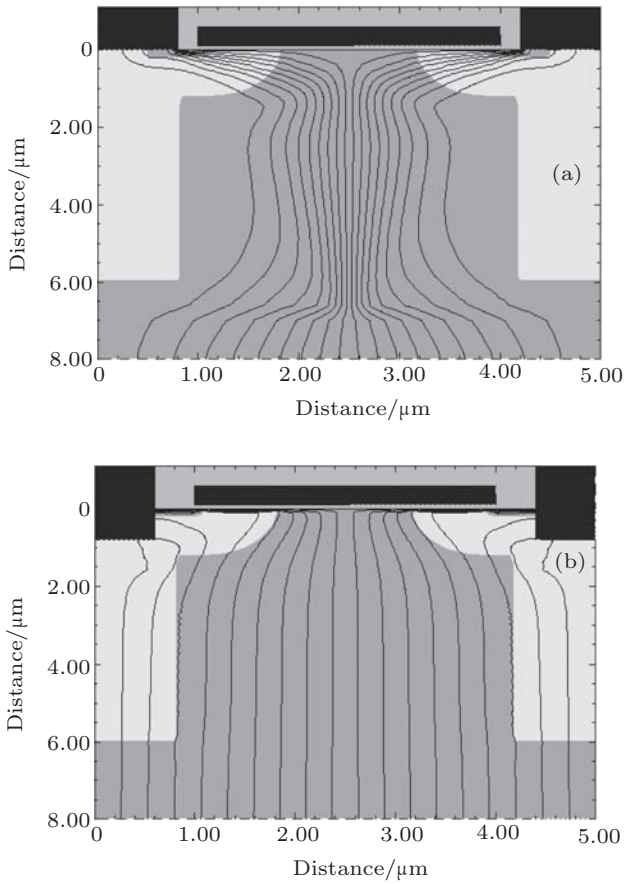


Fig. 5. (a) Avalanche currents of the conventional SJ corresponding to point B in Fig. 2 (a); (b) avalanche currents of the OACP-SJ corresponding to point D in Fig. 2(b).

3.2. On-state breakdown characteristics

The OACP-SJ on-state breakdown characteristics are also studied. As shown in Fig. 6(a), the first breakdown voltage of the conventional SJ decreases dramatically when a positive voltage is applied to its gate ($V_{gs} > 0$). The higher the value of V_{gs}, the lower the breakdown voltage is. This is because the high density electron current, flowing from the source electrode through the channel to the drain electrode, narrows down the positive space charge region in the N– drift region, and thus severely disturbs the charge balance between the P-column and the N– drift regions. Therefore, the parasitic BJT must be turned on in advance, resulting in a decrease in the second breakdown voltage.

The OACP-SJ also has undesired decreases in the first and second breakdown voltages when $V_{gs} > 0$. However, the decreasing amplitude is much smaller than that of the conventional SJ, as shown in Fig. 6(b). The reason is that the initial N– drift doping concentration in the OACP-SJ, relative to the P-column doping concentration, is slightly higher than the value required by the charge balance rule. The extra electrons in the on-state counteract some excessive positive space charges in the N– drift and suppress the imbalance to some extent. We can expect that the OACP-SJ is also more rugged than the conventional SJ when $V_{gs} > 0$. It yields a prominent advantage of the OACP-SJ for switching applications.

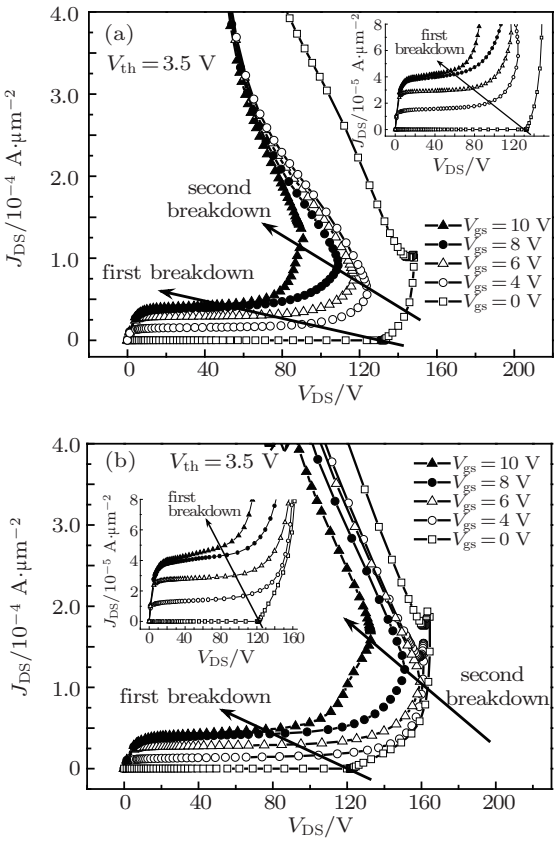


Fig. 6. Simulated forward I–V curves of the conventional SJ (a) and the OACP-SJ (b) with different values of V_{gs} applied. The roughness arrow lines indicate the reducing trend of the breakdown voltages.

3.3. Unclamped inductive switching

A mixed-mode device and circuit simulation[15] was used to predict the devices' performances under realistic UIS conditions with the help of the MEDICI package. The Kirchhoff equations describing the circuit and the semiconductor equations describing the devices are solved as a coupled set. The UIS test circuit[1,2] is demonstrated in Fig. 7. The device-under-test (DUT) is the OACP-SJ/conventional SJ composed of 10^3 cells in parallel with the main parameters in Table 1. The load inductor L is unclamped since there is no free-wheeling diode to discharge its current.

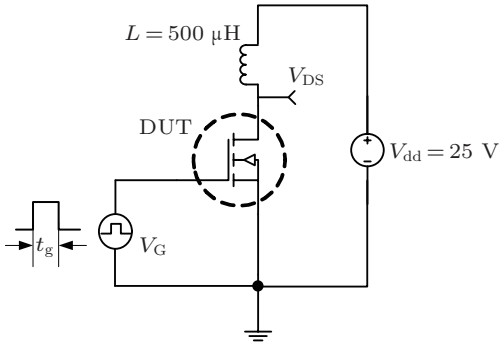


Fig. 7. The UIS test schematic circuit.

The device characteristics are sensitive to the temperature, so the self-heating effect and temperature-dependent device models, such as temperature-dependent mobility, temperature-dependent impact ionization, have been considered in the simulation. The increase in lattice temperature due to current flow and carriers recombination is included self-consistently in the solution of the device equation. To solve the heat equation, the lattice temperature at the bottom of the device is set as the environment temperature. The criterion for the destruction is defined as that the maximum lattice temperature in the device is higher than the epitaxial layer's intrinsic temperature. Here it is set to be 550 K.

The simulated UIS waveforms are shown in Fig. 8. First, a positive pulse (V_G) is applied to the DUT gate to turn it on. The current (I_{DS}) passing through the DUT and the inductor increases linearly with a rate

$$\mathrm{d}i/\mathrm{d}t = \frac{V_{dd}}{L}, \tag{1}$$

where V_{dd} is the rail voltage and L is the inductance, respectively. In this stage, drain-source currents in the OACP-SJ ($I_{DS-OACP}$) and in the conventional SJ ($I_{DS-Conv}$) are approximately identical. After a duration t_g, both $I_{DS-OACP}$ and $I_{DS-Conv}$ are charged to peak I_p. At this point the DUT is turned off. All energy stored in the inductor is dissipated in the DUT. Both the induced voltage and the V_{dd} exert on the DUT and force it into the avalanche breakdown condition. The drain-source voltage of the DUT (V_{DS}) is rapidly raised to the instantaneous peak value (V_p), which is approximately equal to its first breakdown voltage (BV). If the parasitic BJT is not activated by the avalanche current, I_{DS} will gradually decay from I_p to zero with the discharging rate

$$\mathrm{d}i/\mathrm{d}t = \frac{V_p - V_{dd}}{L} \approx \frac{BV - V_{dd}}{L}. \tag{2}$$

Hence the total energy the DUT resists is

$$E_{AS} = \frac{LI_p^2}{2}\frac{V_p}{V_p - V_{dd}} \approx \frac{LI_p^2}{2}\frac{BV}{BV - V_{dd}}. \tag{3}$$

In Fig. 8(a), t_g is set as 20 μs to charge I_p up to 1 A. The waveforms show that both devices can withstand the avalanche energy because the discharge currents gradually decay to zero with the rate in Eq. (2). The discharge time of the OACP-SJ is slightly larger than that of the conventional SJ because of its lower BV.

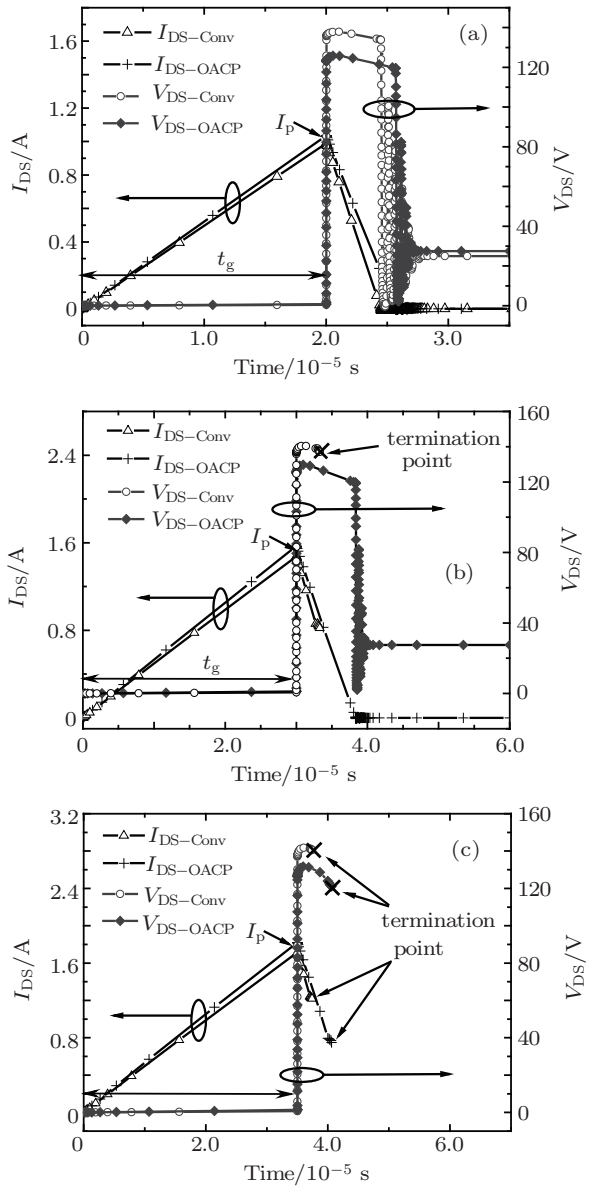


Fig. 8. Simulated waveforms of the OACP-SJ and the conventional SJ under UIS with different values of t_g: t_g = 20 μs (a), 30 μs (b), and 35 μs (c). $I_{DS-OACP}$ and $V_{DS-OACP}$ are the OACP-SJ drain-source current and voltage, respectively. $I_{DS-Conv}$ and $V_{DS-Conv}$ are the conventional SJ drain-source current and voltage, respectively.

However, if the parasitic BJT is activated, the avalanche current will be amplified by the BJT and

the lattice temperature will increase to the destructive temperature. In Fig. 8(b), t_g is 30 μs and I_P is 1.5 A. The OACP-SJ waveform is normal. However, the conventional SJ reaches the destructive temperature and the simulation terminates. That is, the OACP-SJ can handle 1.5 A discharging current but the conventional SJ cannot. In Fig. 8(c), t_g and I_p are 35 μs and 1.75 A, respectively. Both devices reach their destructive temperatures. Therefore, the simulated maximum E_{AS} of the OACP-SJ is approximately enhanced by 38% because the avalanche failure current increases from 1.5 A to 1.75 A.

4. Conclusion

In order to improve the ruggedness of SJ-MOSFETs under UIS conditions without incurring additional cost, we propose and study a novel structure with an optimized avalanche current path. The avalanche current path is located away from the N+ source/P-body junction and activation of the parasitic transistor can be effectively avoided. Simulation shows that E_{AS} of the OACP-SJ increases by 38%, though its static avalanche breakdown voltage decreases by 9%, and it has a better on-state breakdown characteristic. The process of the OACP-SJ is completely compatible with that of the conventional SJ, without using additional masks. In addition, the trench-type source contact can help reduce the device's on-state resistance by reducing the contact resistances. Consequently, the proposed OACP structure is a promising candidate as a highly reliable SJ-MOSFET.

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