Analytical model including the fringing-induced barrier lowering effect for a dual-material surrounding-gate MOSFET with a high-κ gate dielectric*

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By solving Poisson's equation in both semiconductor and gate insulator regions in the cylindrical coordinates, an analytical model for a dual-material surrounding-gate (DMSG) metal–oxide semiconductor field-effect transistor (MOSFET) with a high-κ gate dielectric has been developed. Using the derived model, the influences of fringing-induced barrier lowering (FIBL) on surface potential, subthreshold current, DIBL, and subthreshold swing are investigated. It is found that for the same equivalent oxide thickness, the gate insulator with high-κ dielectric degrades the short-channel performance of the DMSG MOSFET. The accuracy of the analytical model is verified by the good agreement of its results with that obtained from the ISE three-dimensional numerical device simulator.

Keywords: high-k gate dielectric, fringing-induced barrier lowering, analytical model

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1. Introduction

The surrounding-gate metal–oxide semiconductor field-effect transistor (MOSFET) has been recognized as one of the most promising candidates to continue complementary metal–oxide semiconductor (CMOS) performance boosting beyond the conventional scaling limit.[1,2] In order to enhance immunity against the short-channel effects (SCEs) in the surrounding-gate MOSFET, a new structure called a dual-material surrounding-gate (DMSG) MOSFET has been proposed.[3] It has been demonstrated that the DMSG MOSFET can effectively suppress the SCEs and simultaneously improve the carrier transport efficiency.[4−6]

As the channel length of the surrounding-gate MOSFET scales into the sub-100 nm regime, the gate oxide thickness is projected to be 1.5 nm or below. Such an ultra-thin gate oxide will induce a high direct tunneling gate leakage current. This resulting leakage current will increase the power dissipation and deteriorate the device performance and circuit stability for very-large-scale integration (VLSI) circuits.[7,8] To solve this problem, various high dielectric constant (high-κ) materials have been presented as alternative gate insulators to replace the conventional SiO_2.[9,10] With the same effective oxide thickness (EOT), a higher κ means a greater physical thickness, which can effectively prevent direct gate tunneling. However, a too large physical thickness will bring about a phenomenon known as the fringing-induced barrier lowering (FIBL) effect, which will induce threshold behavior degradation.[11,12]

In order to investigate the FIBL effect of a DMSG MOSFET with a high-κ gate dielectric (HDMSG), based on the fully resultant solution of Poisson's equation for both the gate dielectric layer and the silicon depletion region in the cylindrical coordinates, an FIBL-included, physical, and analytical model is derived in this paper. With the derived model, the influence of the FIBL on the HDMSG's short channel performance is thoroughly examined. The model results are verified by comparing them with the simulated results obtained from the ISE three-dimensional (3D) numerical device simulator.

2. Model derivation

Figure 1 shows the structure of the HDMSG. Considering the gate structure, the channel can be divided into two parts. The lengths of the two metals M_1 and M_2 are L_1 and $(L_2 - L_1)$, respectively. The symmetry of the structure ensures that the po-

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tential and the electric field have no variation with angle in the plane of the radial direction, hence, a two-dimensional analysis is sufficient. Since the channel is undoped (or lightly doped), in the subthreshold region, both fixed and mobile charge densities are negligible.[13] The oxide charge density is assumed to be zero for simplicity.[14−17] Then the electrostatic potential $\phi(r,z)$ in both the silicon channel and the gate dielectric regions can be written as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\phi_j\left(r,z\right)\right)+\frac{\partial^2}{\partial z^2}\phi_j\left(r,z\right)=0,\quad j=1,2. \tag{1}$$

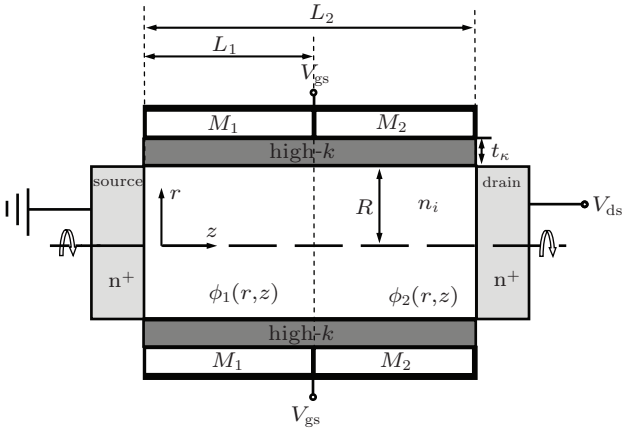


Fig. 1. Cross-section view of the HDMSG.

Assuming that the source and the drain junctions are abrupt, the boundary conditions are given as follows: (i) at the gate end,

$$\phi_j\left(r=R_i,z\right)=V_{\rm gs}-\phi_{\rm MS}^{(j)},\quad j=1,2; \tag{2}$$

(ii) at the source end,

$$\phi_1\left(r,z=0\right)=\begin{cases}V_{\rm bi}, & 0\le r\le R,\\ V_{\rm bi}+(V_{\rm gs}-\phi_{\rm MS}^{(1)}-V_{\rm bi})\dfrac{\ln(r/R)}{\ln(R_i/R)}, & R\le r\le R_i;\end{cases} \tag{3}$$

(iii) at the drain end,

$$\phi_2(r,z=L_2)=\begin{cases}V_{\rm bi}+V_{\rm ds}, & 0\le r\le R,\\ V_{\rm bi}+V_{\rm ds}+(V_{\rm gs}-\phi_{\rm MS}^{(2)}-V_{\rm bi}-V_{\rm ds})\dfrac{\ln(r/R)}{\ln(R_i/R)}, & R\le r\le R_i;\end{cases} \tag{4}$$

(iv) at $z=L_1$, the electrostatic potential is continuous

$$\phi_1(r,z=L_1)=\phi_2(r,z=L_1), \tag{5}$$

and the electric flux is continuous

$$\left.\frac{\partial\phi_1\left(r,z\right)}{\partial z}\right|_{z=L_1}=\left.\frac{\partial\phi_2\left(r,z\right)}{\partial z}\right|_{z=L_1}, \tag{6}$$

where $R_i=R+t_\kappa$, $\phi_{\rm MS}^{(j)}$ is the work function, and $V_{\rm bi}$ is the build-in voltage.

Using the superposition method, the electrostatic potential $\phi(r,z)$ can be written as

$$\phi_j(r,z)=W_j(r)+V_{\rm L}^{(j)}(r,z)+V_{\rm R}^{(j)}(r,z),\quad j=1,2, \tag{7}$$

where $V_{\rm L}^{(j)}(r,z)$ and $V_{\rm R}^{(j)}(r,z)$ are solutions of Eq. (1) and satisfy the source and the drain boundary conditions (3) and (4), respectively. Moreover, they also satisfy the continuous boundary conditions (5) and (6) of the electric flux and the electric potential at the interface between the silicon channel and the gate dielectric. Based on the results in Ref. [18], we can choose $W_j(r)=V_{\rm gs}-\phi_{\rm MS}^{(j)}$. Therefore, $V_{\rm L}^{(j)}(r,z)$ and $V_{\rm R}^{(j)}(r,z)$ can be written as

$$V_{\rm L}^{(j)}(r,z)=\sum_{n=1}^{\infty}b_n^{(j)}B_n^{(j)}(r,z),\quad j=1,2, \tag{8}$$

$$V_{\rm R}^{(j)}(r,z)=\sum_{n=1}^{\infty}c_n^{(j)}C_n^{(j)}(r,z),\quad j=1,2 \tag{9}$$

with

$$B_n^{(1)}(r,z)=\begin{cases}{\rm J}_0(\alpha_n r)\dfrac{\sinh[\alpha_n(L_1-z)]}{\sinh(\alpha_n L_1)}, & 0\le r\le R,\\ {\rm J}_0(\alpha_n R)T(r)\dfrac{\sinh[\alpha_n(L_1-z)]}{\sinh(\alpha_n L_1)}, & R\le r\le R_i,\end{cases} \tag{10}$$

$$C_n^{(1)}(r,z)=\begin{cases}\mathrm{J}_0(\alpha_n r)\dfrac{\sinh(\alpha_n z)}{\sinh(\alpha_n L_1)}, & 0\le r\le R,\\ \mathrm{J}_0(\alpha_n R)T(r)\dfrac{\sinh(\alpha_n z)}{\sinh(\alpha_n L_1)}, & R\le r\le R_i,\end{cases} \tag{11}$$

$$B_n^{(2)}(r,z)=\begin{cases}\mathrm{J}_0(\alpha_n r)\dfrac{\sinh[\alpha_n(L_2-z)]}{\sinh[\alpha_n(L_2-L_1)]}, & 0\le r\le R,\\ \mathrm{J}_0(\alpha_n R)T(r)\dfrac{\sinh[\alpha_n(L_2-z)]}{\sinh[\alpha_n(L_2-L_1)]}, & R\le r\le R_i,\end{cases} \tag{12}$$

$$C_n^{(2)}(r,z)=\begin{cases}\mathrm{J}_0(\alpha_n r)\dfrac{\sinh[\alpha_n(z-L_1)]}{\sinh[\alpha_n(L_2-L_1)]}, & 0\le r\le R,\\ \mathrm{J}_0(\alpha_n R)T(r)\dfrac{\sinh[\alpha_n(z-L_1)]}{\sinh[\alpha_n(L_2-L_1)]}, & R\le r\le R_i,\end{cases} \tag{13}$$

$$T(r)=\frac{\mathrm{J}_0(\alpha_n r)\mathrm{Y}_0(\alpha_n R_i)-\mathrm{J}_0(\alpha_n R_i)\mathrm{Y}_0(\alpha_n r)}{\mathrm{J}_0(\alpha_n R)\mathrm{Y}_0(\alpha_n R_i)-\mathrm{J}_0(\alpha_n R_i)\mathrm{Y}_0(\alpha_n R)}, \tag{14}$$

where $\mathrm{J}_i(x)$ is the Bessel function of order i, $\mathrm{Y}_i(x)$ is the Neumann function of order i, eigenvalue α_n is determined by the continuous boundary conditions of the electric flux and the electric potential at the interface between the silicon channel and the gate dielectric

$$\varepsilon_{\mathrm{si}}\frac{\mathrm{J}_1(\alpha_n R)}{\mathrm{J}_0(\alpha_n R)}=\varepsilon_i\frac{\mathrm{J}_1(\alpha_n R)\mathrm{Y}_0(\alpha_n R_i)-\mathrm{J}_0(\alpha_n R_i)\mathrm{Y}_1(\alpha_n R)}{\mathrm{J}_0(\alpha_n R)\mathrm{Y}_0(\alpha_n R_i)-\mathrm{J}_0(\alpha_n R_i)\mathrm{Y}_0(\alpha_n R)}. \tag{15}$$

It has already been demonstrated that $B_n^{(j)}(r,z=0)$ and $C_n^{(j)}(r,z=L)$ satisfy the following orthogonality relationship:[13]

$$\int_0^{R_i}B_n^{(j)}(r,0)B_m^{(j)}(r,0)\varepsilon(r)r\,\mathrm{d}r=0,\quad n\ne m, \tag{16}$$

$$\int_0^{R_i}C_n^{(j)}(r,L)C_m^{(j)}(r,L)\varepsilon(r)r\,\mathrm{d}r=0,\quad n\ne m. \tag{17}$$

Using source/drain boundary conditions (3) and (4) and orthogonal relationships (16) and (17), we can determine $b_n^{(1)}$ and $c_n^{(2)}$ as

$$b_n^{(1)}=\frac{\int_0^{R_i}(\phi_1(r,0)-W_1(r))B_n^{(1)}(r,z=0)\varepsilon(r)r\,\mathrm{d}r}{\int_0^{R_i}[B_n^{(1)}(r,z=0)]^2\varepsilon(r)r\,\mathrm{d}r}=(V_{\mathrm{gs}}-\phi_{\mathrm{MS}}^{(1)}-V_{\mathrm{bi}})E_n, \tag{18}$$

$$c_n^{(2)}=\frac{\int_0^{R_i}(\phi_2(r,z=L_2)-W_2(r))C_n^{(2)}(r,z=L_2)\varepsilon(r)r\,\mathrm{d}r}{\int_0^{R_i}[C_n^{(2)}(r,z=L_2)]^2\varepsilon(r)r\,\mathrm{d}r}=(V_{\mathrm{gs}}-\phi_{\mathrm{MS}}^{(2)}-V_{\mathrm{bi}}-V_{\mathrm{ds}})E_n \tag{19}$$

with

$$E_n=\frac{\left\{\dfrac{-\varepsilon_{\mathrm{si}}R\mathrm{J}_1(\alpha_n R)}{\alpha_n}+\dfrac{\varepsilon_i A\mathrm{J}_0(\alpha_n R)}{\alpha_n^2}\left[\dfrac{\alpha_n R}{D}-\dfrac{1}{\ln(R_i/R)A}\right]\right\}}{\left\{\begin{array}{c}\dfrac{\varepsilon_{\mathrm{si}}R^2}{2}\left\{[\mathrm{J}_1(\alpha_n R)]^2+[\mathrm{J}_0(\alpha_n R)]^2\right\}\\ +\dfrac{\varepsilon_i R^2}{2}\mathrm{J}_0{}^2(\alpha_n R)A^2\left[\dfrac{4}{\pi^2\alpha_n{}^2R^2}-\dfrac{1}{A^2}-\dfrac{1}{D^2}\right]\end{array}\right\}}, \tag{20}$$

$$C=V_{\mathrm{gs}}-\phi_{\mathrm{MS}}-V_{\mathrm{bi}}, \tag{21}$$

$$A=\frac{1}{\mathrm{J}_0(\alpha_n R)\mathrm{Y}_0(\alpha_n R_i)-\mathrm{J}_0(\alpha_n R_i)\mathrm{Y}_0(\alpha_n R)}, \tag{22}$$

$$D=\frac{1}{\mathrm{J}_1(\alpha_n R)\mathrm{Y}_0(\alpha_n R_i)-\mathrm{J}_0(\alpha_n R_i)\mathrm{Y}_1(\alpha_n R)}. \tag{23}$$

By applying continuous boundary conditions (5) and (6) and orthogonal relationships (16) and (17), we can derive

$$c_n^{(1)}-b_n^{(2)}=\frac{\int_0^{R_i}\left(\phi_{\mathrm{MS}}^{(1)}-\phi_{\mathrm{MS}}^{(2)}\right)C_n^{(1)}(r,z=L_1)\varepsilon(r)r\,\mathrm{d}r}{\int_0^{R_i}\left[C_n^{(1)}(r,z=L_1)\right]^2\varepsilon(r)r\,\mathrm{d}r}=\left(\phi_{\mathrm{MS}}^{(1)}-\phi_{\mathrm{MS}}^{(2)}\right)F_n, \tag{24}$$

where

$$F_n = \frac{\left\{\varepsilon_{\rm si}\dfrac{R\mathrm{J}_1(\alpha_n R)}{\alpha_n} + \varepsilon_i \mathrm{J}_0(\alpha_n R)\, A\dfrac{1}{\alpha_n}\left\{\dfrac{2}{\pi\alpha_n} - R\dfrac{1}{D}\right\}\right\}}{\left\{\begin{array}{c}\dfrac{\varepsilon_{\rm si}R^2}{2}\left\{[\mathrm{J}_1(\alpha_n R)]^2 + [\mathrm{J}_0(\alpha_n R)]^2\right\} \\ +\varepsilon_i {\mathrm{J}_0}^2(\alpha_n R)\, A^2\left[\dfrac{2}{\pi^2 {\alpha_n}^2} - \dfrac{R^2}{2A^2} - \dfrac{R^2}{2D^2}\right]\end{array}\right\}}, \tag{25}$$

and

$$\alpha_n \operatorname{csch}(\alpha_n L_1) b_n^{(1)} = \alpha_n \coth(\alpha_n L_1) c_n^{(1)} + \alpha_n \coth[\alpha_n (L_2 - L_1)] b_n^{(2)} - \alpha_n \operatorname{csch}[\alpha_n (L_2 - L_1)] c_n^{(2)}. \tag{26}$$

Substituting Eqs. (18) and (19) into Eqs. (24) and (26), we can determine $b_n^{(2)}$ and $c_n^{(1)}$ as

$$b_n^{(2)} = \frac{\left\{\begin{array}{c}\alpha_n \operatorname{csch}\left[\alpha_n (L_2 - L_1)\right] c_n^{(2)} + \alpha_n \operatorname{csch}(\alpha_n L_1)\, b_n^{(1)} \\ -\alpha_n \coth(\alpha_n L_1)\left(\phi_{\rm MS}^{(1)} - \phi_{\rm MS}^{(2)}\right) F_n\end{array}\right\}}{\alpha_n \coth(\alpha_n L_1) + \alpha_n \coth\left[\alpha_n (L_2 - L_1)\right]}, \tag{27}$$

$$c_n^{(1)} = \left(\phi_{\rm MS}^{(1)} - \phi_{\rm MS}^{(2)}\right) F_n + b_n^{(2)}. \tag{28}$$

For $L > 1.5 \times \pi/\alpha_1$, series of $V_{\rm L}^{(j)}(r,z)$ and $V_{\rm R}^{(j)}(r,z)$ decay rapidly. Therefore, only the lowest order terms in the series need to be kept. Then the expressions for the electrostatic potential of the two regions under the subthreshold condition can be explicitly given as

$$\phi_1(r,z) = V_{\rm gs} - \phi_{\rm MS}^{(1)} + \frac{b_1^{(1)} \sinh\left[\alpha_1 (L_1 - z)\right] + c_1^{(1)} \sinh(\alpha_1 z)}{\sinh(\alpha_1 L_1)} \mathrm{J}_0(\alpha_1 r), \tag{29}$$

$$\phi_2(r,z) = V_{\rm gs} - \phi_{\rm MS}^{(2)} + \frac{b_1^{(2)} \sinh\left[\alpha_1 (L_2 - z)\right] + c_1^{(2)} \sinh\left[\alpha_1 (z - L_1)\right]}{\sinh\left[\alpha_1 (L_2 - L_1)\right]} \mathrm{J}_0(\alpha_1 r). \tag{30}$$

Once the analytical potential is obtained, the subthreshold current can be derived based on the current continuity equation[19]

$$\begin{aligned} I_{\rm ds} &= 2\pi\mu q n_i \frac{\displaystyle\int_0^{Vds} \mathrm{e}^{-qV(z)/kT}\,\mathrm{d}V(z)}{\displaystyle\int_0^L \frac{\mathrm{d}z}{\displaystyle\int_0^R \mathrm{e}^{q\phi(r,z)/kT} r\,\mathrm{d}r}} \\ &= 2\pi kT\mu n_i \frac{1 - \mathrm{e}^{-qV_{\rm ds}/kT}}{\displaystyle\int_0^L \frac{\mathrm{d}z}{\displaystyle\int_0^R \mathrm{e}^{q\phi(r,z)/kT} r\,\mathrm{d}r}}, \end{aligned} \tag{31}$$

where μ is the effective mobility, and n_i is the intrinsic carrier density. The subthreshold current can be calculated analytically as a function of $V_{\rm gs}$ and $V_{\rm ds}$ according to Eq. (31).

By applying the same method in Ref. [13], we can obtain the threshold voltage roll-off model

$$\Delta V_{\rm th} = \Delta V_{\rm th1} + \Delta V_{\rm th2} + \Delta V_{\rm th3}, \tag{32}$$

where

$$\Delta V_{\rm th1} = -2\sqrt{b_1^{(1)} c_1^{(1)}} \exp\left(-\frac{\alpha_1 L_1}{2}\right), \tag{33}$$

$$\Delta V_{\rm th2} = \frac{kT}{q} \ln\left\{\frac{\sqrt{\pi}}{2G_1 L_1}\left[\operatorname{erf}\left(G_1 (L_1 - z_c)\right) + \operatorname{erf}(G_1 z_c)\right]\right\}, \tag{34}$$

$$\Delta V_{\rm th3} = \frac{kT}{q} \ln\left\{\frac{G_1^2 R^2}{2\left(1 - \exp\left(-\frac{G_1^2 R^2}{2}\right)\right)}\right\}, \tag{35}$$

$$G_1 = \left(\frac{q\alpha_1^2 \sqrt{b_1^{(1)} c_1^{(1)}} \exp(-\alpha_1 L_1/2)}{kT}\right)^{1/2}, \tag{36}$$

$$\operatorname{erf}(z) = \frac{2}{\sqrt{\pi}} \int_0^z \exp\left(-u^2\right) \mathrm{d}u, \tag{37}$$

and the subthreshold slope degradation model

$$\begin{aligned} S &= \left[\frac{\partial\left(\log_{10} I_{\rm ds}\right)}{\partial V_{\rm gs}}\right]^{-1} \\ &\simeq \left(\frac{\partial\phi_{\rm min}}{\partial V_{\rm gs}}\right)^{-1} \times 60\ \mathrm{mV/Dec}, \end{aligned} \tag{38}$$

where

$$\frac{\partial \phi_{\min}}{\partial V_{\rm gs}} = 1 - 2E_1 \frac{\left(V_{\rm bi} + \phi_{\rm MS}^{(1)} + V_{\rm ds}/2 - V_{\rm gs}\right) \exp\left(-\alpha_1 L_1/2\right)}{\sqrt{\left(V_{\rm bi} + \phi_{\rm MS}^{(1)} - V_{\rm gs}\right)\left(V_{\rm ds} + V_{\rm bi} + \phi_{\rm MS}^{(1)} - V_{\rm gs}\right)}}. \tag{39}$$

3. Results and discussion

Using the derived analytical models, we examine the performance of the HDMSG in terms of surface electrostatics potential, subthreshold current, threshold voltage roll-off, DIBL, and subthreshold swing. To consider the influence of the FIBL, the simulated data of higher gate dielectric constants are also included for comparison. To verify the analytical model, the ISE 3D device simulator is employed to simulate the device characteristics. Unless otherwise stated, the drain and source doping concentration is $N_{\rm d} = 5 \times 10^{19}$ cm^{-3}, the silicon channel is undoped, and the work functions of M_1 and M_2 are 4.65 eV and 4.4 eV, respectively.

Figure 2 shows the 3D electrostatic potential distribution in the channel and the gate dielectric regions of the HDMSG. It can be observed that the electrostatic potential distribution in the gate dielectric region is non-uniform, which is caused by the influence of the FIBL. For this reason, the conventional analytical model[4–6] for the DMSG MOSFET, which needs to assume a uniform electrostatic potential distribution in the gate dielectric region, will be invalid when considering the effect of the FIBL.

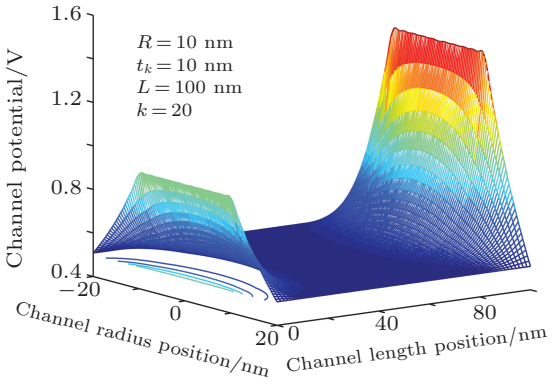


Fig. 2. (colour online) 3D electrostatic potential distribution in the channel of the HDMSG.

The surface electrostatic potential distribution of the HDMSG along the channel is plotted in Fig. 3. The simulation results (dotted line) of the conventional analytical model for the DMSG MOSFET are also included for comparison. For a given effective oxide thickness of 1.5 nm, the physical thickness of the gate dielectric will be 19.23 nm with a dielectric constant of 50, which will result in a serious FIBL effect. Therefore, ignoring the influence of the FIBL on the surface potential will lead to large errors.

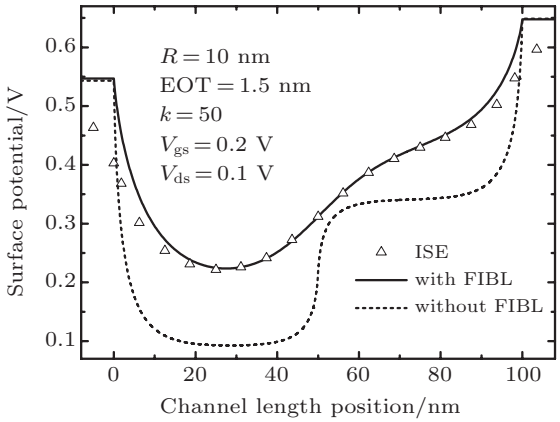


Fig. 3. Surface electrostatic potential distribution of HDMSG along the channel.

To gain an insight into the physical mechanism responsible for the influence of the FIBL on the HDMSG, Fig. 4 shows the surface potential profile for the HDMSG with different gate dielectric constants and drain biases. It can be seen from the figure that for a smaller κ value (inset, $\kappa = 3.9$), the step-like surface potential distribution can effectively screen the channel region near the source from the drain voltage. Whereas given $\kappa = 50$, as the drain bias increases, the position of the minimum surface potential for the HDMSG shifts toward the source, while the minimum channel potential pulls up, leading to bad immunity of the DIBL.

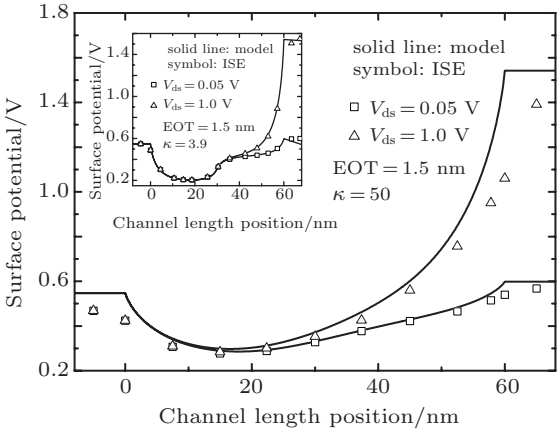


Fig. 4. Surface potential profile for the HDMSG with different κ and $V_{\rm ds}$.

The $I_{\rm ds}$–$V_{\rm gs}$ curves calculated from Eq. (34) are compared with the 3D numerical simulation results in

Fig. 5. It is demonstrated that the results obtained from the analytical solution agree well with the simulated results obtained using the ISE in the subthreshold region. Figure 5 also shows the dependence of the subthreshold current on the gate bias with gate dielectric constant κ as a parameter. It can be observed that a higher gate dielectric constant suffers more serious FIBL, therefore it leads to a larger subthreshold current.

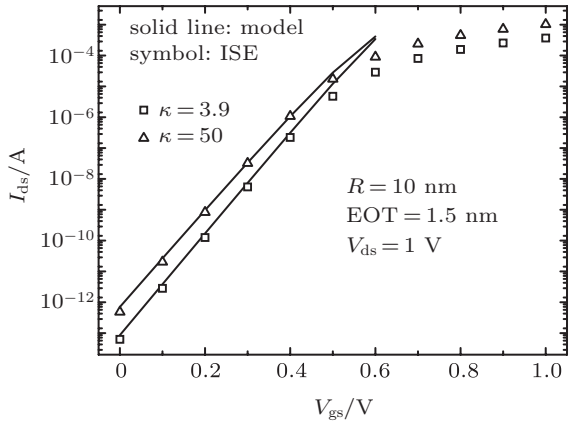


Fig. 5. Subthreshold current of HDMSG with various κ values.

The threshold voltage roll-off versus the gate length is plotted in Fig. 6 for different gate dielectric constants. It reveals that for the same EOT, the higher-κ gate dielectric will be subjected to more serious FIBL than the lower-κ gate dielectric does. Therefore, a significant reduction of the channel barrier for $\kappa = 50$ will induce great threshold voltage roll-off when the channel length is decreased further.[20]

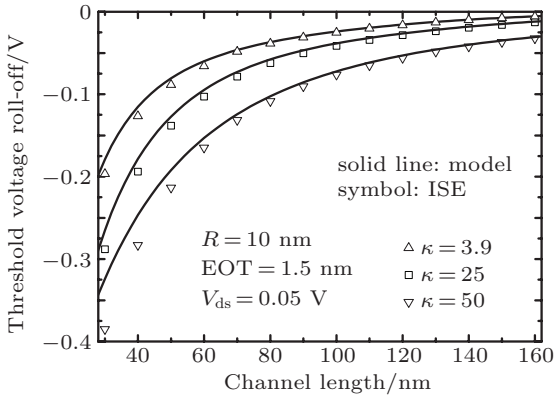


Fig. 6. Threshold voltage roll-off versus gate length for different κ values.

DIBL and subthreshold swing variations of various gate dielectric constant κ with the gate length are presented in Figs. 7 and 8, respectively. The DIBL is defined as $\Delta V_{\rm th}/\Delta V_{\rm ds}$, where $\Delta V_{\rm th} = V_{\rm th}|_{V_{\rm ds}=0} - V_{\rm th}|_{V_{\rm ds}=2}$. It is indicated that with the same EOT, a higher gate dielectric constant will induce a greater DIBL and subthreshold swing.

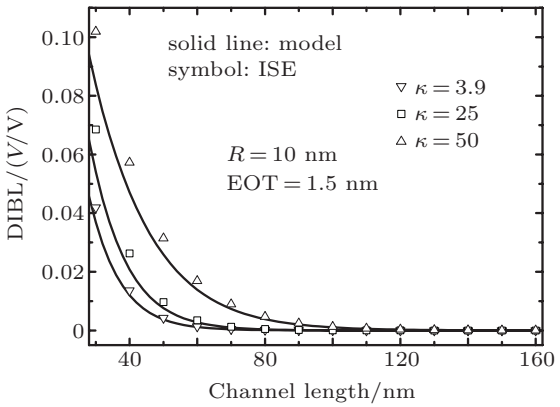


Fig. 7. DIBL versus channel length with various κ values.

From Figs. 4–8, it can be seen that in order to suppress the SCEs (such as threshold voltage roll-off, DIBL, and subthreshold swing), low-κ gate dielectrics are preferred. Even though a smaller dielectric constant of gate insulator is required to reduce threshold voltage roll-off, the DIBL, and the subthreshold swing caused by the FIBL, the lower-κ gate dielectric will possibly induce a large gate leakage current due to its weak gate insulation, especially in the nanoscale device regime. The trade-off between alleviating the short-channel performance degradation using lower-κ gate dielectric and decreasing the gate leakage current using a higher-κ gate dielectric should be considered when optimizing the DMSG MOSFET design.

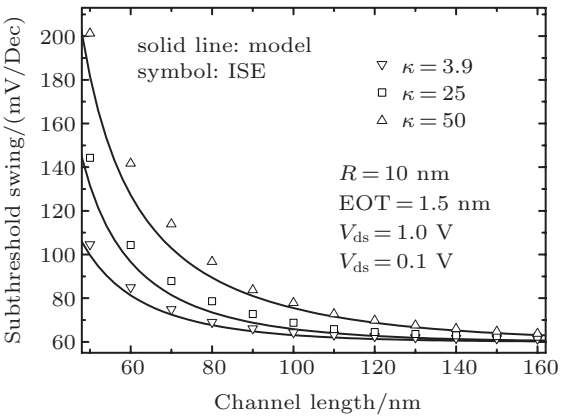


Fig. 8. Subthreshold swing versus channel length with various κ.

4. Conclusion

On the basis of a fully 2D solution of the potential in both the silicon and the gate insulator, a new physical and analytical model for the HDMSG has been presented incorporating the FIBL effect. The influence of the FIBL on the device performance is

thoroughly examined in terms of subthreshold current, threshold voltage roll-off, DIBL, and subthreshold swing. It is found that for the same equivalent oxide thickness, the gate insulator with a high-κ dielectric constant will degrade the short-channel performance of the HDMSG. The results obtained from the model agree well with the simulated results from the ISE. This paper not only provides analytical models for the HDMSG, but also a physical insight into the mechanism of the HDMSG.

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