Analysis of the breakdown mechanism for an ultra high voltage high-side thin layer silicon-on-insulator p-channel lateral double-diffused metal–oxide semiconductor*

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This paper discusses the breakdown mechanism and proposes a new simulation and test method of breakdown voltage (BV) for an ultra-high-voltage (UHV) high-side thin layer silicon-on-insulator (SOI) p-channel lateral double-diffused metal–oxide semiconductor (LDMOS). Compared with the conventional simulation method, the new one is more accordant with the actual conditions of a device that can be used in the high voltage circuit. The BV of the SOI p-channel LDMOS can be properly represented and the effect of reduced bulk field can be revealed by employing the new simulation method. Simulation results show that the off-state (on-state) BV of the SOI p-channel LDMOS can reach 741 (620) V in the 3-μm-thick buried oxide layer, 50-μm-length drift region, and at −400 V back-gate voltage, enabling the device to be used in a 400 V UHV integrated circuit.

Keywords: silicon on insulator, breakdown voltage, back-gate voltage, p-channel lateral double-diffused metal–oxide semiconductor

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1. Introduction

For many high voltage integrated circuit (IC) applications, e.g., in power conversion, automotive and medical uses, silicon on insulator (SOI) technology has obvious advantages over the commonly used junction isolation technology, such as high speed, low power dissipation, perfect radiation hardness, and superior isolation.[1−6] Thin layer SOI technology provides obvious merits over thick layer SOI technology, since it has better process compatibility, higher packing density, and lower parasitic effect.[7−9] Consequently, thin layer SOI technology has become very promising for power IC applications. The thin layer SOI thick gate oxide p-channel lateral double-diffused metal–oxide semiconductor (LDMOS) is commonly used in high voltage circuits, such as lever-shift circuits, driver circuits, and output stage circuits.[8,10] It is important to confirm the simulation and test method of breakdown voltage (BV). To ensure the lowest back-gate voltage, it is conventional to connect the drain electrode and the back-gate electrode to a negative high voltage which scans during the simulation. Additionally, the gate and source electrodes are grounded.[8,10,11] However, this conventional simulation method does not reflect the actual situations of the device used in the high voltage circuit. When the fixed high voltage is applied to the back-gate electrode, the effect of the back-gate on the breakdown performance of SOI transistors has been discussed in recent years.[12−18] However, the impact of the back-gate on the breakdown behaviour of power devices has been discussed only for n-channel LDMOS. The back-gate effect on breakdown behaviour of SOI p-channel LDMOS is seldom studied.

In this paper, we propose a new simulation and test method of BV and discuss the impact of the back-gate bias on an ultra-high-voltage (UHV) high-side thin layer SOI p-channel LDMOS. The breakdown mechanism is investigated by both two-dimensional (2D) process simulation with Tsuprem4 and device simulation with Medici. The BV of the SOI p-channel LDMOS can be properly reflected and the effect of reduced bulk field (REBULF) is revealed by employing

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the new simulation method.

2. Proposed simulation condition

The schematic cross-sectional view of a UHV high-side thin layer SOI p-channel LDMOS is shown in Fig. 1. The gate oxide layer of the p-channel LDMOS is as thick as the field oxide layer because the p-channel LDMOS gate is driven by a high voltage level. Double reduced surface field technology is used for the device, where an additional layer of opposite conductivity (p-drift layer) is incorporated inside an extended n-drift region. Both the n-drift region and the p-drift region have employed the variation of lateral doping technique, which uses a layer of oxide with a series of small slit openings to mask the impurity implantation. The n-drift region of the device is doped with a charge profile, which decreases monotonically from the source towards the drain of the device. The p-drift region is doped oppositely, which increases from the source to the drain. This optimizes the lateral electric field, and thus a high BV of p-channel LDMOS is obtained. The buried oxide thickness ($t_{\rm I}$) is 3 μm, the thickness of top silicon layer ($t_{\rm s}$) is 1.5 μm, and the length of drift region ($L_{\rm d}$) is 50 μm. In Fig. 1, $V_{\rm D}$, $V_{\rm S}$, $V_{\rm G}$, and $V_{\rm BG}$ are the voltages applied to the drain, source, gate, and back-gate electrodes, respectively. $V_{\rm DD}$ represents the power supply voltage and the negative high voltage ($V_{\rm nh}$) is a variable which is scanned during simulation. X and Y axes are shown in Fig. 1.

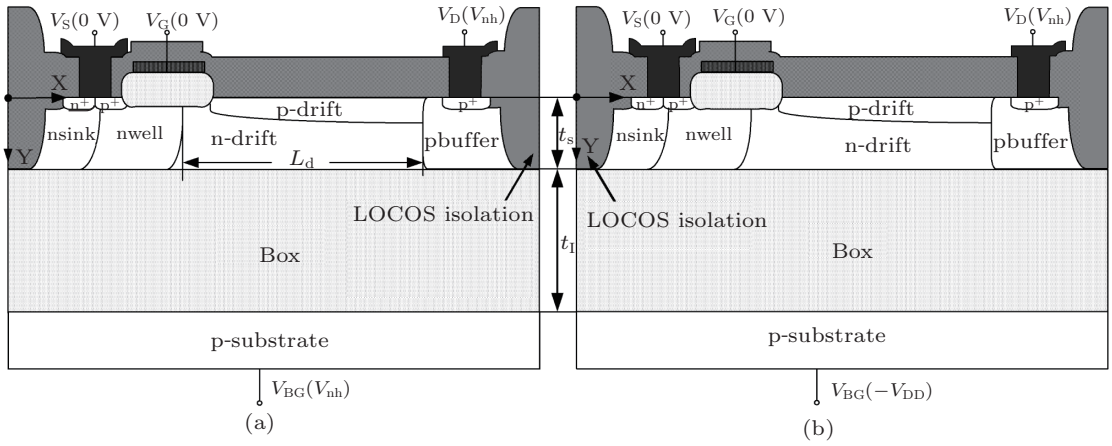


Fig. 1. Schematic cross-sectional view of thin layer SOI p-channel LDMOS structure. (a) The conventional simulation conditions ($V_{\rm G} = V_{\rm S} = 0$ V, $V_{\rm D} = V_{\rm BG} = V_{\rm nh}$), (b) the proposed simulation conditions ($V_{\rm G} = V_{\rm S} = 0$ V, $V_{\rm BG} = -V_{\rm DD}$, $V_{\rm D} = V_{\rm nh}$).

High-side SOI p-channel LDMOS is widely used in high voltage circuit. The applied voltage conditions in the actual operation are as follows: $V_{\rm DD}$ is applied to $V_{\rm S}$, $V_{\rm G}$ and $V_{\rm D}$ shift from 0 V to a high voltage, and $V_{\rm BG}$ is grounded. Although the applied voltage to $V_{\rm BG}$ is fixed at 0 V and $V_{\rm S}$ is connected to $V_{\rm DD}$ in the actual situation, to simplify the analysis, the applied voltage conditions in the simulation are as follows. Figure 1(a) shows the conventional simulation conditions in which $V_{\rm BG}$ is tied together with $V_{\rm D}$ connected to $V_{\rm nh}$, and $V_{\rm G}$ and $V_{\rm S}$ are connected to 0 V. With the conventional simulation and test method, the potential difference between $V_{\rm S}$ and $V_{\rm BG}$ is always changing. Therefore, this conventional simulation condition does not reflect the practical applications of the device used in high voltage circuits. A new simulation method of BV for SOI p-channel LDMOS is proposed. $V_{\rm G}$ and $V_{\rm S}$ are still grounded, $V_{\rm BG}$ is connected to $-V_{\rm DD}$, and $V_{\rm D}$ is connected to $V_{\rm nh}$. The potential difference between $V_{\rm S}$ and $V_{\rm BG}$ is still $V_{\rm DD}$ and this new simulation method is more accordant with the actual conditions of the device than the conventional one. The proposed simulation conditions of the BV for the SOI p-channel LDMOS can be commonly applied in the high voltage circuit. The following discussion will take high voltage of 400 V as an illustration by 2D device simulation with Medici.

3. Results and discussion

Figure 2 shows equipotential contours of two simulation conditions for the SOI p-channel LDMOS at breakdown under $V_{\rm DD}$ of 400 V. With the conventional simulation method, equipotential lines will be distributed under the source side. The vertical blocking voltage is only supported by the drift region and

the buried oxide layer (Fig. 2(a)). The BV is only 475 V and the breakdown of the device occurs at the interface of the buried oxide layer at source side. Figure 2(b) gives the equipotential contours at breakdown with the proposed simulation method. The BV reaches 685 V and the breakdown point transfers to the drain side. If −400 V is applied to V_{BG}, the partial vertical blocking voltage will be transferred and supported by the depletion layers between V_D and V_{BG}, more equipotential lines will be distributed under the drain side. Because of the negative back-gate bias, the vertical blocking voltage is not only supported by the drift layers under the source side but also by the depletion layers between V_D and V_{BG}. Therefore, for the same bias of V_D, the bulk electric field in silicon is reduced at the source side and enhanced at the drain side, and then the BV of the SOI p-channel LDMOS will increase.

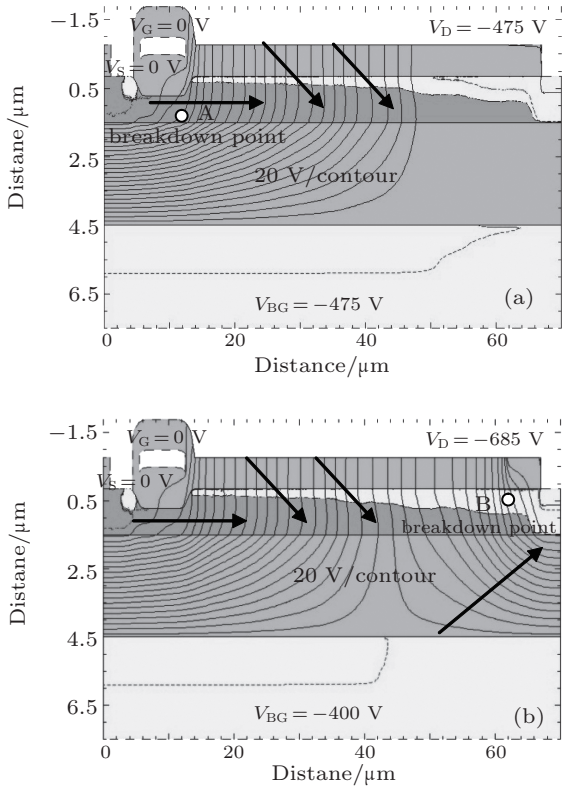


Fig. 2. Equipotential contours at breakdown (the implantation doses of nwell region, n-drift and p-drift layers are respectively $Q_{nwell} = 5 \times 10^{12}$ cm^{-2}, $Q_{p-drift} = 1 \times 10^{12}$ cm^{-2}, $Q_{n-drift} = 5 \times 10^{12}$ cm^{-2}). (a) The conventional simulation conditions ($V_G = V_S = 0$ V, $V_D = V_{BG} = -475$ V), (b) the proposed simulation conditions ($V_G = V_S = 0$ V, $V_{BG} = -400$ V, $V_D = -685$ V).

Figure 3 gives the lateral and vertical electric field distributions of the two simulation methods of BV for the SOI p-channel LDMOS. With the conventional simulation method, the lateral electric field distribution is mainly located on the source side and the lateral electric field on the drain side is extremely low. The bulk electric field on the source side reaches 3.5×10^5 V/cm, which is beyond the silicon critical electric field of about 3×10^5 V/cm. With the proposed simulation method, bulk electric field in silicon will be modulated, the lateral electric field on the source side will be reduced and the lateral electric field on the drain side will be enhanced markedly, as shown in Fig. 3(a). Now the electric field on the source side is far below the critical electric field and a much higher

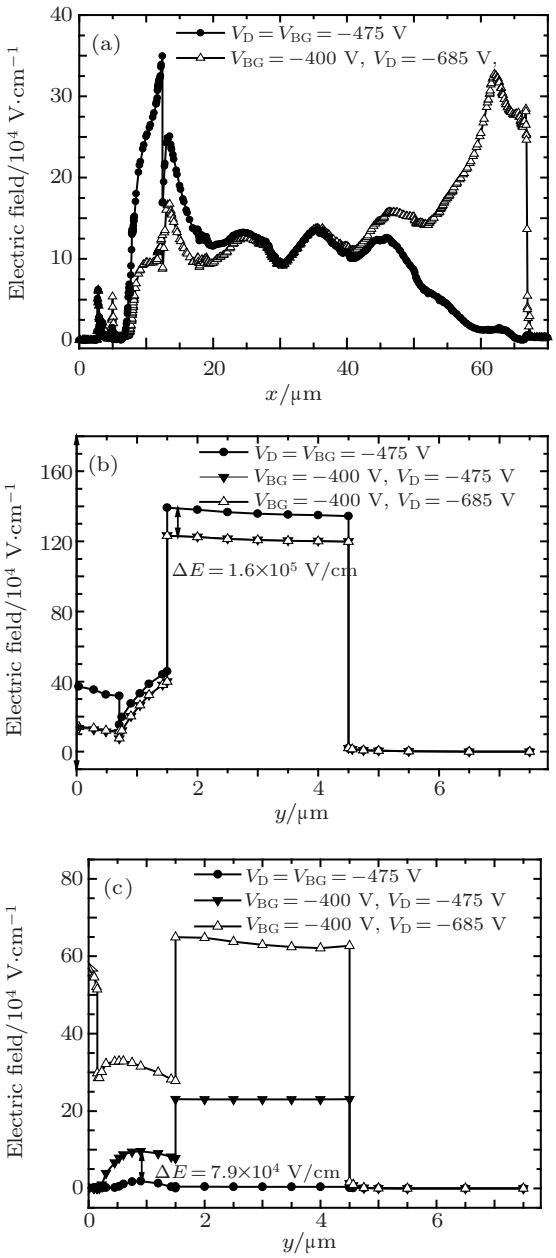


Fig. 3. Lateral and vertical electric field distributions (ΔE represents the electric field difference). (a) Lateral bulk electric field ($y = 0.7$ μm), (b) vertical electric field ($x = 12$ μm), (c) vertical electric field ($x = 62$ μm).

voltage can be applied before the breakdown occurs. The bulk electric field on the source side is reduced to 1.6×10^5 V/cm and the bulk electric field on the drain side increases to 3.2×10^5 V/cm, which exceeds the silicon critical electric field. When $V_{\rm nh}$ is applied to $V_{\rm D}$ and $V_{\rm BG}$ is connected to -400 V, the maximum electric field of the source side is reduced from 13.9×10^5 V/cm to 12.3×10^5 V/cm and the maximum bulk electric field of the drain side in silicon increases from 1.7×10^4 V/cm to 9.6×10^4 V/cm with a negative back-gate bias at the same bias of $V_{\rm D}$. The bulk electric field on the drain side is reduced, but the bulk electric field on the source side is enhanced. The BV of SOI p-channel LDMOS increases owing to the modulation of the active region electric field distributions induced by the back-gate voltage.

Figure 4 gives the bulk lateral and vertical electric field distributions on the source side for the SOI p-channel LDMOS with different back-gate biases. With the increase of $|V_{\rm BG}|$, the n-drift region will deplete gradually, the electric field on the source side is enhanced and a new electric field peak appears at the source side. If -400 V is applied to $V_{\rm BG}$, the electric field on the source side reaches 2.5×10^5 V/cm. Due to the impact of the back-gate, the bulk electric field is modulated and more equipotential lines will be distributed on the source side. With the increase of the bulk electric field in silicon on the source side, the electric field in the buried oxide layer is enhanced. When $V_{\rm BG}$ is connected to -400 V, the maximum buried oxide layer electric field on the source side increases to 11.9×10^5 V/cm.

Figure 5 shows the simulated BV as a function of $Q_{\rm p\text{-}drift}$ with different simulation methods. With the conventional simulation method, the BV of the p-channel LDMOS will decrease with the increase of $Q_{\rm p\text{-}drift}$. As the same potential is applied to $V_{\rm BG}$ and $V_{\rm D}$, the vertical blocking voltage is only supported by the depletion layers between $V_{\rm S}$ and $V_{\rm BG}$. The n-drift and p-drift regions will be depleted by each other, the p-drift region will be fully depleted at a suitable $Q_{\rm p\text{-}drift}$, and the blocking voltage will be improved. The maximum BV reaches 475 V when $Q_{\rm p\text{-}drift}$ is 1×10^{12} cm^{-2} and the minimum BV is 190V when $Q_{\rm p\text{-}drift}$ is 4×10^{12} cm^{-2}. With the proposed simulation method, the blocking voltage will be influenced by the field-modulated effect of the charges in the interface induced by the back-gate. As the vertical blocking voltage is not only supported by the drift layers under the source side but also by the depletion layers between $V_{\rm D}$ and $V_{\rm BG}$, the maximum blocking voltage reaches 741 V at $Q_{\rm p\text{-}drift} = 2\times10^{12}$ cm^{-2}. However, the BV is reduced to 120 V when $Q_{\rm p\text{-}drift}$ is 4×10^{12} cm^{-2}. The blocking voltage will decrease when the $Q_{\rm p\text{-}drift}$ takes values of 2.5×10^{12} cm^{-2}, 3×10^{12} cm^{-2}, 3.5×10^{12} cm^{-2}, and 4×10^{12} cm^{-2}.

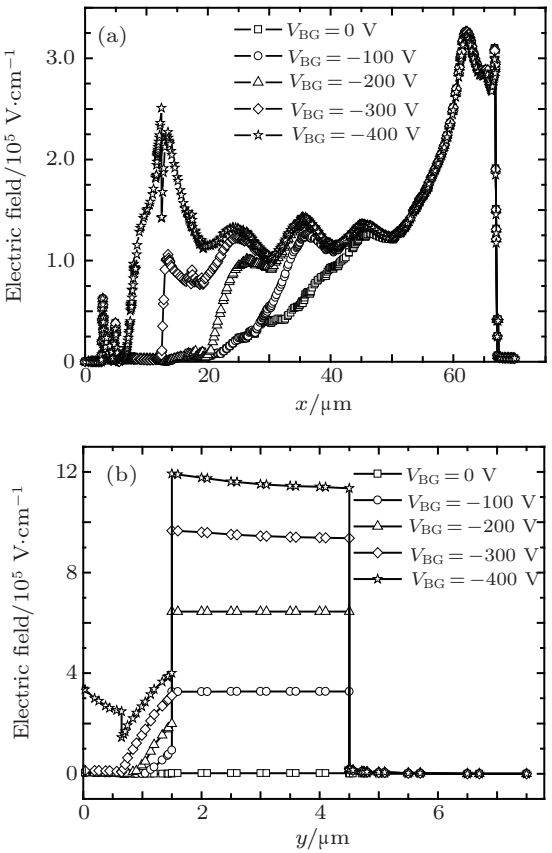


Fig. 4. (a) Bulk lateral electric field distribution (x = 0.7 μm). (b) Vertical electric field distribution (y = 12 μm).

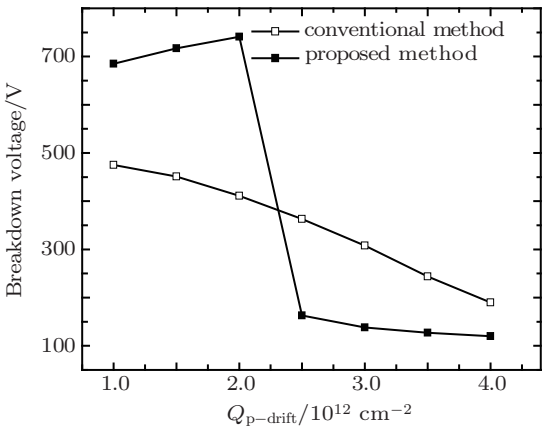


Fig. 5. Breakdown voltage versus $Q_{\rm p-drift}$ with different simulation methods ($Q_{\rm nwell} = 5\times10^{12}$ cm^{-2}, $Q_{\rm n-drift} = 5\times10^{12}$ cm^{-2}).

Figure 6 shows the equipotential distribution obtained by two simulation methods for SOI p-channel

LDMOS at breakdown when $Q_{\text{nwell}} = 5 \times 10^{12}$ cm^{-2}, $Q_{\text{n-drift}} = 5 \times 10^{12}$ cm^{-2}, and $Q_{\text{p-drift}} = 2.5 \times 10^{12}$ cm^{-2}. With the conventional simulation method, the n-drift and p-drift regions will be depleted by each other and the equipotential lines will be distributed under the source side. However, with the proposed simulation method, the BV will be reduced from 363 V to 163 V. When V_{BG} is connected to −400 V, the n-drift and p-drift regions are depleted partially and the hole inversion layer appears at the back-channel. After V_{nh} is applied to V_{D}, the n-drift region is fully depleted and the p-drift region is not fully depleted at a high $Q_{\text{p-drift}}$, the breakdown will occur early at the same implantation dose of the p-drift region. Therefore, it is mandatory for the device engineer to know the impact of the back-gate in order to optimize the dose of the drift region.

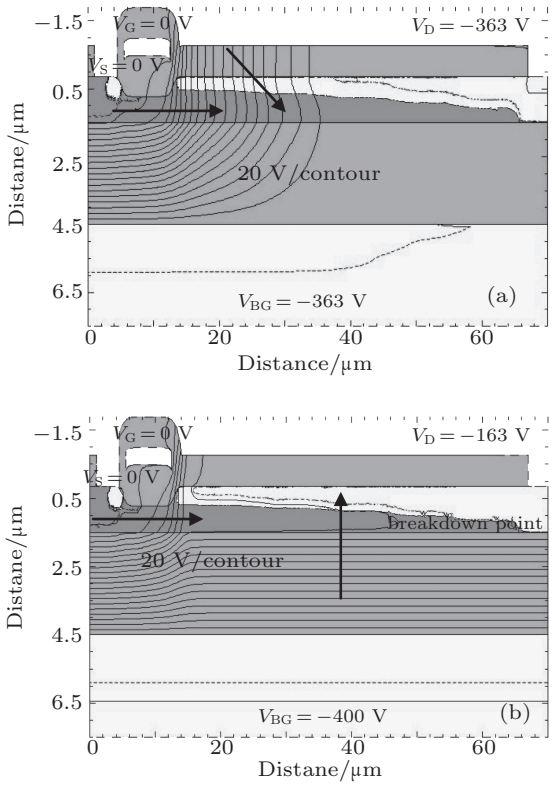


Fig. 6. Equipotential contours at breakdown ($Q_{\text{nwell}} = 5 \times 10^{12}$ cm^{-2}, $Q_{\text{p-drift}} = 2.5 \times 10^{12}$ cm^{-2}, $Q_{\text{n-drift}} = 5 \times 10^{12}$ cm^{-2}). (a) The conventional simulation conditions ($V_{\text{G}} = V_{\text{S}} = 0$ V, $V_{\text{BG}} = V_{\text{D}} = -363$ V). (b) The proposed simulation conditions ($V_{\text{G}} = V_{\text{S}} = 0$ V, $V_{\text{BG}} = -400$ V, $V_{\text{D}} = -163$ V).

Figure 7 shows the simulated BV as a function of $Q_{\text{n-drift}}$ obtained with different simulation methods. With the conventional simulation method, the BV of the SOI p-channel LDMOS will increase with the increase of $Q_{\text{n-drift}}$. As the same potential is applied to V_{BG} and V_{D}, the vertical blocking voltage is only supported by the depletion layers between the V_{S} and V_{BG}. The n-drift and p-drift regions will be depleted by each other, the p-drift region will be depleted gradually with the increase of $Q_{\text{n-drift}}$, and the blocking voltage will be improved. The maximum BV can reach 502 V when $Q_{\text{n−drift}}$ is 7×10^{12} cm^{-2}. The minimum BV is 251 V when $Q_{\text{p−drift}}$ is 3×10^{12} cm^{-2}. With the proposed simulation method, the BV will increase due to the field-modulated effect induced by the back-gate when $Q_{\text{n−drift}}$ takes a value of 5×10^{12} cm^{-2}, 6×10^{12} cm^{-2}, and 7×10^{12} cm^{-2}. However, the breakdown will decrease when $Q_{\text{n−drift}}$ takes values of 3×10^{12} cm^{-2}, 4×10^{12} cm^{-2}. When V_{BG} is connected to −400 V, the n-drift and p-drift regions are depleted partially and the hole inversion layer appears at the back-channel. After V_{nh} is applied to V_{D}, the n-drift region is fully depleted and then the p-drift region is not fully depleted at a low $Q_{\text{n−drift}}$ and the breakdown will occur early at the same implantation dose of the n-drift region.

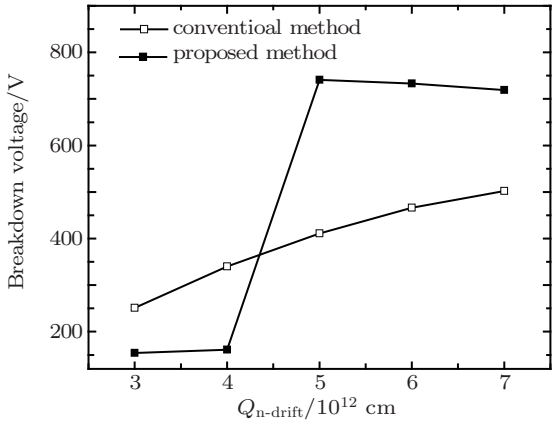


Fig. 7. Breakdown voltage versus $Q_{\text{n-drift}}$ with different simulation conditions ($Q_{\text{nwell}} = 5 \times 10^{12}$ cm^{-2}, $Q_{\text{p−drift}} = 2 \times 10^{12}$ cm^{-2})

Figure 8 shows the simulated BV as a function of V_{BG} obtained with different doses in the p-drift layer. The BV will increase with $|V_{\text{BG}}|$ when $Q_{\text{p-drift}}$ take values of 1×10^{12} cm^{-2}, 1.5×10^{12} cm^{-2}, and 2×10^{12} cm^{-2}. When V_{BG} equals −400 V, the maximum blocking voltage is 741 V at $Q_{\text{p-drift}} = 2 \times 10^{12}$ cm^{-2}. The BV is reduced to 685 V at $Q_{\text{p-drift}} = 1 \times 10^{12}$ cm^{-2} owing to the decrease of $Q_{\text{p-drift}}$. The BV first increases and then decreases with increasing $|V_{\text{BG}}|$ when $Q_{\text{p-drift}}$ takes 3×10^{12} cm^{-2}, 4×10^{12} cm^{-2}. BV will be reduced to 138 V at $Q_{\text{p-drift}} = 3 \times 10^{12}$ cm^{-2} when V_{BG} is −400 V. While the BV will begin to decrease at $Q_{\text{p-drift}} = 4 \times 10^{12}$ cm^{-2} when V_{BG} is −200 V. This

is because the breakdown of the device occurs early at a high $Q_{\text{p-drift}}$. The BV is reduced to 163 V at $Q_{\text{p-drift}} = 4 \times 10^{12}$ cm^{-2} when $V_{\text{BG}} = -200$ V.

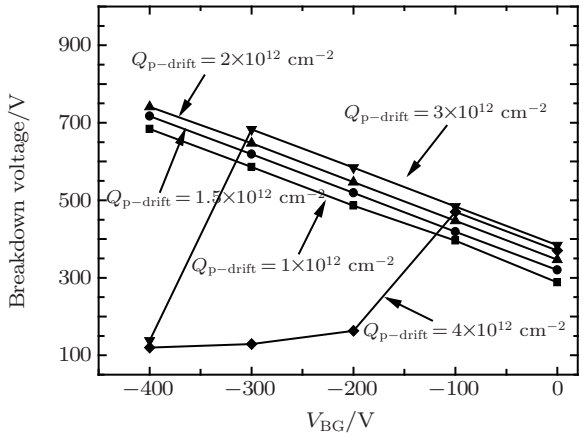


Fig. 8. Breakdown voltage versus back-gate bias with different values of $Q_{\text{p-drift}}$ ($Q_{\text{nwell}} = 5 \times 10^{12}$ cm^{-2}, $Q_{\text{n-drift}} = 5 \times 10^{12}$ cm^{-2})

Figure 9 gives the simulated output characteristics when V_{BG} is connected to -400 V. When $Q_{\text{nwell}} = 5\times10^{12}$ cm^{-2}, $Q_{\text{n-drift}} = 5\times10^{12}$ cm^{-2}, and $Q_{\text{p-drift}} = 2\times10^{12}$ cm^{-2}, with increasing $|V_{\text{GS}}|$, the on-resistance (R_{on}) will decrease and the drain-source saturation current ($I_{\text{DS,SAT}}$) will increase. When $V_{\text{GS}} = -400$ V, $I_{\text{DS,SAT}}$ reaches 105 μA/μm, the off-state BV reaches 741 V and the on-state BV reaches 620 V.

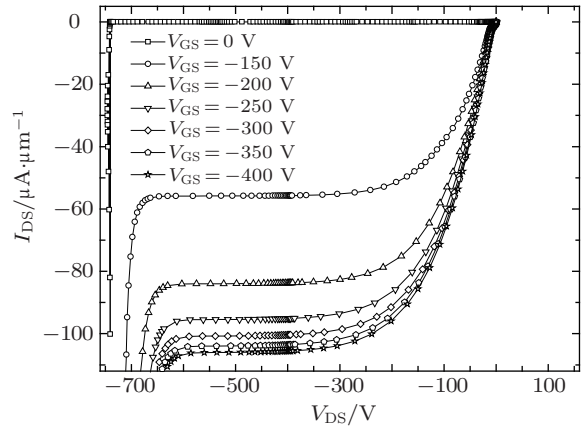


Fig. 9. I_{DS}–V_{DS} characteristic of p-channel LDMOS ($Q_{\text{nwell}} = 5 \times 10^{12}$ cm^{-2}, $Q_{\text{n-drift}} = 5 \times 10^{12}$ cm^{-2}, $Q_{\text{p-drift}} = 2 \times 10^{12}$ cm^{-2}).

4. Conclusion

In this paper, we propose a new simulation and test method of BV and analyse the breakdown mechanism for a UHV high-side thin layer SOI p-channel LDMOS. The proposed simulation conditions of the off-state BV are that V_{G} and V_{S} are still grounded, V_{BG} is connected to $-V_{\text{DD}}$, and V_{D} is connected to V_{nh}. This simulation method is more accordant with the actual conditions of the devices used in the high voltage circuit than the conventional one, and the effect of REBULF is revealed. The off-state and on-state simulated BVs of the SOI p-channel LDMOS reach 741 V and 620 V, respectively, at 3 μm-thick buried oxide layer, 50-μm-length drift region and -400 V back-gate voltage, enabling the device to be used in a 400 V UHV IC.

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