Temperature-dependent characteristics of 4H–SiC junction barrier Schottky diodes*

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The current–voltage characteristics of 4H–SiC junction barrier Schottky (JBS) diodes terminated by an offset field plate have been measured in the temperature range of 25–300 °C. An experimental barrier height value of about 0.5 eV is obtained for the Ti/4H–SiC JBS diodes at room temperature. A decrease in the experimental barrier height and an increase in the ideality factor with decreasing temperature are shown. Reverse recovery testing also shows the temperature dependence of the peak recovery current density and the reverse recovery time. Finally, a discussion of reducing the reverse recovery time is presented.

Keywords: 4H–SiC junction barrier Schottky diode, temperature dependence, electrical characteristics

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1. Introduction

Nowadays, almost all power electronic converter systems use Si-based power semiconductor switches. The performance of these switches is approaching the theoretical limit of the Si material. Another material with superior properties as compared with Si is silicon carbide (SiC), which is a promising candidate for use in the next generation of power devices, especially for high-voltage or high-temperature applications. Several papers have compared the Si-based with SiC-based power electronic devices and given the relative merits of wide band gap semiconductors, like SiC for high-voltage or high-temperature applications.[1−3] The 4H–SiC Schottky barrier diodes (SBDs) have been proved to have great potential in power applications because of their low conduction loss and fast switching speed.[4] One major issue of the SBD is its high reverse leakage current, especially at elevated temperatures. The junction barrier Schottky (JBS) diode is proposed for it offers Schottky-like on-state and fast switching characteristics, while the off-state characteristics have a low leakage current similar to that of the PiN diode.[5]

However, when temperature rises, the electrical parameters and the conduction mechanism of the metal-semiconductor (MS) interface change. To understand the influence of variation of temperature on the characteristics of 4H–SiC JBS diodes, temperature variation measurements were carried out. Furthermore, current–voltage (I–V) and reverse recovery characteristics are discussed in this paper. Moreover, the ideality factor, barrier height, series resistance, reverse recovery time, and peak reverse voltage were calculated and analysed.

2. Design and fabrication

An offset field plate (FP) is employed as the edge termination in this experiment, and its structure is shown in Fig. 1.

A 10 μm N^- epilayer with nitrogen doping of 1.56×10^{15} cm^{-3} was grown on the N^+ substrate produced by Cree and doped with nitrogen at a concentration higher than 1×10^{18} cm^{-3}. To form selective P-type regions in 4H–SiC, aluminum-ion (Al^+) or boron-ion (B^+) implantation is commonly employed. Aluminum is particularly attractive for implantation

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to form heavily doped P^+ regions with low sheet resistances, because Al acceptors have smaller ionisation energies (190 and 240 meV) than B acceptors (285 and 300 meV) in 4H– and 6H–SiC, respectively. Whereas the use of B is much more effective for implantation to form deep P–N junctions because of its lighter atom mass resulting in larger projected ranges.[6] In this work, Al^+ and B^+ were implanted with energy and dose being 150 eV/1.45×10^{14} cm^{-2}, and 400 eV/1.79×10^{15} cm^{-2}, respectively. Then the sample was annealed at 1650 °C for 45 min in argon ambience to activate the implanted ions. During annealing, a graphite crucible full of SiC powder was used to protect the surface of 4H–SiC, and avoid Si atoms escaping from surface at high annealing temperature.[7] A 500 nm SiO_2 layer was deposited on the surface as a passivation layer. A multi-layer consisting of Ti and Al was deposited in the P^+ regions, followed by a tri-layer metallization of Ti/Ni/Ag deposited on the backside, and subsequently annealed at 1000 °C in a gas mixture of 97% N_2 and 3% H_2 for 5 min. Finally, bi-layer metallization of Ti/Ag was used to form the front Schottky metal contact and FPs simultaneously.

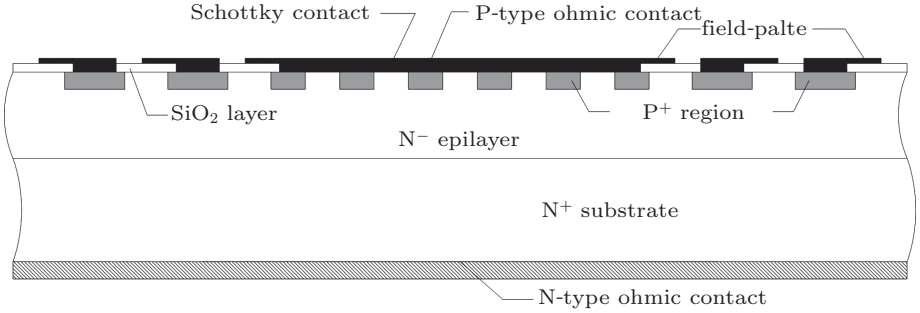


Fig. 1. Schematic cross section of a JBS diode with an offset FP as edge termination.

3. Results and discussion

3.1. DC characteristics

Temperature-dependent I–V characteristics of the devices were tested by using a Keithley 4200. Figure 2 shows the temperature-dependent forward I–V characteristics of a 6.25×10^{-4} cm^2 JBS diode. As can be seen in region I, the JBS current coincides with the Schottky diode due to the thermionic emission effect, which is characterised by a positive temperature coefficient (TC). In region II, the series resistance is dominated by the N-drift layer of the Schottky portion, so that a negative TC arises.[8,9] It is easy to see that when the voltage reaches 2 V, the current density is larger than 200 A/cm^2 at room temperature. With temperature increasing from 25 to 300 °C, the turn-on voltage of the JBS diode decreases from 0.81 to 0.63 V.

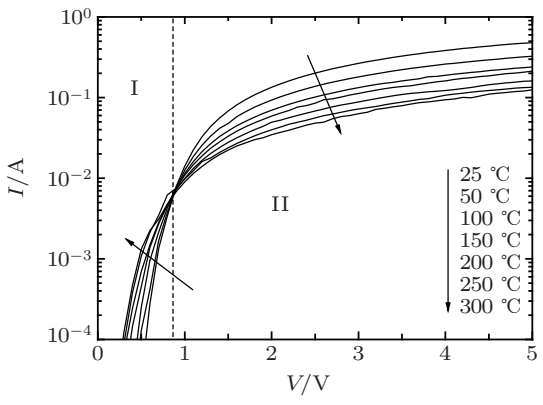


Fig. 2. Forward characteristics of the JBS diode in the temperature range of 25–300 °C.

The forward bias current passing through a uniform MS interface due to thermionic emission can be expressed as

$$I = I_{\rm S}\left[\exp\left(\frac{qV}{nkT}\right) - 1\right], \tag{1}$$

where $I_{\rm S}$ is the saturation current derived from the straight line intercept of $\ln I$ at $V = 0$ and is given by

$$I_{\rm S} = AA^*T^2\exp\left(-\frac{\phi_{\rm B}}{kT}\right), \tag{2}$$

where $\phi_{\rm B}$ is the zero bias apparent barrier height, k is the Boltzmann constant, T is the absolute temperature, V is the forward-bias voltage, A is the diode area, and A^* is the Richardson constant which is 146 A·cm^{-2}·K^{-2} for N-type 4H–SiC;[10] n in Eq. (1) is the ideality factor and can be used to find the deviation of the experimental I–V data from those of the

ideal thermionic model. At a low forward voltage, the ideality factor can be calculated as follows:

$$n = \frac{q}{kT}\frac{\partial V}{\partial \ln I}, \tag{3}$$

Equation (3) shows that in a suitable range of forward bias voltage, the slope of the forward waveform in logarithmic coordinates should be close to q/kT, therefore, n should have a value close to 1.

Since the inhomogeneity of Schottky barrier height in the actual area of electrode is hard to determine, the conventional activation energy method is employed to obtain $\phi_{\rm B}$. When V takes a suitable value, we can obtain the following equation from Eqs. (1) and (2):

$$I_{\rm F} = AA^*T^2 \exp\left(\frac{qV}{nkT} - \frac{\phi_{\rm B}}{kT}\right). \tag{4}$$

Take the logarithm of both sides of Eq. (4), we can obtain

$$\ln\left(\frac{I_{\rm F}}{T^2}\right) = \ln(AA^*) - \frac{1}{kT}\left(\phi_{\rm B} - \frac{qV}{n}\right), \tag{5}$$

where $\phi_{\rm B} - \frac{qV}{n}$ is the activation energy, and $I_{\rm F}$ is the forward current at certain forward bias V. Figure 3 shows the $\ln(I_{\rm S}/T^2)$ versus $1/T$ plot according to Eq. (5).

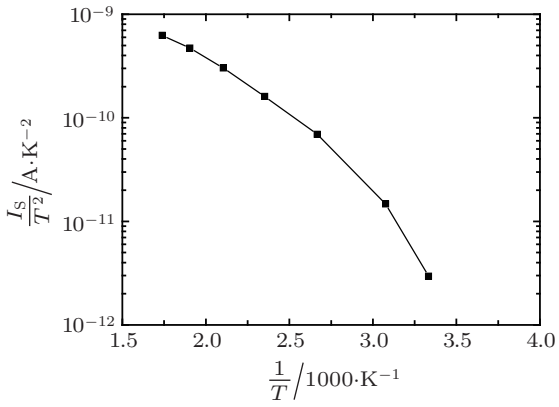


Fig. 3. Richardson plot of $\ln(I_{\rm S}/T^2)$ versus $1/T$ according to the activation energy method.

Figure 4(a) shows the n and $\phi_{\rm B}$ as a function of temperature extracted from I–V experimental data. As can be seen in this figure, the experimental value of n increases and $\phi_{\rm B}$ decreases with the decrease in temperature.

At a high forward voltage, the series resistance $R_{\rm D}$ can be given by

$$R_{\rm D} = \left(1 - \frac{\partial \ln I_{\rm F}}{\partial V}\frac{nkT}{q}\right) \Big/ \left(\frac{\partial I_{\rm F}}{\partial V}\right). \tag{6}$$

Figure 4(b) shows the series resistance extracted from Eq. (6). As can be seen in this figure that it increases significantly from 8.04 Ω at 25 °C to 33.83 Ω at 300 °C. The increased resistance is largely due to the increasing resistance in the 10-μm-thick drift layer caused by the decrease of electron mobility with elevated temperature.

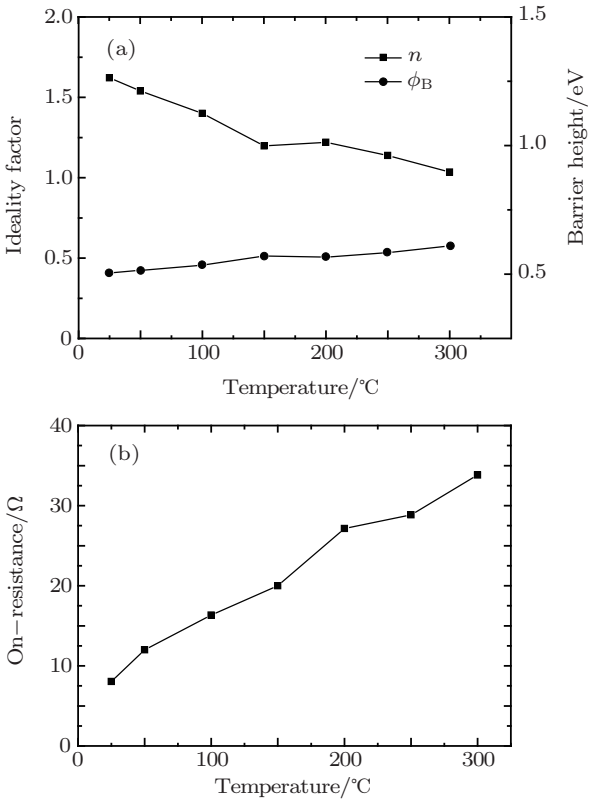


Fig. 4. Extracted results at different temperatures. (a) Temperature dependence of the ideality factor and barrier height. (b) Temperature dependence of series resistance.

The temperature-dependent reverse blocking characteristics of the JBS diode are shown in Fig. 5. In the temperature range of 50 °C–300 °C, the reverse current of

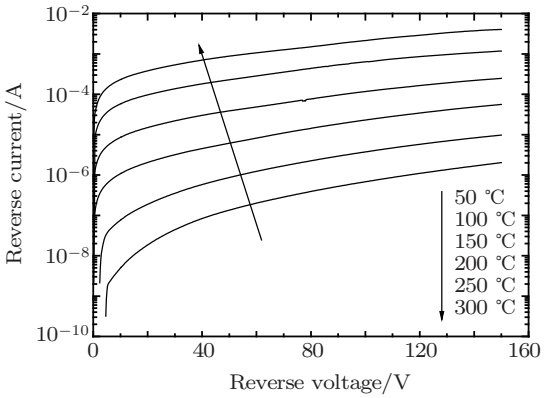


Fig. 5. Temperature-dependent reverse I–V characteristics of a JBS diode.

JBS diode grows from 1.9×10^{-6} to 4.1×10^{-3} A under 150 V reverse bias. Apparently, because at low voltage bias, the leakage current is dominated by thermionic emission, the reverse current increases with temperature. At high reverse bias, the leakage current is less sensitive to the temperature, which is mainly dominated by the tunneling current.[11]

3.2. Reverse recovery characteristics

The reverse–recovery test was performed using the setup shown in Fig. 6. The system includes a Cascade probe station with micromanipulators and microscope for probe positioning, two Agilent E3631A voltage sources supplying a forward voltage and a 50 V reverse voltage, a single-pole double-throw switch which switches forward state to reverse state within 20 ns, a Tektronix TPS2012 oscilloscope with a frequency limit $f_{\rm MAX}$ = 100 MHz to monitor and record the output waveforms, and a 100 Ω resistance R1 used to measure the current.

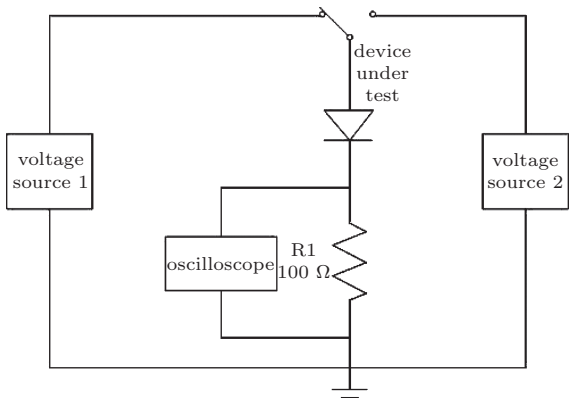


Fig. 6. Schematic of experimental setup for reverse–recovery measurements.

For the test, the chopper circuit was set up with device under test (DUT) in a temperature-controlled probe station. Under the test conditions, the JBS diode was switched from a 10 V forward bias to the blocking state with a reverse bias of 50 V within 20 ns as shown in Fig. 7. Table 1 shows the reverse recovery time $t_{\rm rr}$ and peak reverse current density $J_{\rm RM}$ at different temperatures extracted from Fig. 8. It can be seen that $t_{\rm rr}$ increases slightly from 44 to 52 ns, while $J_{\rm RM}$ increases from 87.2 to 162.3 A/cm^2 when the temperature rises, corroborating the bipolar conduction under these conditions.

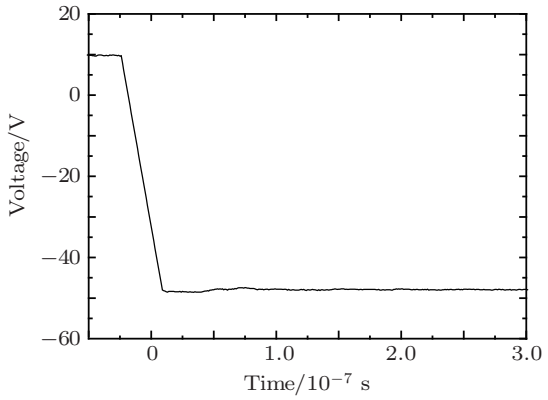


Fig. 7. Voltage waveform.

Table 1. The values of $t_{\rm rr}$ and $J_{\rm RM}$ at different temperatures.

Temperature/°C	$t_{\rm rr}$/ns	$J_{\rm RM}$/A·cm^2
25	44	87.2
50	44	91.9
100	46	102.5
150	47	111.4
200	47	116.8
250	51	140.9
300	52	162.3

The fast switching behaviour of JBS diodes with Al and B implanted in P^+ regions as in this work can be related to the presence of lifetime-killing defects (recombination centers) in the vicinity of P–N junction compared with Refs. [12]–[14]. The influence of boron on minority carrier lifetime in N-type 4H–SiC CVD-grown epilayers was studied by Storasta *et al.*[15] Although the recombination mechanism was not understood, the clear correlation between the background boron concentration (in the range from 6×10^{12} to 4×10^{13} cm^{-3}) and reduction of the minority carrier

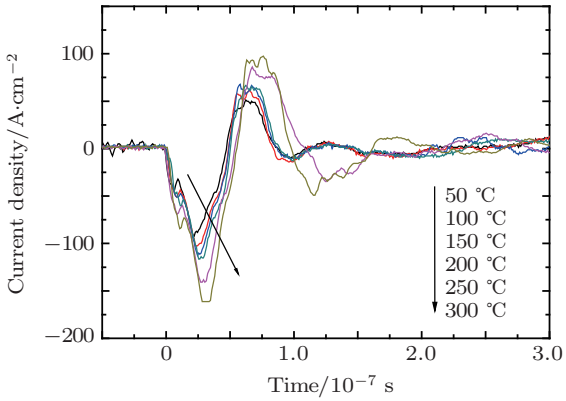


Fig. 8. (colour online) Temperature-dependent recovery characteristics of a JBS diode.

lifetime (from 500 to 200 ns) has been shown.[16] It demonstrates that SiC JBS diodes can operate at a fast switch speed and a high temperature.

4. Conclusion

4H–SiC SBD and JBS diodes with offset FP have been fabricated. DC tests show that the JBS diodes have excellent performances with a turn-on voltage of 0.85 V and a series resistance of 8.04 Ω. It also shows very good performances in the temperature range of 25–300 °C. Switch tests demonstrate that the JBS diodes have a fast switch speed. Reverse recovery time and peak reverse current density increase with operating temperature. Implantation of boron can be effectively used to improve the switch speed, and thus to reduce energy loss during switching.

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