Modeling of the drain-induced barrier lowering effect and optimization for a dual-channel 4H silicon carbide metal semiconductor field effect transistor*

Zhang Xian-Jun(张现军)†, Yang Yin-Tang(杨银堂), Duan Bao-Xing(段宝兴), Chai Chang-Chun(柴常春), Song Kun(宋 坤), and Chen Bin(陈 斌)

Key Laboratory of Wide Band Gap Semiconductor Materials and Devices of the Ministry of Education, School of Microelectronics, Xidian University, Xi'an 710071, *China*

A new analytical model to describe the drain-induced barrier lowering (DIBL) effect has been obtained by solving the two-dimensional (2D) Poisson's equation for the dual-channel 4H-SiC MESFET (DCFET). Using this analytical model, we calculate the threshold voltage shift and the sub-threshold slope factor of the DCFET, which characterize the DIBL effect. The results show that they are significantly dependent on the drain bias, gate length as well as the thickness and doping concentration of the two channel layers. Based on this analytical model, the structure parameters of the DCFET have been optimized in order to suppress the DIBL effect and improve the performance.

Keywords: drain-induced barrier lowering effect, Poisson's equation, metal semiconductor field effect transistor

PACS: 73.40.Jn, 85.30.Tv, 85.30.De **DOI:** 10.1088/1674-1056/21/3/037303

1. Introduction

SiC-based metal semiconductor field effect transistors (MESFETs) are emerging as a promising technology for high power microwave applications such as the transmitters for the commercial and military communications.[1] A number of reports in the literature describe excellent power and small-signal radio frequency (RF) characteristics for SiC MESFETs.[2−7] Recently, SiC MESFET with a dual-channel layer (DCFET) has been proposed, and its direct current (DC) characteristics are measured by experiments,[8] which are found to have an improved DC performance compared with the conventional single-channel layer devices by using the lower doped upper-channel layer and higher doped lower-channel layer to improve the breakdown voltage and the channel current. In order to obtain better RF performances, the gate length of the device should be reduced. Furthermore, with the development in the VLSI/ULSI technology, it is required for the device to decrease in size. However, for short-channel devices, the short-channel effects should not be overlooked. The drain-induced barrier lowering (DIBL) effect is the most pervasive effect in the short-channel devices which degrades the output conductance and consequently the gain of field effect transistor logic gates and amplifiers when it is present even to a small extent, and causes threshold voltage control problems and the current to be partially controlled by the drain potential rather than the gate potential when it is present to a great extent. High power and high frequency 4H-SiC MESFETs are particularly susceptible to this effect due to the large applied drain voltage and their short-channel length. Therefore, in order to understand and optimize the device characteristics, there is a need to develop an analytical model for the DIBL. The DIBL effect has been investigated analytically in Refs. [9–15] for the conventional MESFET. However, it has not been studied yet for the DCFET.

In this paper, we have studied the DIBL effect of the DCFET and derived the analytical models for the two-dimensional (2D) potential distribution function, threshold voltage and sub-threshold slope factor by solving 2D Poisson's equation. Furthermore, using these analytical models, we have optimized the structure parameters so as to suppress the DIBL effect and improve the performance of the DCFET.

*Project supported by the Pre-research Foundation from the National Ministries and Commissions of China (Grant No. 51308030201).

†Corresponding author. E-mail: xianjun_zhang@yahoo.com.cn

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2. Theoretical models

The cross-sectional view of the DCFET is shown in Fig. l, where the x coordinate represents the direction along the channel and the y coordinate represents the direction perpendicular to the surface. The gate length is L. The thickness and doping concentration are, respectively, a_0 and N_0 for the upper-channel layer, and a and $N_{\rm D}$ for the lower-channel layer. In the channel region, the 2D Poisson's equation can be written as

$$\frac{\partial^2 \Phi_1(x,y)}{\partial x^2}+\frac{\partial^2 \Phi_1(x,y)}{\partial y^2}=-\frac{qN_0}{\varepsilon},\ (-a_0<y<0), \tag{1a}$$

$$\frac{\partial^2 \Phi_2(x,y)}{\partial x^2}+\frac{\partial^2 \Phi_2(x,y)}{\partial y^2}=-\frac{qN_D}{\varepsilon},\ (0<y<a), \tag{1b}$$

where ε is the permittivity, and q is the electronic charge.

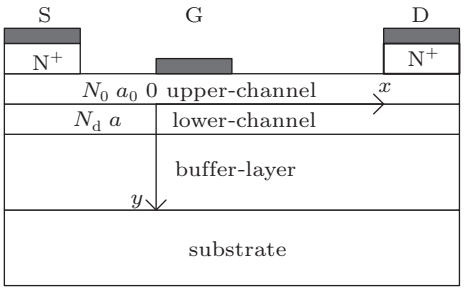


Fig. 1. The schematic diagram for the DCFET structure.

Under the condition that the gate–source and gate–drain resistances are omitted, the boundary conditions are

$$\Phi_1(x,-a_0)=U(-a_0)=\Phi_{\rm s0}, \tag{2a}$$

$$\frac{\partial \Phi_2}{\partial y}(x,a)=\frac{\partial U}{\partial y}(a), \tag{2b}$$

$$\Phi_1(x,0)=\Phi_2(x,0), \tag{2c}$$

$$\frac{\partial \Phi_1}{\partial y}(x,0)=\frac{\partial \Phi_2}{\partial y}(x,0), \tag{2d}$$

$$\Phi_1(0,y)=\Phi_2(0,y)=\Phi_{\rm ss}, \tag{2e}$$

$$\Phi_1(L,y)=\Phi_2(L,y)=\Phi_{\rm ss}+V_{\rm DS}, \tag{2f}$$

where $U(y)$ is the solution of 1D Poisson's equation, $\Phi_{\rm ss}$ is the built-in potential across the source/drain-to-substrate, $\Phi_{\rm s0}$ is the potential at the gate-channel interface, and $V_{\rm DS}$ is the applied drain bias.

According to the approach in Ref. [12], the potential $\Phi\ (x,y)$ in Eqs. (1a) and (1b) can be expressed as a superposition of two functions, $U(y)$ and $\Psi(x,y)$ as

$$\Phi(x,y)=U(y)+\Psi(x,y), \tag{3}$$

where $U(y)$ and $\Psi(x,y)$ satisfy the following equations:

$$\frac{\partial^2 U_1(y)}{\partial y^2}=-\frac{qN_0}{\varepsilon},\ (-a_0<y<0), \tag{4a}$$

$$\frac{\partial^2 U_2(y)}{\partial y^2}=-\frac{qN_{\rm D}}{\varepsilon},\ (0<y<a), \tag{4b}$$

$$\frac{\partial^2 \Psi(x,y)}{\partial x^2}+\frac{\partial^2 \Psi(x,y)}{\partial y^2}=0. \tag{4c}$$

Based on the boundary conditions (2a)–(2f), Eqs. (4a)–(4c) are solved as

$$U_{1(2)}(y)=-\frac{qN_{0(\rm D)}}{2\varepsilon}y^2+\frac{qN_{\rm D}a}{\varepsilon}y+\frac{qN_0a_0^2}{2\varepsilon}+\frac{qN_{\rm D}aa_0}{\varepsilon}+\varphi_{\rm s0}, \tag{5a}$$

$$\Psi_{1(2)}(x,y)=\sum_{k=0}^{\infty}\frac{n_{1(2)}(y)}{m}\Big[A_{1(2)k}\sinh\Big(\frac{(2k+1)\pi(L-x)}{2(a+a_0)}\Big)+B_{1(2)k}\sinh\Big(\frac{(2k+1)\pi x}{2(a+a_0)}\Big)\Big], \tag{5b}$$

where

$$m=\sinh\Big[\frac{(2k+1)\pi L}{2(a+a_0)}\Big],$$

$$n_{1(2)}(y)=\sin\Big[\frac{(2k+1)\pi y}{2(a+a_0)}\Big]+\tan\Big[\frac{(2k+1)\pi a_0(a)}{2(a+a_0)}\Big]\cos\Big[\frac{(2k+1)\pi y}{2(a+a_0)}\Big],$$

$$A_{1(2)k}=\frac{4(\phi_{\rm ss}-\phi_{\rm s0})}{(2k+1)\pi}-\frac{4q}{(2k+1)\pi\varepsilon}\Big(N_{\rm D}a^2-\frac{N_0a_0^2}{2}\Big)+\frac{4q}{(2k+1)\pi\varepsilon}\Big\{N_{0(\rm D)}(a+a_0)^2\Big[1-\frac{4}{(2k+1)^2\pi^2}\Big]\Big\},$$

$$B_{1(2)k}=A_{1(2)k}+\frac{4V_{\rm DS}}{(2k+1)\pi}.$$

Thus, the potential solution $\Phi(x,y)$ is

$$\Phi_{1(2)}(x,y)=U_{1(2)}(y)+\Psi_{1(2)}(x,y). \tag{6}$$

From the obtained results, we can see that the potential distribution is symmetrical about the channel midpoint. At $y=0$ level, the minimum vertical electric field is obtained at $x=L/2$ from Eq. (7) as

$$-\frac{\partial}{\partial x}\Big[\Big(\frac{\partial \Phi(x,y)}{\partial y}\Big)_{y=0}\Big]=0. \tag{7}$$

Therefore, the minimum vertical electric field is

$$E_{y\min} = E\Big(\frac{L}{2}, 0\Big) = \frac{qN_{\rm D}a}{\varepsilon} + \Delta E_{y\min}, \qquad (8)$$

where

$$\Delta E_{y\min} = \xi \sum_{k=0}^{\infty} \Big[-\frac{(2k+1)\pi L}{4(a+a_0)}\Big] + \zeta \sum_{k=0}^{\infty} \frac{\exp\Big(-\frac{(2k+1)\pi L}{4(a+a_0)}\Big)}{[(2k+1)\pi]^2},$$

$$\xi = \frac{2}{a+a_0}\Big\{2(\phi_{\rm ss} - \phi_{\rm s0}), + \frac{2q}{\varepsilon}\Big[N_{\rm D}(a+a_0)^2 - N_{\rm D}a^2 - \frac{N_0 a_0^2}{2}\Big] + V_{\rm DS}\Big\},$$

$$\zeta = -\frac{16qN_{\rm D}(a+a_0)}{\varepsilon}.$$

At threshold of a long channel device, all the field lines from the gate terminate on the ionized donor charges in the completely depleted channel.[11] However, when the channel length decreases, a part of the vertical field lines at the surface terminates on source and drain instead and the DIBL effect occurs. The $\Delta E_{y\min}$ is the extent of electric field induced by DIBL effect. Thus, when a gate bias which equals the long-channel threshold voltage ($V_{\rm TL}$) is applied to the short-channel device, the charge per unit area terminating at the midpoint of the channel between source and drain is $qN_{\rm D}a - \varepsilon\Delta E_{y\min}$. To achieve the threshold condition (that is, complete depletion of the channel at midpoint), an additional negative voltage should be applied to the gate to supply the excess charge equal to $\varepsilon\Delta E_{y\min}$. Therefore, the short-channel threshold voltage is $V_{\rm TS} = V_{\rm TL} - \Delta V_{\rm T}$, where $\Delta V_{\rm T} = \Delta E_{y\min}a$ is the DIBL-induced short-channel threshold voltage shift. Summing the first infinite series and taking the first term of the second series, we obtain the expression of the drain bias induced threshold voltage shift $\Delta V_{\rm T}$ as

$$\Delta V_{\rm T} = \xi a \frac{\exp\Big[-\frac{\pi L}{4(a+a_0)}\Big]}{1-\exp\Big[-\frac{\pi L}{2(a+a_0)}\Big]} + \zeta\frac{a}{\pi^2}\exp\Big[-\frac{\pi L}{4(a+a_0)}\Big]. \qquad (9)$$

For SiC MESFET, the sub-threshold slope factor ($N_{\rm s}$) is also of interest for the researchers since it is a measure of the coupling between the gate bias and the channel potential minimum $\Phi_{\rm cmin}$ and its value evaluates the extent of the DIBL. The sub-threshold slope factor can be expressed by

$$\frac{1}{N_{\rm s}} = \frac{\partial\Phi_{\rm cmin}}{\partial V_{\rm GS}}, \ (V_{\rm GS} = V_{\rm TL}, V_{\rm DS} = 0), \qquad (10)$$

where $\Phi_{\rm cmin}$ is obtained from the potential function $\Phi(x,y)$ by substituting $x = L/2$ and $y = a$. Taking only the first term of the infinite summation series, we obtain

$$\Phi_{\rm cmin} = \Gamma + \phi_{\rm s0} + 2\eta\left(R + \frac{2V_{\rm DS}}{\pi}\right), \qquad (11)$$

where

$$\Gamma = \frac{qN_{\rm D}a^2}{2\varepsilon} + \frac{qN_0a_0^2}{2\varepsilon} + \frac{qN_{\rm D}aa_0}{\varepsilon} + \phi_{\rm s0},$$

$$\eta = \Big[\sin\Big(\frac{\pi a}{2(a+a_0)}\Big) + \cot\Big(\frac{\pi a}{2(a+a_0)}\Big)\cos\Big(\frac{\pi a}{2(a+a_0)}\Big)\Big] \times \exp\Big[-\frac{\pi L}{4(a+a_0)}\Big],$$

$$R = \frac{4}{\pi}\Big[E_{\rm n} - \frac{2qN_{\rm D}aa_0}{\varepsilon} - \frac{2qN_{\rm D}a^2}{2\varepsilon} + \frac{qN_{\rm D}(a+a_0)^2}{\varepsilon}(1-\frac{4}{\pi^2})\Big].$$

From Eqs. (10) and (11), we obtain the sub-threshold slope factor

$$N_{\rm s} = \frac{1}{1-\frac{8}{\pi}\eta}. \qquad (12)$$

3. Results and discussion

Using our obtained models, we calculate the channel potential, threshold voltage shift, and sub-threshold slope factor of the DCFET. Under condition that $y = a$ in the potential distribution function $\Phi_2(x,y)$, the channel potential is obtained. Figure 2 is the channel potential variation in the channel direction. It is shown that there is a minimum for the channel potential which is located about in the middle of the channel. Thus, there exists a potential barrier near the source which comes from the potential difference between the source potential and the channel potential minimum. This potential barrier is the equivalent of that in the p–n junction between the source and the channel in MOSFETs. It is just this potential barrier that limits the sub-threshold drain current in DCFET. To show the effect of the drain bias on the potential barrier, three potential curves are plotted in Fig. 2 for $V_{\rm DS} = 1$ V, 2 V, and 3 V, respectively. It can be seen that the potential minimum depends on the drain bias is, that is, the larger the drain bias is, the higher the potential minimum is. Therefore, increasing the drain bias lowers the potential barrier and the DIBL effect appears. This effect adversely affects the subthreshold characteristics of the device and should be minimized. Figure 3 shows the channel potential variation in the channel direction with the doping concentration and thickness of the two channel layers as the parameters. From the results we can see that higher doping concentration and lower thickness of the channel layer will

suppress the DIBL effect, which is in agreement with the results in Ref. [11].

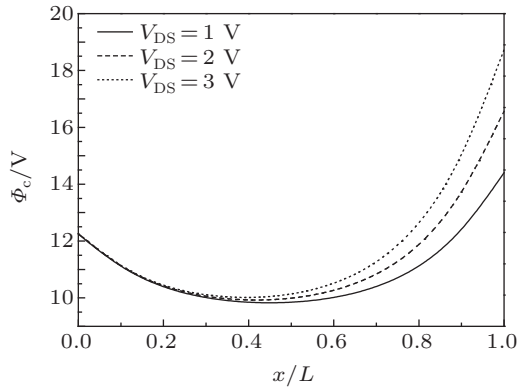


Fig. 2. Variation of the channel potential Φ_c in the sub-threshold region with respect to the normalized position from source to drain for the DCFET at V_{DS}=1 V (solid line), V_{DS} = 2 V (dash line), and V_{DS} = 3 V (dot line). The other parameters are $L = 0.7$ μm, $N_D = 5.2 \times 10^{17}$ cm^{-3}, $a = 0.08$ μm, $N_0 = 1.4 \times 10^{17}$ cm^{-3}, $a_0 = 0.12$ μm.

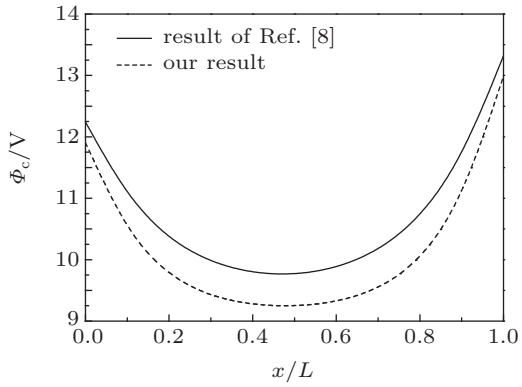


Fig. 3. The channel potential versus the normalized position from source to drain for different channel dopings and thicknesses. $N_D = 5.2 \times 10^{17}$ cm^{-3}, $a = 0.08$ μm, $N_0 = 1.4 \times 10^{17}$ cm^{-3}, $a_0 = 0.12$ μm (solid line); $N_D = 9.0 \times 10^{17}$ cm^{-3}, $a = 0.06$ μm, $N_0 = 1.0 \times 10^{17}$ cm^{-3}, $a_0 = 0.09$ μm (dash line). $V_{DS} = 0.5$ V.

One of the negative effects caused by the DIBL effect is the threshold voltage shift, which is shown in Figs. 4 and 5. It can be seen that increasing the drain bias results in the threshold voltage degradation. This degradation happens because when the drain bias is increased, more field lines penetrate to the middle of the channel from the drain end. This degradation is more significant for shorter channel devices. For $L = 2.0$ μm, the threshold voltage is almost fixed. In contrast, for $L = 0.5$ μm, the threshold voltage is decreased evidently when the drain bias is increased from 0 V to 30 V.

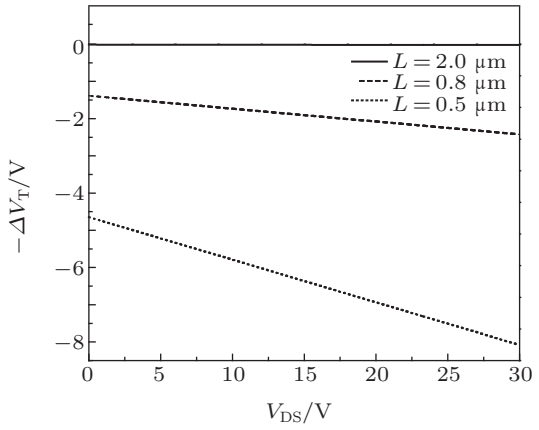


Fig. 4. The threshold voltage shift ($-\Delta V_T$) versus the drain bias for channel length of 2.0 μm (solid line), 0.8 μm (dash line), and 0.5 μm (dot line). $N_D = 5.2 \times 10^{17}$ cm^{-3}, $a = 0.08$ μm, $N_0 = 1.4 \times 10^{17}$ cm^{-3}, $a_0 = 0.12$ μm.

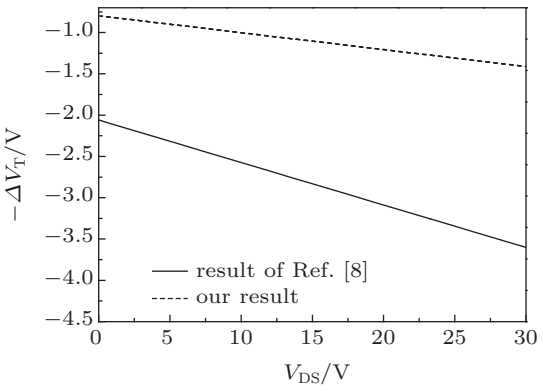


Fig. 5. The threshold voltage shift ($-\Delta V_T$) versus the drain bias for different channel dopings and thicknesses. $L = 0.7$ μm. $N_D = 5.2 \times 10^{17}$ cm^{-3}, $a = 0.08$ μm, $N_0 = 1.4 \times 10^{17}$ cm^{-3}, $a_0 = 0.12$ μm (solid line); $N_D = 9.0 \times 10^{17}$ cm^{-3}, $a = 0.06$ μm, $N_0 = 1.0 \times 10^{17}$ cm^{-3}, $a_0 = 0.09$ μm (dash line).

The threshold voltage shift as a function of the gate length is shown in Fig. 6 with the channel thickness and doping concentration as the parameters. When the gate length is more than 2 μm, that is, the DCFET is regarded as a long channel device, the threshold voltage is not degraded and the device exhibits a long-channel characteristics for both Zhu's and our optimized parameters. However, when the gate length is reduced, the DIBL effect is gradually significant and the threshold voltage is decreased. For example, when the gate length is reduced from 2 μm to 0.3 μm, the threshold voltage is degraded by 7 V for our optimized parameters, in comparison with 12 V for Zhu's parameters. Thus, the DIBL effect is suppressed and the performance for the threshold voltage is significantly improved after our optimization, as is also indicated in Fig. 5.

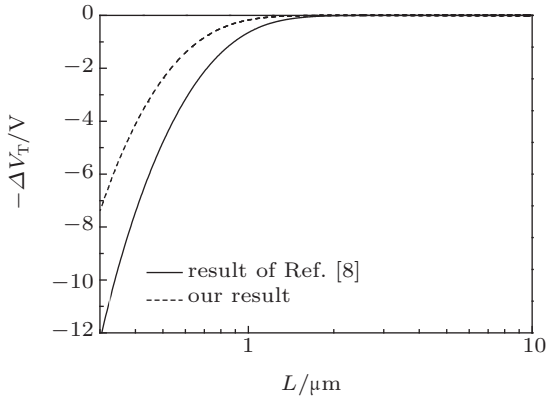


Fig. 6. The threshold voltage shift ($-\Delta V_T$) versus the channel length for different channel dopings and thicknesses. $V_{DS} = 0.5$ V. $N_D = 5.2\times10^{17}$ cm^{-3}, $a = 0.08$ μm, $N_0 = 1.4 \times 10^{17}$ cm^{-3}, $a_0 = 0.12$ μm (solid line); $N_D = 9.0 \times 10^{17}$ cm^{-3}, $a = 0.06$ μm, $N_0 = 1.0 \times 10^{17}$ cm^{-3}, $a_0 = 0.09$ μm (dash line).

The sub-threshold slope factor is also important for the SiC MESFET, since it is a measure of the coupling between the gate bias and channel potential minimum, and reflects the capability of the gate electrode to control the sub-threshold drain current. Figure 7 shows the dependence of the sub-threshold slope factor on the gate length. It is indicated that the sub-threshold slope factor is increased when the gate length is decreased or the DIBL effect is more significant. For comparison, our optimized result is also plotted in Fig. 7. For the same gate length, our obtained sub-threshold slope factor is smaller than that for Zhu's parameters. From the sub-threshold drain current expression in Eq. (13),[14] we can see that the sub-threshold drain current is more sensitive to the gate bias for smaller N_s. Therefore, it demonstrates better capability of the gate to control the

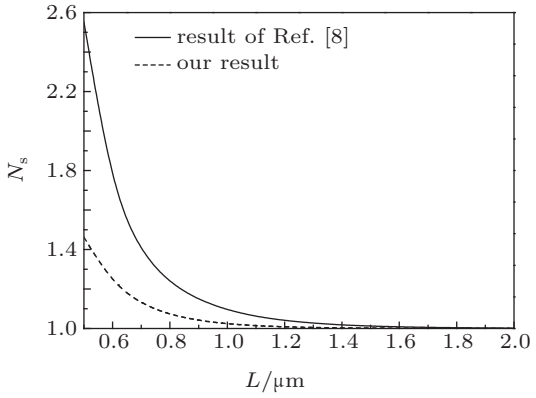


Fig. 7. The sub-threshold slope (N_s) factor versus the channel length for different channel dopings and thicknesses. $N_D = 5.2 \times 10^{17}$ cm^{-3}, $a = 0.08$ μm, $N_0 = 1.4 \times 10^{17}$ cm^{-3}, $a_0 = 0.12$ μm (solid line); $N_D = 9.0 \times 10^{17}$ cm^{-3}, $a = 0.06$ μm, $N_0 = 1.0 \times 10^{17}$ cm^{-3}, $a_0 = 0.09$ μm (dash line).

sub-threshold drain current for our optimized channel parameters,

$$I_{DS} = WJ_{s0}\Big[1 - \exp\Big(-\frac{qcV_{DS}}{kT}\Big)\Big] \times \exp\Big[\frac{q}{N_s kT}(1 - \alpha V_{DS})(V_{GS} - V_{TL} + \gamma V_{DS})\Big]. \quad (13)$$

4. Conclusion

In this paper, an analytical model to describe the DIBL effect for the DCFET is derived by solving 2D Poisson's equation. Using this obtained analytical model, we have obtained the dependence of the DIBL effect on the drain bias, gate length, as well as the thickness and doping concentration of the two channel layers. The results showed that the larger the drain bias and channel thickness are, or the smaller the gate length and doping concentration are, the more significant the DIBL effect is. Thus, the DIBL effect of the DCFET can be minimized by optimizing the thickness and doping concentration of the two channel layers in condition that the drain bias and gate length are fixed. The achieved analytical model of the DIBL effect and the calculated results will supply valuable references to the improvement in the performance of the power microwave semiconductor devices.

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