Recovery of single event upset in advanced complementary metal–oxide semiconductor static random access memory cells*

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Using computer-aided design three-dimensional (3D) simulation technology, the recovery mechanism of single event upset and the effects of spacing and hit angle on the recovery are studied. It is found that the multi-node charge collection plays a key role in recovery and shielding the charge sharing by adding guard rings. It cannot exhibit the recovery effect. It is also indicated that the upset linear energy transfer (LET) threshold is kept constant while the recovery LET threshold increases as the spacing increases. Additionally, the effect of incident angle on recovery is analysed and it is shown that a larger angle can bring about a stronger charge sharing effect, thus strengthening the recovery ability.

Keywords: single event upset, multi-node charge collection, static random access memory, angular dependence

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1. Introduction

Among all the reliability issues concerned, radiation-induced soft error is becoming more and more noticeable in defense and space systems.[1−4] Single event transients (SETs) on nodes of cross-coupled inverters may lead to single event upset (SEU) on storage cells such as static random access memories (SRAMs) and flip-flops. With device size shrinking and circuit frequency increasing, the probability of a single particle causing SET in a circuit or depositing charge on multiple nodes increases.[5−8] Previous investigations in 130-nm and 90-nm bulk complementary metal–oxide semiconductors (CMOSs) have shown how dual interlocked cell (DICE) latches are vulnerable to upset in these technologies.[9,10]

SRAMs are ubiquitous in modern integrated circuits (ICs) and SRAM is more prone to soft errors because of larger sensitive volume (SV) and lower node capacitance than its dynamic counterpart.[6] In addition, the soft error rate (SER) in SRAMs increases with technology shrinking.[11,12] As SRAM cells have scaled down in size, a new effect is observed: a different mechanism for SRAM SEU due to indirect charge collection.[13] Black *et al.*[13] used technology computer-aided design (TCAD) simulations to demonstrate that the SRAM design upsets with less charge deposition, but then recovers the original state when the linear energy transfer (LET) is much larger. The initial flip is due to direct charge collection, while the entrance into, and the recovery from, the metastable state are due to indirect charge collection.

In this work we analyse the recovery mechanism of SEU for the SRAM cell. It is found that this phenomenon is caused by the charge collection of the adjacent p-channel metal–oxide–semiconductor (PMOS) and the recovery LET threshold is closely related to multi-node charge collection. Finally, the effects of spacing and incident angle on recovery are also investigated.

2. Description of the recovery mechanism

A commercial SRAM cell, which consists of six transistors, is shown in Fig. 1: two cross-coupled inverters and two access pass-gate transistors. A three-dimensional (3D) device/circuit mixed mode is constructed using Synopsys TCAD, where P1 and P2 use

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the 3D TCAD model while other transistors use the SPICE models. The unhardened SRAM cell is fabricated by 90-nm complementary metal–oxide semiconductor (CMOS) bulk technology, which is the same as that in Ref. [14]. The doping profiles are calibrated within the 3D model by process simulation and an inverse modeling approach[15] and the I–V characteristics between TCAD and SPICE simulations are in good agreement. The 3D dual-PMOS model is shown in Fig. 2.

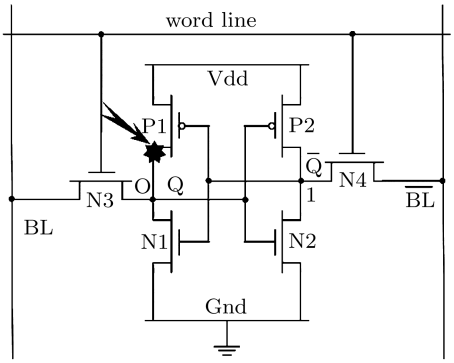


Fig. 1. Schematic illustration of a commercial SRAM cell.

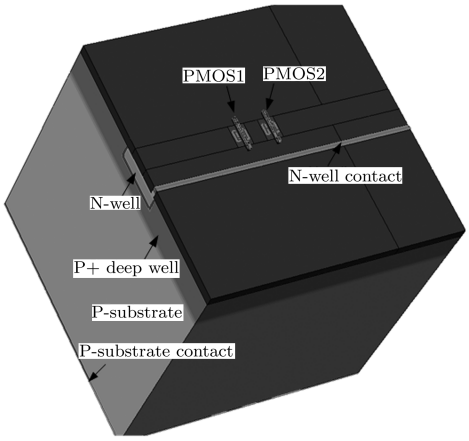


Fig. 2. A 3D dual-PMOS model for 90-nm bulk CMOS.

For all simulations, the following physical models are used: (i) Fermi–Dirac statistics, (ii) band-gap narrowing effect, (iii) doping-dependent Shockley–Read–Hall (SRH) recombination and Auger recombination, (iv) temperature, doping, electric field and carrier–carrier scattering effects on mobility, (v) incident heavy ions are modeled by using a Gaussian radial profile with a characteristic $1/e$ radius of 30 nm and a Gaussian temporal profile with a characteristic decay time of 0.5 ps. All simulations are conducted by using the YINHE computing cluster.

Assume that the storage state of Q is low. At first, P1 is off and P2 is on. If a particle strikes the drain of off-state P1, the logic low state at Q is driven to a high state due to the charge collection. Figure 3 shows the voltage pulses of Q at different LETs of strike particles. With the increase of LET, in the design SRAM cell would occur SEU, but the storage state can recover to a low state when LET is large enough.

In order to eliminate the interaction between P1 and P2 during charge collection in device level, two individual PMOS models are designed on separated wafers and are connected just by metal lines in the SPICE level, which is called the separated model. TCAD simulations show that the SEU threshold for separated model is 2 MeV $\cdot$ cm^2/mg, which is the same as that obtained from the dual-PMOS model, but the state of Q cannot recover by increasing LET. It means that the recovery mechanism is caused by multi-node charge collection.

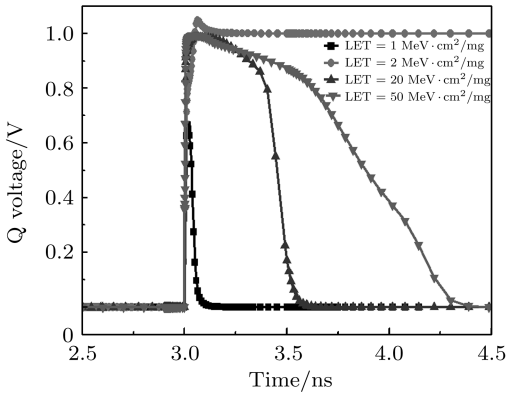


Fig. 3. Voltage pulses of Q at different LETs of striking particles.

3. Results and discussion

3.1. Simulation of the recovery mechanism

To ensure that the SEU recovery is caused by delayed charge sharing at $\bar{Q}$, the same simulation mode and hit location are used and the hit time is 3 ns, but the storage state is opposite (i.e., hit P1 is on and adjacent P2 is off), in order to observe the effect of the delayed charge collection at the adjacent P2 on Q directly. For this simulation set up, the hit P1 does not result in an SEU at Q because it will not collect charge at first, and the resulting SEU at Q is due to charge sharing only.

The waveforms of $\bar{Q}$ after particles striking in the conditions of P1 on and off are plotted in Fig. 4. For the case of hit P1 off, Q state will upset after the striking, thus P2 turns off and $\bar{Q}$ jumps from high to low. When P2 becomes off, it will collect the charge generated from the struck node Q. The $\bar{Q}$ will jump to high state again because of the multi-node charge collection. This low-to-high transition at $\bar{Q}$ "resets" the node voltage to the pre-event state, which will "recover" Q node to low state directly. As shown in Fig. 4, the $\bar{Q}$ waveforms for both hit P1 on and off cases are the same after particles striking, which verifies that the recovery mechanism is caused by the charge collection of the adjacent PMOS. Figure 5 shows the Q states for both hit P1 on and off cases after particles striking. It can be seen that Q will recover from the turbulence soon in hit P1 off case and the waveform in this case is totally the same as that in the hit P1 on case after striking. The transition at Q is also due to the multi-node charge collection, which is analysed above in detail.

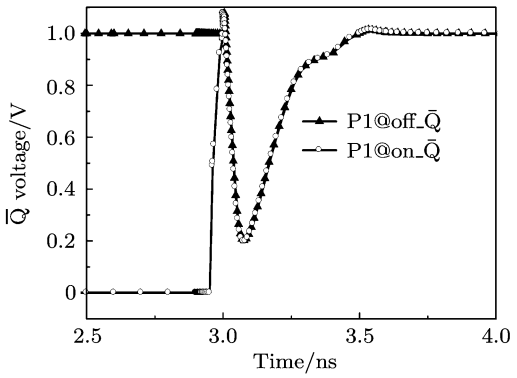


Fig. 4. The $\bar{Q}$ waveforms after strike in the conditions of P1 on and off.

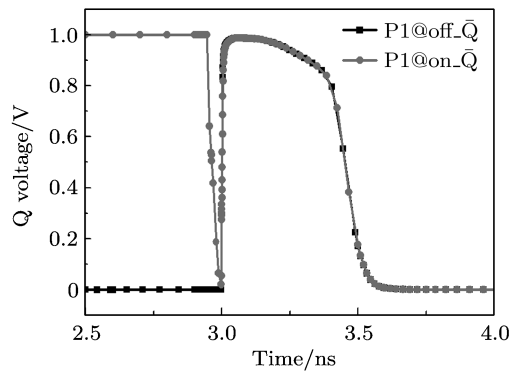


Fig. 5. The Q waveforms after the strike in the conditions of P1 on and off.

3.2. Effects of charge sharing on recovery

It is known that multi-node charge collection is the key contributor to the recovery mechanism. SRAM cells with strong charge sharing should exhibit strong recovery effect and can reduce the dependence of soft error rates (SERs) on LET. Consequently, mitigation of charge sharing should also mitigate recovery. That is, SRAM cells with reduced charge sharing should exhibit a stronger LET dependence on SER.

The using of guard rings is a successful technique in mitigating charge sharing.[16] It can reduce the effect of charge sharing by serving as a charge sink, thus maintaining the bulk potential to a fixed level. 3D TCAD simulations for 90-nm bulk CMOS technology are performed to compare the effects of charge sharing on adjacent PMOS both with and without guard bands. Figure 6 shows the TCAD 3D dual-PMOS models for 90-nm CMOS technology without and with guard rings where the two PMOS transistors in panel (a) are without guard rings while the ones in panel (b) are surrounded by N-well contacts. Except for the presence of guard rings, the rest of the simulation setup is kept the same for both cases, including the TCAD 3D device parameters.

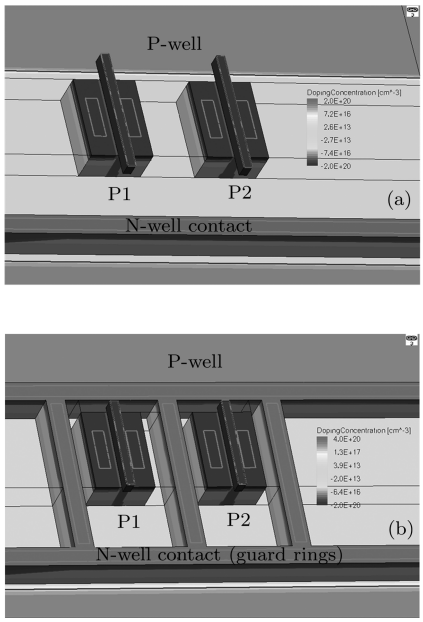


Fig. 6. The 3D dual-PMOS models for 90-nm bulk CMOS without (a) / with (b) guard rings.

The amount of charge collected versus LET in these two cases are shown in Fig. 7. It can be discovered that the charge sharing for transistor without guard ring is different from that with guard ring and

the existence of the guard rings can reduce the multi-node charge collection greatly.

Figure 8 shows the voltage pulses of Q at different LETs of striking particles where the 3D dual-PMOS model is used and the transistors are equipped with guard rings. By comparison with the case in Fig. 3, the SEU occurs in the designed SRAM with the increase of LET and the SEU threshold is 2 MeV $\cdot$ cm^2/mg which is the same as that obtained with the separated model, but the storage state cannot recover to low state again when LET is large enough. This is because the guard rings will suppress the excess carriers collected by the adjacent transistor and the upset state cannot be redressed through multi-node charge collection.

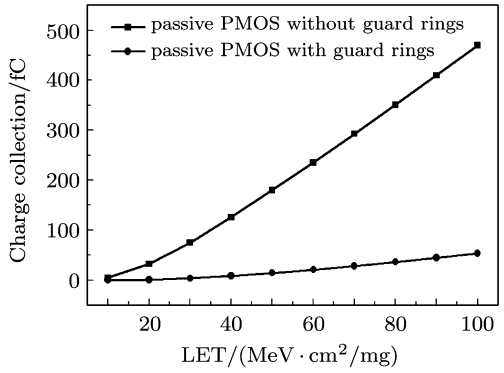


Fig. 7. The amount of charge collected for the cases without/with guard rings.

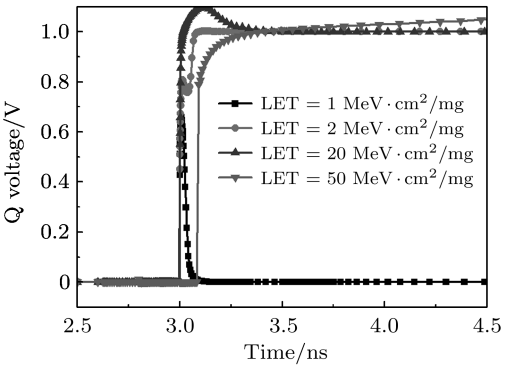


Fig. 8. Voltages of Q at different LETs of striking particles where the PMOS transistors are equipped with guard rings.

4. Effects of spacing and incident angle on recovery

4.1. Spacing dependence

Upset LET threshold is the smallest LET causing SRAM cells to upset and we here define recovery LET threshold as the smallest LET for SRAM to recover again after the upset. According to illustrations mentioned above, it is known that the storage state of SRAM can only maintain the opposite state when LET is larger than the upset threshold and smaller than the recovery threshold. Table 1 shows the upset and the recovery threshold values for different transistor spacings. Only the spacing between P1 and P2 in Fig. 1 is changed and the rest of the simulation parameters are kept unchanged. It can be seen that the upset LET threshold remains the same for different spacings, while the recovery LET threshold is proportional to transistor spacing.

The upset of SRAM state is caused by the charge collection of the struck node directly and the SEU will occur in Q when the amount of charge collected is larger than the critical charge for the upset, so the upset LET threshold is determined by the direct charge collection and is independent of the charge collection of the adjacent transistor. The recovery mechanism is mainly caused by multi-node charge collection and the charge sharing will decrease as the spacing increases, thus the recovery of Q state needs large LET. This is the reason why the recovery LET threshold increases as spacing increases.

Table 1. Upset threshold and recovery threshold values of SRAMs for different spacings.

Spacing /μm	Upset LET threshold /(MeV $\cdot$ cm^2/mg)	Recovery LET threshold /(MeV $\cdot$ cm^2/mg)
0.14	2.5	8
0.5	2.5	19
1.0	2.5	37
1.5	2.5	66

4.2. Angular dependence

The amount of charge collected is determined by the strike trace in SV and the incident angle of particles will change the length and the range of collection, thus affecting the charge collection of adjacent PMOS transistors. The capabilities of upset and recovery will also be different as the incidence angle changes.

The angle of hit particles is illustrated in Fig. 9 and the normal incidence is perpendicular to the drain of P1. Taking the cases where the hit direction is 15°, 30° and 60° tilting with respect to P2 for example, we study the effects of the incident angle on the recovery mechanism in four different situations as shown in Fig. 10. It can be seen that the SET voltage pulses at Q node are quite different for different incidence angles. The larger the hit angle, the less the pulse width is. When the incidence angle is 60°, Q state will recover immediately after the upset and the pulse width

is just about 70 ps. The conclusion can be made after analysing the strike trace in Fig. 9 that the excess carriers produced by particles will be far from P1 and are drawn near to P2 when the hit angle increases. At the same time, the larger the hit angle, the less the charge collected by P1 is and so the larger charge can be collected by the adjacent transistor P2, thus the strength of recovery will be enhanced at a larger incident angle.

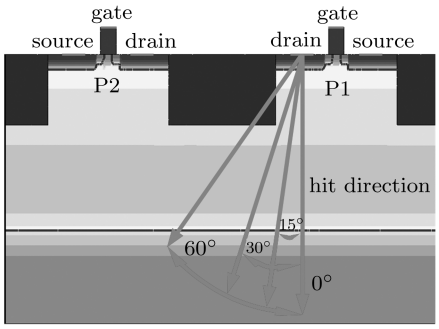


Fig. 9. Two-dimensional slice of two PMOS transistors illustrating the angle of hit particles.

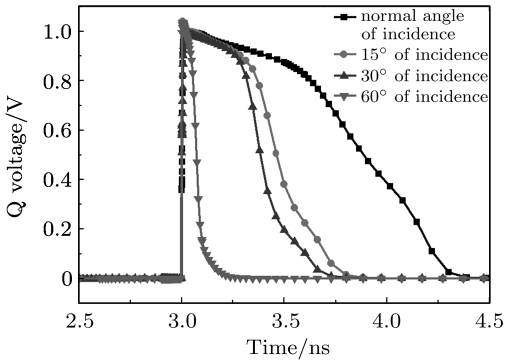


Fig. 10. The Q node pulses when particles are at four different incident angles.

5. Conclusion

Based on 90-nm bulk CMOS technology, the recovery mechanism of SEU in SRAM cells and the effects of spacing and hit angle dependence on the recovery are studied using TCAD 3D simulation. It is found that the multi-node charge collection plays a key role in the recovery and shielding the charge sharing by adding guard rings cannot exhibit the recovery effect. By comparing the charge collections between structures with and without guard rings, it is concluded that the recovery effect is caused by indirect charge collection. It is also indicated that the upset LET threshold is kept constant while the recovery LET threshold increases with the spacing. That is because charge sharing will decrease as spacing increases, thus the Q state would need larger LET to recover when the spacing is larger. Additionally, the effect of incidence angle on the recovery of Q state is analysed and it is shown that a larger angle can bring about stronger charge sharing effect, thus strengthening the recovery ability.

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