An RLC interconnect analyzable crosstalk model considering self-heating effect*

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According to the thermal profile of actual multilevel interconnects, in this paper we propose a temperature distribution model of multilevel interconnects and derive an analytical crosstalk model for the distributed resistance–inductance–capacitance (RLC) interconnect considering effect of thermal profile. According to the 65-nm complementary metal–oxide semiconductor (CMOS) process, we compare the proposed RLC analytical crosstalk model with the Hspice simulation results for different interconnect coupling conditions and the absolute error is within 6.5%. The computed results of the proposed analytical crosstalk model show that RCL crosstalk decreases with the increase of current density and increases with the increase of insulator thickness. This analytical crosstalk model can be applied to the electronic design automation (EDA) and the design optimization for nanometer CMOS integrated circuits.

Keywords: multilevel interconnects, temperature distribution, RLC crosstalk

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1. Introduction

With the development of nanometer level complementary metal–oxide semiconductor (CMOS) integrated circuits, the integration density and the power losses of the system chip grow unceasingly, thereby causing the thermal problem of metal interconnect to be more and more serious. So, people pay more attention to the influence of the interconnect thermal effect on the performance and the design of integrated circuits.[1−4] With the further increases of the layer of metal interconnect and the current density of nanometer level high performance integrated circuits, the interconnect self-heating effect has already become one of the primary effects on the interconnect reliability and the signal integrality. Meanwhile, the influence of inductance coupling on crosstalk cannot be neglected due to the fact that as the frequency of system clock increases continuously,[5−8] crosstalk is more and more influenced by the technological parameters of the integrated circuits.[9,10] Therefore, it is necessary to analyse the influence of the thermal profile effect of multilevel interconnects on the resistance–inductance–capacitance (RLC) crosstalk.

As a hot research topic, the thermal problem of the interconnect has already been deeply studied.[1−5,8−13] In Ref. [1] an analytical expression of thermal profile of a single interconnect through the heat diffusion equation was deduced, but the influence of the via and fringe effects on the thermal profile of multilevel interconnect were not taken into consideration, thereby resulting in higher interconnect temperature than the actual interconnect temperature distribution. Wang and Zhou[2] considered the influence of via and fringe effects and obtained an analytical model of thermal profile of multilevel metal interconnects quite close to the actual condition. However, they only took the via as a heat conduction channel and they did not consider the influence of via self-heating effect. The via self-heating has already become a very important heat source of the integrated circuits and affects the temperature distribution of metal interconnects. For the nanometer level multilevel interconnects, the via self-heating effect cannot be neglected.[3] In Refs. [1] and [4] the influence of interconnect temperature distribution effect on the interconnect delay based on these temperature models was studied. However, in these studies the influences of the temperature distribution effect on interconnect crosstalk were not considered. As the CMOS integrated circuits develop into nanometer level, the influence of inductive coupling effect strengthens gradually and interconnect analytical

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crosstalk model also develops from the RC model to a more accurate RLC model,[5,6,8] but in these models the aggressive influence of interconnect self-heating effect on the RLC crosstalk is not taken into consideration.

In this paper, we analyse the temperature distribution of multilevel interconnect based on the interconnect parameter of the 65-nm CMOS process, propose a kind of multilevel interconnect temperature distribution model, then, use the analytical RLC crosstalk model in Ref. [5] to develop a kind of analytical RLC crosstalk model with considering thermal profile, which is verified based on the intermediate and global interconnect of the 65-nm CMOS process and carry on the analysis and discussion on the results.

2. Multilevel interconnect temperature distribution model

The structure of integrated circuits is becoming more and more complex as the layer of metal interconnect increases in the nanometer level CMOS processing, International Semiconductor Technology Road Map (ITRS)[14] pointed out in 2007 that in the future the number of layers of interconnects will achieve 13 or more, for such a complex interconnect structure and huge interconnect network, it is difficult to obtain an exactly analytical expression of the thermal profile as proposed in Ref. [1]. Furthermore, the via self-heating has already become a very important heat source of integrated circuit since the diameter of the via further reduces in ultra-large-scale integration (ULSI).[3] Therefore, in this paper we take via not only as a heat conduction channel, but also as an important heat source that affects the interconnect thermal profile.

A multilevel interconnect structure is shown in Fig. 1. For the i-th layer metal interconnects, $w_{\mathrm{m},i}$ is denoted as the interconnect width, $t_{\mathrm{m},i}$ the metal thickness, L_i the length, d_i the spacing of the interconnect in the same layer, h_i the insulator thickness, D_i the via diameter (generally speaking, the via diameter may be smaller than or equal to the width of the interconnect, in this paper the via diameter is taken to be equal to the interconnect width), $T_i(x)$ the temperature profile of the i-th interconnect, $T_{i-1}(x)$ the temperature profile of the (i–1)-th interconnect, K_{ins} the heat conductivity of the insulator, K_{m} the metal heat conductivity (here, the heat conductivity is assumed to be a constan[1,2,4]), $L_{D,i}$ the heat diffusion length of the interconnect, $J_{\mathrm{m},i}$ the interconnect current density, ρ_{m} the resistivity of metal at 0 °C, β the temperature coefficient of metal resistivity, ρ_{v} the via resistivity and $J_{\mathrm{v},i}$ the via current density.

Assume that the joule heat produced by interconnects is divided into two parts, which is shown in Fig. 2, i.e., the joule heat Q_{via} produced by the interconnect on the top of the via and the self-heating $Q_{\mathrm{via,self\text{-}heat}}$ of the via, which transmits directly

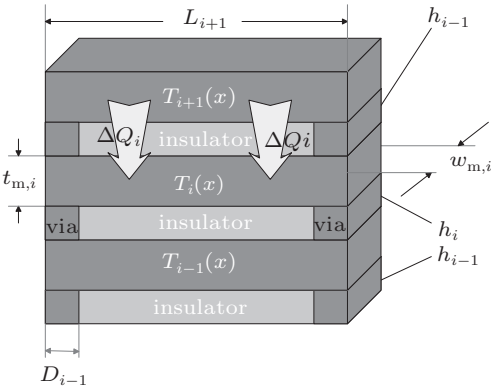


Fig. 1. Schematic illustration of multilevel interconnect structure.

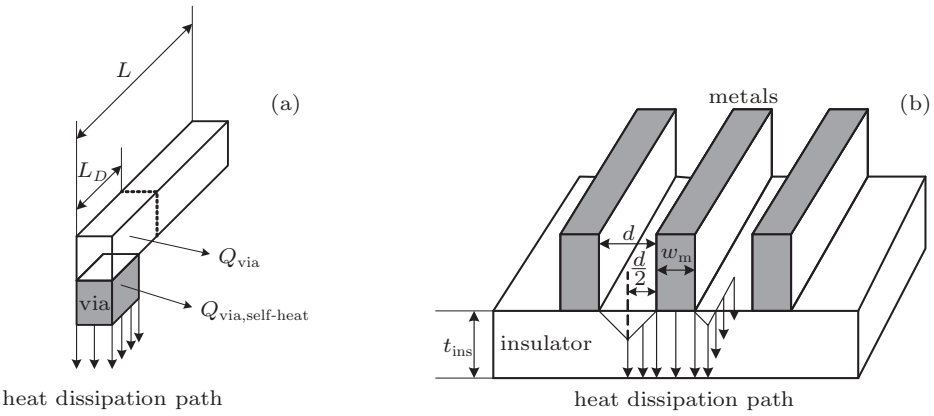


Fig. 2. Schematic illustration of multilevel interconnect heat transmission: (a) heat transmission through via, (b) heat transmission through insulator.

through the via to its connected next metal, which is represented by $Q^*_{\rm via}$ and the joule heat produced by the other parts ($Q_{\rm ins}$) that transmits completely through the insulator to the next metal, then we can obtain expressions as follows:[2]

$$Q_{\rm via,self\text{-}heat} = \Big(J_{v,i+1}\cdot\frac{\pi D^2_{i+1}}{4}\Big)^2\cdot\left(\frac{\rho_v\cdot h_{i+1}}{\frac{\pi D^2_{i+1}}{4}}\right), \tag{1}$$

$$Q_{\rm via} = (J_{{\rm m},i+1}\cdot w_{{\rm m},i+1}\cdot t_{{\rm m},i+1})^2\cdot\Big(\frac{\rho_{\rm m}\cdot L_{D,i+1}}{w_{{\rm m},i+1}\cdot t_{{\rm m},i+1}}\Big) = J^2_{{\rm m},i+1}\cdot\rho_{\rm m}\cdot L_{D,i+1}\cdot w_{{\rm m},i+1}\cdot t_{{\rm m},i+1}, \tag{2}$$

$$Q^*_{\rm via} = Q_{\rm via,self\text{-}heat} + Q_{\rm via}, \tag{3}$$

$$Q_{\rm ins} = L_i w_{{\rm m},i}\Big\{J^2_{{\rm m},i+1}\rho_{\rm m}t_{{\rm m},i+1}\cdot\frac{w_{{\rm m},i+1}}{w_{{\rm m},i+1}+d_{i+1}}\cdot\frac{L_{i+1}-2\cdot L_{D,i+1}}{L_{i+1}} + \sum_{j=i+2}^{n}\Big(J^2_{m,j}\rho_{\rm m}t_{m,j}\cdot\frac{w_j}{w_j+d_j}\Big)\Big\}. \tag{4}$$

Thus heat transmitting to the i-th interconnect from upper interconnects is

$$\Delta Q_i = 2Q^*_{\rm via} + Q_{\rm ins}. \tag{5}$$

The joule heat transmitting directly through the via $Q^*_{\rm via}$ is multiplied by 2, which is because the interconnects has two ends. Then we can obtain the heat generated by the i-th metal interconnect as[1]

$$\begin{aligned} p_{\rm g}(x) &= (J_{{\rm m},i}\cdot w_{{\rm m},i}\cdot t_{{\rm m},i})^2\cdot r(x)\\ &= (J_{{\rm m},i}\cdot w_{{\rm m},i}\cdot t_{{\rm m},i})^2\cdot\frac{\rho_{\rm m}\cdot L_i}{w_{{\rm m},i}}\\ &\quad\times t_{{\rm m},i}(1+\beta\cdot T_i(x)). \end{aligned} \tag{6}$$

On the other hand, the energy losses due to the heat transfer between the i-th metal and the $(i-1)$-th metal through the insulator are[1]

$$\begin{aligned} p_l(x) &= \frac{T_i(x)-T_{i-1}(x)}{R_{{\rm T},i}}\\ &= (T_i(x)-T_{i-1}(x))\cdot\frac{k^*_{{\rm ins,eff},i}w_{{\rm m},i}\cdot L_i}{h_i}, \end{aligned} \tag{7}$$

$$\begin{aligned} k^*_{{\rm ins,eff},i} &= k_{\rm ins}\cdot\frac{h_i}{w_{{\rm m},i}}\cdot 1.685\cdot\Big[\log\Big(1+\frac{h_i}{w_{{\rm m},i}}\Big)\Big]^{-0.59}\\ &\quad\times\Big(\frac{h_i}{t_{{\rm m},i}}\Big)^{-0.078}, \end{aligned} \tag{8}$$

where $R_{{\rm T},i}$ is the insulator thermal resistance and $k^*_{{\rm ins,eff},i}$ a kind of more accurate effective insulator thermal conductivity proposed by Andrews,[15] which is more accurate than the effective thermal conductivity of quasi-two-dimensional model in the deep submicron CMOS process.[1]

Therefore the net energy gain per unit volume of the i-th layer interconnect is

$$Q^*_i = \frac{p_{\rm g}(x)+\Delta Q_i - p_l(x)}{w_{{\rm m},i}\cdot t_{{\rm m},i}\cdot L_i}. \tag{9}$$

Thus the summarized stable interconnect heat flow equation can be written as[1]

$$\begin{aligned} \frac{{\rm d}^2T_i(x)}{{\rm d}x^2} &= -\frac{Q^*_i}{k_{\rm m}}\\ &= \frac{1}{L^2_{D,i}}(T_i(x)-T_{i-1}(x))\\ &\quad-\Big(\theta_i+\frac{\Delta Q_i}{k_{\rm m}w_{{\rm m},i}t_{{\rm m},i}L_i}\Big), \end{aligned} \tag{10}$$

where

$$\frac{1}{L^2_{D,i}} = \frac{1}{k_{\rm m}}\left(\frac{k^*_{{\rm ins,eff},i}}{t_{{\rm m},i}h_i} - J^2_{{\rm m},i}\rho_{\rm m}\beta\right),$$

and

$$\theta_i = \frac{J^2_{{\rm m},i}\rho_{\rm m}}{k_{\rm m}}.$$

In order to simplify the computation, assume that the temperature of the $(i-1)$-th interconnect is a constant ($T_{i-1}(x) = T_{{\rm avg},i-1}$), then solve Eq. (10), we can obtain the temperature profile and the average temperature of the i-th interconnect respectively as[1]

$$\begin{aligned} T_i(x) &= T_{{\rm avg},i-1} + L^2_{D,i}\cdot\Big(\theta_i+\frac{\Delta Q_i}{k_{\rm m}w_{{\rm m},i}t_{{\rm m},i}L_i}\Big)\\ &\quad\times\left(1-\frac{\sinh\frac{x}{L_{D,i}}+\sinh\frac{L_i-x}{L_{D,i}}}{\sinh\frac{L_i}{L_{D,i}}}\right), \end{aligned} \tag{11}$$

$$\begin{aligned} T_{{\rm avg},i} &= T_{{\rm avg},i-1} + L^2_{D,i}\cdot\Big(\theta_i+\frac{\Delta Q_i}{k_{\rm m}w_{{\rm m},i}t_{{\rm m},i}L_i}\Big)\\ &\quad\times\left(1-\frac{\tanh\frac{L_i}{2L_{D,i}}}{\frac{L_i}{2L_{D,i}}}\right). \end{aligned} \tag{12}$$

Assume that the lengths of layer interconnect are 10, 20, 40, 80, 200, 400, 800, 1000, 1500, and 2000 μm respectively and according to the data provided by ITRS2007,[14] the thermal conductivity of Cu ($K_{\rm m}$) is 386 W/(m·K), the thermal conductivity of insulator ($K_{\rm ins}$) is 0.12 W/(m·K), the temperature coefficient of Cu (β) is 4.3×10^{-3}/°C and the resistivity of metal is 2.2×10^{-8} Ω·m, assume that all the metals are electrified and each of all the metals achieves a limiting current density of 9.95×10^9 A/m^2, set a uniform substrate temperature at 105 °C, then we can obtain

Table 1. The interconnect parameters of 65 nm CMOS process.[10]

	Wire width $w_m/\mu m$	Wire thickness $t_m/\mu m$	Spacing $d/\mu m$	Insulator thickness $h/\mu m$	Relative ε
Local line M1∼M3	0.10	0.20	0.10	0.20	2.2
Intermediate line M4∼M6	0.14	0.35	0.14	0.20	2.2
Global line M7∼M10	0.45	1.20	0.45	0.20	2.2

the temperature profile of each layer through simulating the ten-layer interconnects based on the BPTM[16] 65-nm CMOS process of Table 1 with Eqs. (11) and (12), the temperature profile of M2, M5, M8 are shown in Fig. 3. The value of abscissa is normalized to the length of interconnect.

We can see from Fig. 3 that the temperature rise in higher layers is much obvious than in local interconnect lines. Figure 4 shows the relationship between the temperature of the global interconnects and the thermal conductivity of insulator. We can see that the temperatures of global interconnects vary abruptly with thermal conductivity of insulator, it is because heat cannot diffuse through insulator with a low conductivity, which results in tremendous temperature rise of global interconnects. So, the characteristics of global interconnect lines will be greatly influenced by the serious thermal problem such as crosstalk, which will be analysed in the next section.

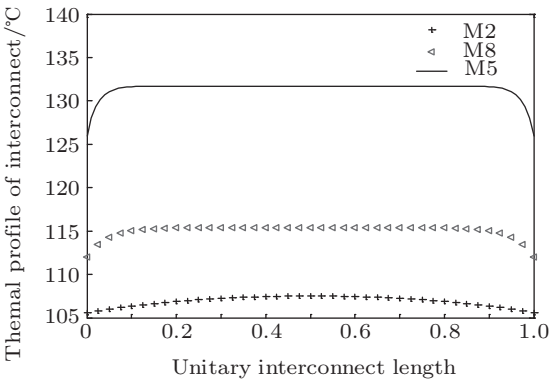


Fig. 3. Temperature profiles of the interconnects.

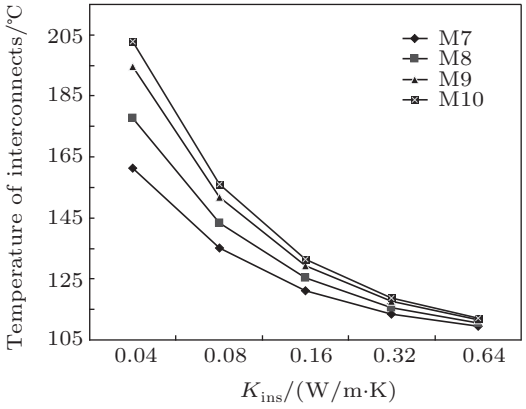


Fig. 4. Interconnect temperatures versus thermal conductivity of insulator.

3. RLC interconnect crosstalk model with considering thermal profile of multilevel interconnects

Figure 5 shows the section structure of interconnects, where l is the interconnect length, w the interconnect width, t the interconnect thickness, s the interconnect spacing and h the spacing between interconnect and ground.

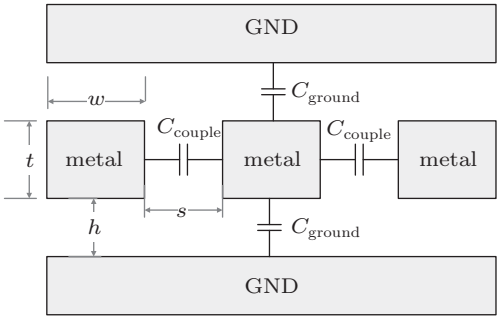


Fig. 5. Schematic illustration of interconnect section structure.

In the nanometer level CMOS process, the traditional aluminum interconnect is replaced by the copper interconnect, although the resistivity of the copper is low, aggressive temperature rise of the global interconnect (as shown in Fig. 3) makes the temperature distribution effect play an important role in the interconnect resistance. The interconnect resistance distribution is shown as follows:

$$R(x) = \rho_m \frac{l}{wt}(1 + \beta T(x)), \tag{13}$$

where $T(x)$ is the interconnect temperature profile.

The parasitic inductance and the parasitic capacitance are the primary parasitic parameters of the nanometer level CMOS process, which have tremendous influence on the transmission of high speed signal. In the new process of integrated circuits, the

change of interconnect structure (for example the reduction of interconnect width and interconnect spacing) causes the proportion of the coupling inductance and capacitance to increase continuously, thus making the coupling crosstalk noise increase.[7] For the interconnect structure as shown in Fig. 5, referring to the nanometer level CMOS parasitic capacitance and inductance extraction method of BPTM Wong model,[16] the self-inductance L and the mutual inductance M of unit length interconnect are shown respectively as follows:

$$L = \frac{\mu_0}{2\pi}\Big[\ln\Big(\frac{2l}{w+t}\Big) + \frac{1}{2} + \frac{0.22(w+t)}{l}\Big], \quad (14)$$

$$M = \frac{\mu_0}{2\pi}\Big[\ln\Big(\frac{2l}{w+s}\Big) - 1 + \frac{w+s}{l}\Big], \quad (15)$$

where the vacuum magnetic conductivity μ_0 is $4\pi \times 10^{-7}$ H/m.

For the interconnect structure shown in Fig. 5, the self-capacitance and the mutual capacitance of unit length interconnect are described respectively as follows:

$$C_{\rm g} = \varepsilon\Big[\frac{w}{h} + 2.04\Big(\frac{s}{s+0.54h}\Big)^{1.77} \times \Big(\frac{t}{t+4.53h}\Big)^{0.07}\Big], \quad (16)$$

$$C_{\rm c} = \varepsilon\Big[1.41\frac{t}{s}e^{-4s/(s+8.01h)} + 2.37\Big(\frac{w}{w+0.31s}\Big)^{0.28} \times \Big(\frac{h}{h+8.96s}\Big)^{0.76} \cdot e^{-2s/(s+6h)}\Big], \quad (17)$$

where ε is the dielectric coefficient of insulator.

For the distributed RLC coupling interconnect model as shown in Fig. 6, $\boldsymbol{R}_{\rm a}$, $\boldsymbol{R}_{\rm v}$, $\boldsymbol{L}_{\rm a}$, $\boldsymbol{L}_{\rm v}$, $\boldsymbol{C}_{\rm a}$, $\boldsymbol{C}_{\rm v}$ denote the resistor matrix, the inductance matrix and the capacitance matrix of the aggressor and victim respectively and $\boldsymbol{M}, \boldsymbol{C}_{\rm c}$ represent the interconnect mutual inductance matrix and the coupling capacitance matrix respectively. According to the equivalent Thevennin model, the aggressor driver can be modeled as a voltage source and connected in series with a resistance $R_{\rm th}$ and the victim driver is a pure resistance $R_{\rm d}$ and $C_{\rm f}$ is the load capacitance of the circuit.

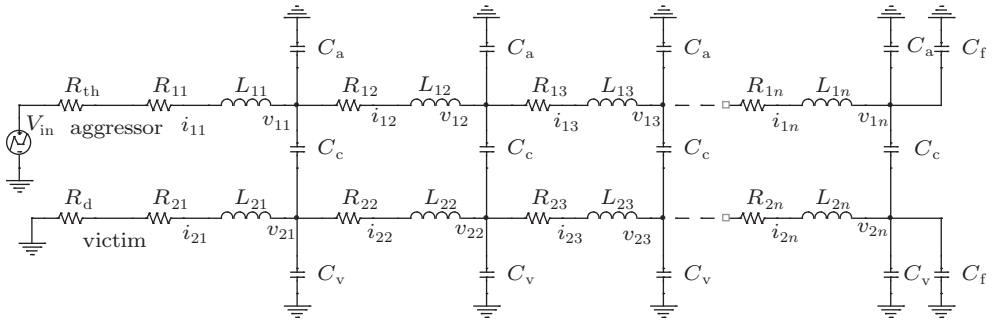


Fig. 6. Distributed RLC parallel interconnect model.

In order to make the model possess the characteristic close to the transmission, the number of RLC segments n is determined by the fastest change rate of the signal edge in simulation. Generally, the shortest delay ($T_{\rm D} = \sqrt{LC}$) of RLC segment less than one tenth of rise (fall) time can satisfy the requirement and n can be obtained by

$$n \geq 10\Big(\frac{x}{t_{\rm r} v}\Big), \quad (18)$$

where x is the length of the transmission line, v the propagation velocity of electromagnetic wave in medium and $t_{\rm r}$ the rise (fall) time. Based on the temperature profile shown in Fig. 3, the computation indicates that for the global interconnects and the intermediate interconnects, when $x = 3L_{\rm D}$, then $T \approx 0.9979T_{\max}$. Therefore, we may consider that at $x = 3L_{\rm D}$ the interconnect has achieved a maximum temperature.[4] So we can divide interconnect into two parts, one part is that the temperature is always constant and the other part is that the temperature is varying. Thus, we can define the number of the subsections of the varying-temperature-part as n^*, expressed below:

$$n^* = \left[\frac{6 \cdot L_{\rm D}}{l} \cdot n\right], \quad (19)$$

where n^* is an integer ($n^* \geq 1$) and $L_{\rm D}$ is the thermal diffusion length of the interconnect, while the number of the subsections of the constant-temperature-part is $(n - n^*)$. Thus the interconnect resistance can be revised into two parts, i.e., the variation-temperature-part,

$$R_1 = \rho_{\rm m}\frac{l}{wt}(1 + \beta T_{\rm avg}), \quad (20)$$

and the constant-temperature-part,

$$R_2 = \rho_{\rm m}\frac{l}{wt}\left(1+\beta T_{\max}\right), \tag{21}$$

where $T_{\rm avg}$ is the average temperature of an interconnect and $T_{\max}$ is the maximum temperature of an interconnect.

Using the Kirchhoff's current law (KCL) and the Kirchhoff's voltage law (KVL) to analyse each RLC subsection in Fig. 6, we can obtain the following matrix formula:[5,8]

$$\begin{bmatrix} \boldsymbol{C}_1 & -\boldsymbol{C}_{\rm c} & 0 & 0 \\ -\boldsymbol{C}_{\rm c} & \boldsymbol{C}_2 & 0 & 0 \\ 0 & 0 & \boldsymbol{L}_{\rm a} & -\boldsymbol{M} \\ 0 & 0 & -\boldsymbol{M} & \boldsymbol{L}_{\rm v} \end{bmatrix} \begin{bmatrix} \dfrac{{\rm d}\boldsymbol{v}_1}{{\rm d}t} \\ \dfrac{{\rm d}\boldsymbol{v}_2}{{\rm d}t} \\ \dfrac{{\rm d}\boldsymbol{i}_1}{{\rm d}t} \\ \dfrac{{\rm d}\boldsymbol{i}_2}{{\rm d}t} \end{bmatrix} = \begin{bmatrix} \boldsymbol{\alpha} & 0 & 0 & 0 \\ 0 & \boldsymbol{\alpha} & 0 & 0 \\ -\boldsymbol{R}_{\rm a} & 0 & \boldsymbol{\beta} & 0 \\ 0 & -\boldsymbol{R}_{\rm v} & 0 & \boldsymbol{\beta} \end{bmatrix} \begin{bmatrix} \boldsymbol{i}_1 \\ \boldsymbol{i}_2 \\ \boldsymbol{v}_1 \\ \boldsymbol{v}_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \boldsymbol{b} \\ 0 \end{bmatrix} \times V_{\rm in}, \tag{22}$$

where $\boldsymbol{C}_1$, $\boldsymbol{C}_2$, $\boldsymbol{C}_{\rm a}$, $\boldsymbol{C}_{\rm v}$, $\boldsymbol{C}_{\rm c}$, $\boldsymbol{L}_{\rm a}$, $\boldsymbol{L}_{\rm v}$, $\boldsymbol{M}$, $\boldsymbol{R}_{\rm a}$, and $\boldsymbol{R}_{\rm v}$ are diagonal matrixes ($n\times n$); $\boldsymbol{C}_1 = \boldsymbol{C}_{\rm a}+\boldsymbol{C}_{\rm c}$, $\boldsymbol{C}_2 = \boldsymbol{C}_{\rm v}+\boldsymbol{C}_{\rm c}$; $\boldsymbol{v}_1$, $\boldsymbol{i}_1$, $\boldsymbol{v}_2$ and $\boldsymbol{i}_2$ are the node voltage and current of the aggressor and victim respectively, which are matrixes $(n\times 1)$, $V_{\rm in}$ is an input to aggressor line. $\boldsymbol{\alpha}$ and $\boldsymbol{\beta}$ are diagonal matrixes $(n\times n)$ and $\boldsymbol{b}$ is a constant matrixes $(n\times 1)$

$$\boldsymbol{\alpha} = \begin{bmatrix} 1 & -1 & 0 & 0 & \cdots & 0 \\ 0 & 1 & -1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & -1 & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & -1 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}, \quad \boldsymbol{\beta} = \begin{bmatrix} -1 & 0 & 0 & 0 & \cdots & 0 \\ 1 & -1 & 0 & 0 & \cdots & 0 \\ 0 & 1 & -1 & 0 & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & 0 & 0 & 1 & -1 \end{bmatrix}, \quad \boldsymbol{b} = \begin{bmatrix} 1 \\ 0 \\ \vdots \\ 0 \\ 0 \end{bmatrix}.$$

By substituting the constant matrix into Eq. (22), we can obtain a voltage differential equation. Assuming that all the initial conditions are zero, invert the equation into a Laplace domain and change them, then we can obtain expressions as follows:

$$\begin{aligned}&(s^2A_{11}+sB_{11}-\beta)v_1(s)+(s^2A_{12}+sB_{12})v_2(s)\\&\quad = bv_{\rm in}(s),\end{aligned} \tag{23}$$

$$\begin{aligned}&(s^2A_{21}+sB_{21})v_1(s)+(s^2A_{22}+sB_{22}-\beta)v_2(s)\\&\quad = 0,\end{aligned} \tag{24}$$

where

$$\begin{aligned} A_{11} &= L_{\rm a}\alpha^{-1}C_1 - M\alpha^{-1}C_{\rm c},\\ A_{12} &= -L_{\rm a}\alpha^{-1}C_{\rm c} + M\alpha^{-1}C_2,\\ A_{21} &= M\alpha^{-1}C_1 - L_{\rm v}\alpha^{-1}C_{\rm c},\\ A_{22} &= -M\alpha^{-1}C_1 + L_{\rm v}\alpha^{-1}C_{\rm c},\\ B_{11} &= R_{\rm a}\alpha^{-1}C_1, \quad B_{12} = -R_{\rm a}\alpha^{-1}C_{\rm c},\\ B_{21} &= -R_{\rm v}\alpha^{-1}C_{\rm c}, \quad B_{22} = R_{\rm v}\alpha^{-1}C_2, \end{aligned}$$

with matrix $\boldsymbol{\alpha}^{-1}$ being the inverse matrix of matrix $\boldsymbol{\alpha}$.

Assume that the input to the aggressor is a saturated ramp signal of rise time $t_{\rm r}$ and given by

$$V_{\rm in} = \frac{V_{\rm DD}}{t_{\rm r}}[tU(t)-(t-t_{\rm r})U(t-t_{\rm r})],$$

where $U(t)$ represents the step signal, $V_{\rm DD}$ the amplitude of the voltage and $t_{\rm r}$ the rise (fall) time of the ramp input. It is easy to find that using the initial and the final value theorems of the Laplace domain, we can expand $v_1(s)$ and $v_2(s)$ into the following series:[5,8]

$$\begin{aligned}v_1(s) &= v_{10}s^{-1}+v_{11}+v_{12}s^{+}v_{13}s^2+\cdots\\&\quad +v_{1n}s^{n-1},\end{aligned} \tag{25}$$

$$\begin{aligned}v_2(s) &= v_{20}+v_{21}s+v_{22}s^2+v_{23}s^3+\cdots\\&\quad +v_{2n}s^{n}.\end{aligned} \tag{26}$$

By substituting Eqs. (25) and (26) into Eqs. (23) and (24) and using the coefficients of all s^i on the left-hand side which are the same as those on the right-hand side, we obtain v_{1i} values:

$$\begin{aligned} v_{10} &= -\beta^{-1}bv_{\rm DD}, \quad v_{11} = \beta^{-1}\Big[B_{11}v_{10}+\frac{t_{\rm r}v_{\rm DD}b}{2}\Big],\\ v_{12} &= \beta^{-1}\Big[A_{11}v_{10}+B_{11}v_{11}+B_{12}v_{20}-\frac{v_{\rm DD}bt_{\rm r}^2}{6}\Big],\\ v_{1i} &= \beta^{-1}\Big[A_{11}v_{1(i-2)}+B_{11}v_{1(i-1)}+A_{12}v_{2(i-3)}\\&\quad +B_{12}v_{2(i-2)}+(-1)^{(i+1)}\frac{v_{\rm DD}bt_{\rm r}^i}{(i+1)}\Big]. \end{aligned}$$

Similarly, the value of v_{2i} can be solved as follows:

$$v_{20} = \beta^{-1}B_{21}v_{10},$$

$$v_{21} = \beta^{-1}[A_{21}v_{10} + B_{21}v_{11} + B_{22}v_{20}],$$
$$v_{22} = \beta^{-1}[A_{21}v_{11} + B_{21}v_{12} + A_{22}v_{20} + B_{22}v_{21}],$$
$$v_{2i} = \beta^{-1}[A_{21}v_{1(i-1)} + B_{21}v_{1i} + A_{22}v_{2(i-2)} + B_{22}v_{2(i-1)}].$$

Using the initial and the final value theorems, for $t \to 0$, $v_2 \to 0$; for $t \to \infty$, $v_2 \to 0$. Thus the voltage of victim $v_{2n}(s)$ can be expressed as

$$v_{2n}(s) = \frac{a_0 + a_1 s + \cdots + a_{n-2}s^{n-2}}{1 + b_1 s + \cdots + b_{n-1}s^{n-1} + b_n s^n}. \quad (27)$$

In this paper, we use the second-order Pade' model which is stable and efficient in computation,[5] then $v_{2n}(s)$ is described as

$$v_{2n}(s) = \frac{a_0}{1 + b_1 s + b_2 s^2}, \quad (28)$$

where $a_0 = v_{20j}$,

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} v_{20j} & 0 \\ v_{21j} & v_{20j} \end{bmatrix}^{-1} \times \begin{bmatrix} -v_{21j} \\ -v_{22j} \end{bmatrix}$$

(j represent the j-th node on the interconnect). Thus we can obtain the time-domain response of victim:

$$v_2(t) = c_1 \cdot \mathrm{e}^{-t/k_1} + c_2 \cdot \mathrm{e}^{-t/k_2}, \quad (29)$$

where $1/k_1$ and $1/k_2$ are the poles of the crosstalk voltage function. Using MATLAB for the wave of $v_2(t)$, we can obtain the noise peak voltage v_{2_peak} and peak time t_{peak} with considering multilevel interconnect temperature distribution effect.

4. Model verification and discussion

In this paper, we focus on the crosstalk analysis of the parallel interconnects in the same layer based on the 65-nm CMOS process and the ramp input signal with rise (fall) time $t_r = 10$ ps and amplitude voltage 1.1 V. The source resistance is 192 Ω and the load capacitance is 52 fF. In this paper we focus only on the verification of and the discussion on the intermediate and the global interconnects in the same layer since both of the coupling effects between different layers and the temperature rise of local interconnect are rather small. The errors relative to the result of the Hspice simulation with considering temperature effect are shown in Table 2, showing that the analytical model proposed in this paper has a high accuracy within 6.5%.

Table 2. Crosstalk model verification based on 65-nm CMOS process.

Interconnects	Partition numbers (n)	v_{2_peak}/mV	Hspice/mV	Error	t_{peak}/ps
M4	20	30.1	29.9	0.669%	22.4
M5		63.8	60.1	6.16%	28.8
M6		102.3	95.7	6.45%	36.8
M7	30	111.9	112	−0.089%	40.1
M8		121.9	124	−1.69%	44.5
M9		136.8	140	−2.29%	54.3
M10		144.2	154	−6.36%	65.7

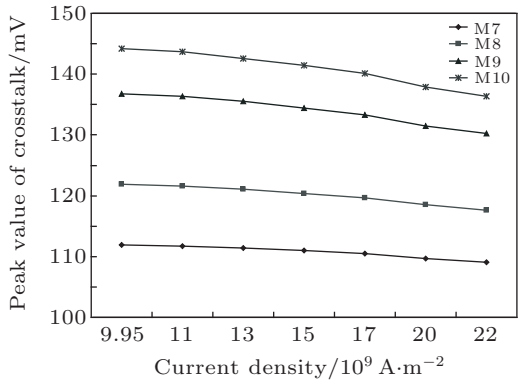


Fig. 7. Global interconnect RLC crosstalks versus current density.

Figure 7 shows the relationship between crosstalk of global interconnect and current density. The interconnect heat and the via self-heating effect become more serious with the increase of current density, which makes the resistance of interconnects increase, but on contrary, the crosstalk noise reduces, which shows that the RLC crosstalk peak value of interconnect decreases with the increase of interconnect temperature in nanometer level CMOS process.

Figure 8 shows the global interconnect crosstalks versus thermal conductivity of insulator, indicating that the crosstalk noise increases with the thermal conductivity of insulator increase. Because the increase of thermal conductivity of insulator makes the temperature of interconnects decrease, the resis-

tance interconnects decreases, which also shows that the RLC crosstalk noise of interconnect increases with the decrease of interconnect temperature in nanometer level CMOS process. So, nanometer level CMOS process encounters much more serious noise problem at low temperature than at high temperature.

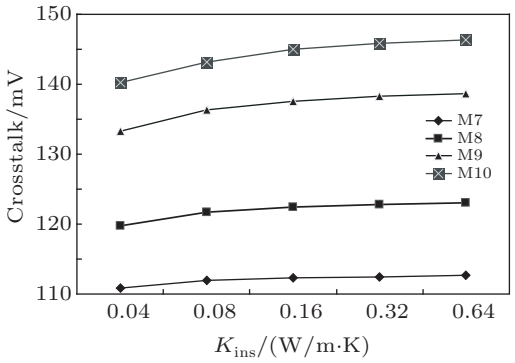


Fig. 8. Crosstalks versus thermal conductivity of insulator.

Figure 9 reveals the relationship between the RLC crosstalk peak value of the global interconnect and the dielectric thickness when the current density is 9.95×10^9 A/m^2. The dashed line shows the curve of crosstalk peak value of each global interconnect without considering the temperature effect and the real line shows the curve of crosstalk peak value of each global interconnect with considering the temperature effect. We can see that the crosstalks of all global interconnects increase with dielectric thickness increasing. The influence of the self-heating of the interconnects in lower layers (for example M7) on the crosstalk is small because of the low temperature rise of the interconnects. Therefore, the two curves are basically coincident with each other. When the thickness of the dielectric is small, the heat dispersion of the interconnect is quite good, so the via self-heating effect and the interconnect self-heating effect are not obvious and so the influence of the interconnect self-heating on the crosstalk is not obvious either. Therefore, curves are basically coincident with each other. When the thickness of the dielectric increases, the heat dispersion of the interconnect become bad, then the interconnect temperature distribution effect has a remarkable influence on the RLC crosstalk peak value. Meanwhile we can see from Fig. 9 that the change of the interconnect structure may have a tremendous influence on the RLC crosstalk peak value, and the interconnect crosstalk is obviously overestimated if the temperature effect is neglected. Therefore, it is necessary to analyse the influence of the temperature distribution effect of multilevel interconnect on the RLC crosstalk accurately.

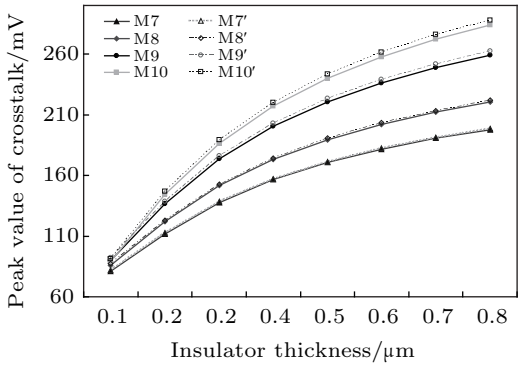


Fig. 9. Global interconnect RLC crosstalks versus dielectric thickness.

5. Conclusion

According to the actual multilevel interconnect thermal profile, in this paper we proposed a kind of new multilevel interconnect temperature distribution model and derived an analytical crosstalk model for the distributed RLC interconnect with considering the effect of thermal profile. According to the 65-nm CMOS process, we verified the proposed RLC analytical crosstalk model in different interconnect coupling conditions and the absolute error is within 6.5%. The analysis result indicates that the RLC crosstalk model in which the temperature effect is neglected will overestimate the interconnect crosstalk peak value obviously and in the model proposed in this paper the influence of the interconnect parameters on the crosstalk is taken into account, which is closer to the actual case, so it can be applied to the EDA design of nanometer level system chip and layout optimization.

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