Reconfigurable all-optical dual-directional half-subtractor for high-speed differential phase shift keying signal based on semiconductor optical amplifiers*

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All-optical digital logic elementary circuits are the building blocks of many important computational operations in future high-speed all-optical networks and computing systems. Multifunctional and reconfigurable logic units are essential in this respect. Employing the demodulation properties of delay interferometers for input differential phase shift keying signals and the gain saturation effect in two parallel semiconductor optical amplifiers, a novel design of 40 Gbit/s reconfigurable all-optical dual-directional half-subtractor is proposed and demonstrated. All output logic results show that the scheme achieves over 11=dB extinction ratio, clear and wide open eye diagram, as well as low polarization dependence (< 1 dB), without using any additional input light beam. The scheme may provide a promising candidate for future ultrafast all-optical signal processing applications.

Keywords: nonlinear optics, optical communications devices, semiconductor optical amplifier

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1. Introduction

All-optical digital logic elementary circuits are basic building blocks in all-optical signal processing for their extensive applications in high-speed all-optical networks and all-optical computing systems, such as all-optical address recognition, packet forwarding, packet checksum calculation, etc.[1−4] An all-optical half-subtractor is the key element of data processors performing binary subtraction, dual-directional binary counting, encryption, and decryption of secure network data, all-optical arithmetic-logic units (ALUs), etc. Therefore, various kinds of all-optical combinational logic circuits, such as encoder, half-subtractors have been studied recently.[5−8] By employing cross-gain modulation (XGM) in two semiconductor optical amplifiers (SOAs) and difference-frequency generation (DFG) with a periodically poled lithium niobate (PPLN) waveguide, all-optical digital half-subtraction and half-addition have been demonstrated at 5 Gbit/s.[5] In addition, an ultra-high-speed all-optical encoder and half-subtractor based on four-wave mixing (FWM) in a single SOA with polarization-shift-keying (PolSK) modulation signals has been proposed and numerically analysed.[6,7] However, the proposed logic circuits cannot be reconstructed in the previous SOA-based schemes.[5−7] Moreover, the input signals must be in the PolSK modulation format in Refs. [6] and [7]. Although a simple all-optical dual-directional half-subtractor scheme has been proposed and simulated by exploiting the sum-frequency generation (SFG) with a PPLN waveguide,[8] the conversion efficiency and the wavelength tuning range of the SFG with a PPLN waveguide scheme are very limited and requires a relatively high pump power as well, which is similar to the scheme of the FWM in the SOA.[6,7]

On the other hand, differential-phase-shift-keying (DPSK) format has achieved record capacities and distances in high-bit-rate long-haul optical transmission networks, as it can improve receiver sensitivity by a factor of 3-dB and it is also robust against fibre nonlinear effect.[9] Therefore, all-optical operation of PSK data, such as the logic operation of DPSK signals becomes an expected problem that needs solving.

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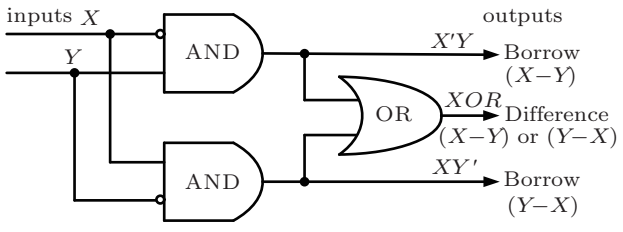
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In the past years, all-optical logic gates and circuits which perform complex logic functionalities were developed mainly for OOK signals.[5−8] For the DPSK signals, XOR gates have been reported based on the four-wave mixing (FWM) effect in semiconductor optical amplifiers (SOAs)[10,11] and highly nonlinear fibre (HNLF),[12] or cascaded SFG and DFG in PPLN waveguide.[13] To the best of our knowledge, the experimental demonstrations of high-speed SOA-based reconfigurable half-subtractor for input DPSK signals have not yet been reported.

In this paper, a novel reconfigurable all-optical dual-directional half-subtractor for 40-Gbit/s DPSK signals, is proposed and demonstrated using the demodulation properties of delay interferometers (DIs) for DPSK signals, as well as gain saturation effect in SOAs. The scheme has some advantages, such as simple structure, easy reconfigurability and adjustment, high operation speed, low power consumption, wide wavelength tuning range, great potential for hybrid or monolithic integration of SOAs and DIs,[14] etc.

2. Concept and principle

The half subtractor is a combinational logic unit performing subtraction of two binary data. The digital logic gate-level diagram and the logical truth table for a dual-directional half-subtractor are shown in Figs. 1(a) and 1(b), respectively. A dual-directional half-subtractor has two inputs X and Y, and three outputs $X'Y$, XOR, and XY', where $X'Y$, XOR, and XY' can be interpreted as the Borrow of (X–Y), the Difference (X–Y) or (Y–X), and the Borrow of (Y–X), respectively.



Input data		Output logic data		
X	Y	Difference XOR (X−Y) or (Y−X)	Borrow $X'Y$ (X−Y)	Borrow XY' (Y−X)
0	0	0	0	0
0	1	1	1	0
1	0	1	0	1
1	1	0	0	0

Fig. 1. Dual-directional half-subtractor: (a) digital logic gate-level diagram, (b) logical truth table.

Figure 2 shows schematic of the proposed all-optical dual-directional half-subtractor based on the DI and the XGM in two parallel SOAs. The two variables X and Y, as well as their complements X' and Y', are generated by demodulating two input DPSK signals with independent data using one or two DIs. In the sense of obtaining the inverted logic signals, DIs can be viewed as implementing NOT operations. Data X or Y can be recovered at constructive output port of the DI for a special wavelength, while the complement X' or Y' can also be obtained at destructive output port of the DI as shown in Fig. 2(a). In general, the complementary data are not always directly available, but can be derived from inverting the input data using NOT operation in all-optical logic circuits. Thanks to the usage of DPSK signals, the complementary data are obtained conveniently in this simple method which in turn makes the proposed scheme more flexible and reconfigurable.

Considering the two possible output states of the DI for each input carrier wavelength, the output possible data combinations of the DI are therefore four cases, namely (X, Y), (X', Y'), (X', Y), and (X, Y'). For example, X and Y are coupled and fed into the first SOA (SOA_1) simultaneously. Assuming that X serves as a pump and Y as a probe, the pump power is at least 10-dB higher than that of the probe. When the pump power is absent, the probe light will obtain high gain and be amplified in the SOA and the output signal is at a high level. However, when the pump power is present, the probe will obtain less gain because of the gain saturation effect, and the output signal is at a low level. Therefore, logic $X'Y$ can be extracted by a tunable bandpass filter (i.e., $TOBF_1$) centred on λ_Y at the output location SO_1, which is the Borrow of (X–Y). Similarly, when X and Y are coupled and injected into the second SOA (SOA_2), data Y acts as a pump light and X as a probe, logic XY' can be isolated out by another filter ($TOBF_2$) centred on λ_X at the output location SO_2, which corresponds to the Borrow of (Y–X). Subsequently, by coupling $X'Y$ and XY' with a passive optical coupler (OC), logic XOR is acquired at the output location SO_3, corresponding to the difference (X–Y) or (Y–X). Note that the OC could function as an OR gate just because the probability of concurrence of bit "1" in the data streams $X'Y$ and XY' is zero, according to the properties of the logic minterms.

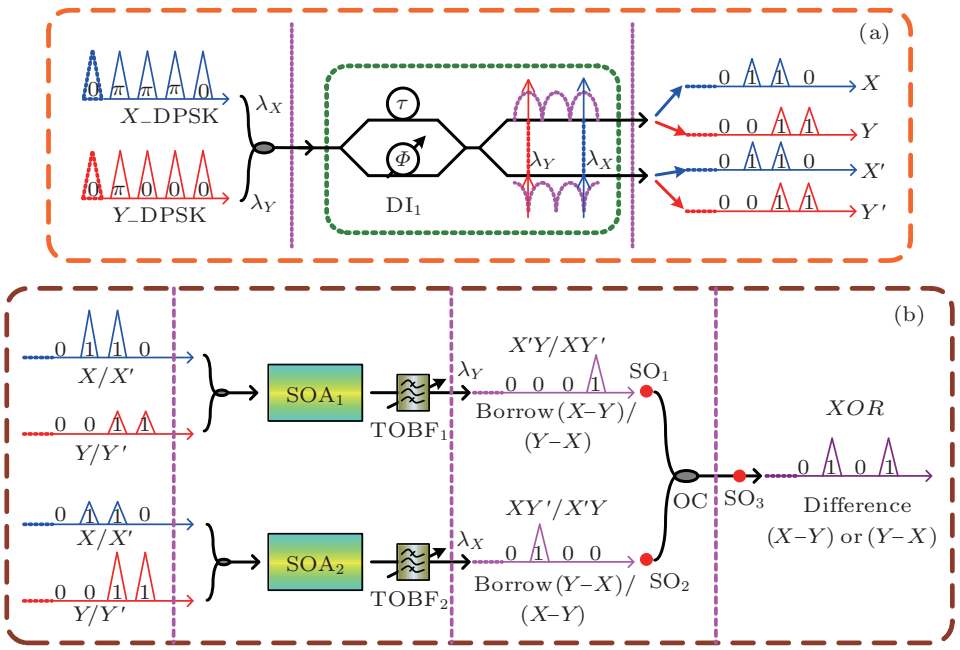


Fig. 2. (colour online) Schematic diagram of the proposed all-optical dual-directional half-subtractor based on the DI and the SOAs: (a) logic functions of the DI, (b) logic functions of two parallel arranged SOAs cascaded TOBFs.

Similarly, when the input data combination is (X', Y') rather than (X, Y), the complementary data are coupled together and injected into SOAs, only by tuning the phase shift of the DI, without changing any physical connection in Fig. 2, logic XY' and $X'Y$ can be extracted by the TOBF$_1$ centred on λ_Y and TOBF$_2$ centred on λ_X at SO$_1$ and SO$_2$, corresponding to the Borrow of $(Y–X)$ and the Borrow of $(X–Y)$, respectively. Note that the output logic data XY' and $X'Y$ can be reconfigured by tuning the phase shift of the DI at the same output location (SO$_1$ or SO$_2$), which indicate the Borrow of $(X–Y)$ and the Borrow of $(Y–X)$ can be interchanged in the same module as shown in Fig. 2(b). Although the Difference $(X–Y)$ or $(Y–X)$ remains constant when the output data combination of the DI is (X, Y) and (X', Y'), the two cases correspond to two different all-optical half-subtraction operations. This reconfigurability is very important for the real systems whose physical connection is fixed. This flexible half-subtractor has not yet been reported in any literature. Finally, XOR operation is derived by coupling the output data XY' and $X'Y$ with the OC, which is the Difference $(X–Y)$ or $(Y–X)$. It can be seen that the complementary data X' and Y' are artfully derived by demodulating DPSK signals, which further gives rise to the flexibility and reconfigurability of the proposed scheme. By the way, it should be noted that NOR, AND and XNOR operation can be derived by using this method, when the input data combination of SOAs is (X', Y) or (X, Y'). Switchable XOR/XNOR, simultaneous NOR and AND operations can be realized in our scheme.

3. Experimental demonstration and discussion

Figure 3 shows the experimental setup of the proposed scheme. Two continuous-wave (CW) beams are generated by two tunable lasers (λ_X = 1559.5 nm and λ_Y = 1553.1 nm) and modulated simultaneously by cascading two Mach–Zehnder modulators (MZMs), which generate 40-Gbit/s return-to-zero (RZ)-DPSK data streams each with a duty cycle of 0.33, with a 16-bit fixed pattern provided by a bit pattern generator (BPG) as shown by the first row in Fig. 4. A single DI is used to demodulate two input DPSK signals simultaneously by adjusting two input wavelengths. In a practical system where input wavelength cannot be adjusted, a separate DI is needed for each input DPSK signal, tuning the phase shift of the DI may be the only choice. The phase controller of the used DI is electrically tunable. The free spectrum range (FSR) of the DI is 0.32 nm, which is suitable for 40-Gbit/s DPSK demodulation as confirmed in Fig. 5. The output port of DI is set to be the constructive port for both λ_X and

λ_Y by adjusting input wavelengths, which is confirmed by S_1 in Fig. 5. Data streams of λ_X and λ_Y are separated by a wavelength division multiplexer (WDM) and amplified by erbium doped fiber amplifiers (EDFAs). Then the signals of λ_Y are relatively delayed several bits by optical delay lines (ODLs). Therefore, different absolute data X and Y are acquired at the input of the SOAs. Similarly, the complementary data X' and Y' can be obtained as well. As a reference, the various demodulated data streams are separately measured. Temporal waveforms and eye diagrams of the modulated signals (X, Y, X', and Y') are shown in Fig. 4. The used SOAs (CIP, NL-SOA) are both biased at 240 mA, where the 10%∼90% saturated gain recovery time is around 45 ps. Two Gaussian TOBFs each with a 3-dB bandwidth of 0.8 nm are used to extract the converted signals. Four variable optical attenuators (VOAs) are used to control the pump and probe powers at the input of the SOAs respectively. To facilitate description, important measuring points, such as SO_1, SO_2, and SO_3, are marked in Fig. 3. When the outputs of the DI are data combination (X, Y), X and Y are coupled together and fed into the SOA_1, where X serves as a pump light and Y as a probe. By tuning the input powers, logic $X'Y$ is extracted by $TOBF_1$ centred on 1552.7 nm at SO_1. The measured average power of pump/probe is 8.86/−4.56 dBm. Similarly, X and Y are injected into the SOA_2, where data Y acts as a pump and X as a probe. When average power of pump/probe is 8.72/−4.64 dBm, logic XY' is extracted by $TOBF_2$ centred on 1559.1 nm at SO_2. Note that the central wavelength of the TOBF is slightly tuned to the blue side of the probe light (around 0.4 nm), in order to mitigate the pattern effects due to the slow carrier recovery time of the SOAs.[15,16] The total insertion losses of the blue-shifting $TOBF_1$ and $TOBF_2$ are around 7 dB. The output powers of two converted signals (i.e., $X'Y$ and XY') from the $TOBF_1$ and $TOBF_2$ are −8.98 dBm and −8.79 dBm, respectively. Two converted signals are then amplified by EDFAs respectively and combined by a passive optical coupler (OC) to obtain logic XOR at SO_3. Finally, the optical spectra, temporal waveforms of the output logic signals are measured by employing an optical spectrum analyzer (OSA) and a digital communication analyzer (DCA), respectively. The Borrow of (X–Y), the Difference (X–Y) or (Y–X) and the Borrow of (Y–X) are thus obtained in our experiment. The temporal waveforms and eye diagrams of the output logic results are shown in Fig. 4.

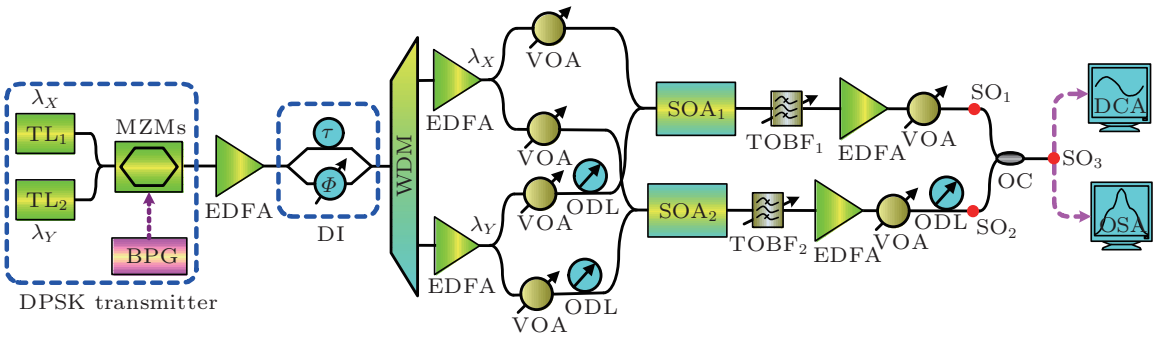


Fig. 3. (colour online) Experimental setup of the proposed scheme.

In this experiment, logic XY' of λ_Y and $X'Y$ of λ_X can also be derived at SO_1 and SO_2 respectively, when the data combination (X', Y') is injected into SOAs, only by tuning the phase shift of the DI with π, or adjusting input wavelengths to set the output of the DI to be the destructive port for both λ_X and λ_Y, without changing any physical connections in Fig. 3, which is confirmed by S_2 in Fig. 5. Therefore, the Borrow of (X–Y) and the Borrow of (Y–X) can be reconfigured at SO_1 and SO_2 by tuning either the phase shift of the DI or input wavelength, which makes the scheme more flexible and multi-functional. To evaluate the logic output performances, the extinction ratios (ERs) and eye opening factors (EOFs) of various logic results are all measured using 2^{31}–1 pseudo random bit sequence (PRBS) instead of the 16-bit fixed pattern. ERs and EOFs of the output logic $X'Y$, XY', and XOR are shown in Fig. 6. Degradation of output logic XY' is caused mainly by the wavelength up-conversion, while the degradation of XOR operation

comes mainly from the additional noises for combining X'Y and XY'.

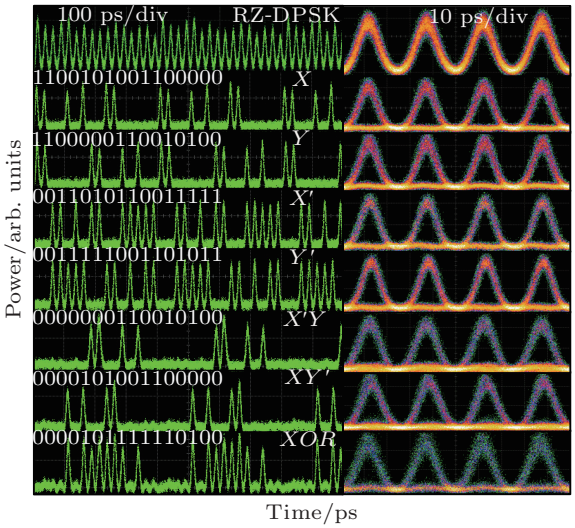


Fig. 4. (colour online) Temporal waveforms (left) and eye diagrams (right) of the demodulated signals (X, Y, X', and Y') and the output logic signals ($X'Y$ (Borrow of (X–Y)), XY' (Borrow of (Y–X)), and XOR (Difference of (X–Y) or (Y–X))).

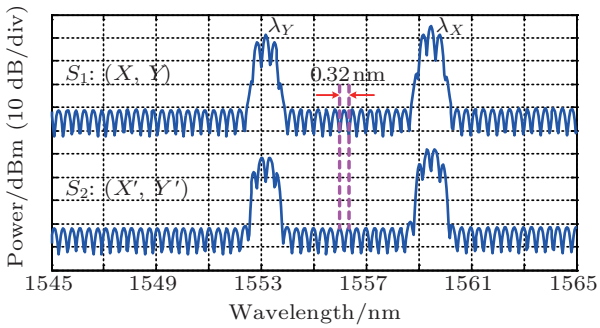


Fig. 5. (colour online) Measured output optical spectra of the DI (S_1: (X, Y), S_2: (X', Y')).

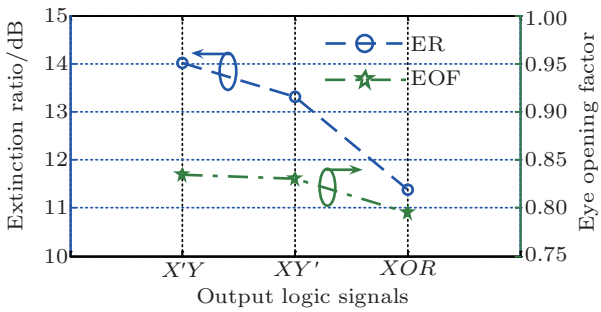


Fig. 6. (colour online) Measured extinction ratios (left) and eye opening factors (right) of the output logic signals (X'Y (Borrow of (X–Y)), XY' (Borrow of (Y–X)), and XOR (Difference of (X–Y) or (Y–X))).

In the experiment, some issues on the operating conditions and the output performances should be addressed. The difference in power between the input pump and the probe light needs to be optimized. The difference in optimum power between the two incoming signals at the input of the SOA is about 12 dB–14 dB. Non-optimum power difference may lead to operating performance degradations in two aspects. On the one hand, if the power difference is less than the optimum value, ghost pulses would become obvious in the output signal in the case that each of two input signals is logic "1". This is because there is not enough pump power to suppress the probe light in this case. On the other hand, however, further the power difference increasing to a value above the optimum value would lead to a serious degradation of the output signal quality due to significant pattern effects. In addition, the speed limit of SOA-based photonic switches is determined by the carrier dynamics of the SOA. Considering the benefits of quantum dot (QD)-SOA, such as ultrafast response time of gain saturation and negligible pattern effect,[17] the photonic logic gate based on QD-SOA is a promising candidate in ultrafast photonic data processing.[18,19]

We also investigated the polarization dependences of all the logic operations. When the polarization states of the input signals are adjusted using polarization controllers, the powers of output logic signals almost keep constant, indicating that all the logic operations are low polarization-dependent (< 1 dB).

4. Conclusions

A design of all-optical dual-directional half-subtractor is demonstrated at 40 Gbit/s, using the demodulation properties of the DI for input DPSK signals and the gain saturation effect in the SOA. All logic results with high ERs, clear open eyes and low polarization dependences are obtained without using any additional input beams. Reconfigurations of the scheme are realized by tuning either the phase shift of the DI or input wavelengths. Moreover, the great potential for hybrid or monolithic integration of DIs and SOAs may make the proposed scheme a promising candidate for future ultrafast all-optical signal processing applications.

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