Analysis on electrical characteristics of high-voltage GaN-based light-emitting diodes*

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(Received 30 March 2012; revised manuscript received 9 May 2012)

In order to investigate their electrical characteristics, high-voltage light-emitting-diodes (HV-LEDs) each containing four cells in series are fabricated. The electrical parameters including varying voltage and parasitic effect are studied. It is shown that the ideality factors (IFs) of the HV-LEDs with different numbers of cells are 1.6, 3.4, 4.7, and 6.4. IF increases linearly with the number of cells increasing. Moreover, the performance of the HV-LED with failure cells is examined. The analysis indicates that the failure cell has a parallel resistance which induces the leakage of the failure cell. The series resistance of the failure cell is 76.8 Ω, while that of the normal cell is 21.3 Ω. The scanning electron microscope (SEM) image indicates that different metal layers do not contact well. It is hard to deposit the metal layers in the deep isolation trenches. The fabrication process of HV-LEDs needs to be optimized.

Keywords: high-voltage light-emitting diode, electrical characteristics, ideality factor, series resistance

PACS: 72.80.Ey, 73.40.Cg, 73.61.Ey, 73.40.Kp **DOI:** 10.1088/1674-1056/21/12/127201

1. Introduction

Light-emitting diodes (LEDs) for lighting application are widely adopted for economic, energy, and environmental reasons.[1] As the "star" of the solid-state lighting industry, a lot of research on electrical and optical characteristics of the GaN LEDs is in active progress.[2,3] Nowadays, the concept of microchips employed in direct-current LEDs (DC-LEDs) is still promising. These series-connected microchips in one large chip would withstand very high forward voltage under dc operation.[4] Compared with normal LEDs, high-voltage LEDs (HV-LED) have some attractive advantages. The high-voltage and low-current operation is safer and more efficient for indoor power transformers. Due to its small chip size, the HV-LED can provide more flexible space for the driver and heat sink. Meanwhile, the numbers of solder joints and components are reduced. As a result, the reliability of LEDs is improved.

The characteristics of HV-LEDs have not been studied much, such as the ideality factor and the non-ideal characteristics. In this paper, we try to explain the electrical characteristics of the high-voltage LED and to analyse the origins of these phenomena.

2. Experiment results and discussion

The epitaxial LED wafer was grown on a sapphire substrate using a metal–organic chemical vapour deposition (MOCVD) system. It included an undoped GaN buffer layer, an Si-doped n-GaN layer, InGaN/GaN multiple quantum wells, an Mg-doped p-AlGaN electron blocking layer, and an Mg-doped p-GaN layer. For the fabrication of a high-voltage LED, the 4.5-μm-deep isolation trenches between cells were defined by an inductively coupled plasma (ICP) etching system. If the LED is fabricated on a patterned substrate, the trenches should be as deep as 5.5 μm for isolating. A 450-nm-thick SiO_2 film was deposited to prevent short circuiting between cells using a plasma enhanced chemical vapour deposition (PECVD) system. Then, the indium tin oxide (ITO) layer was deposited on the p-GaN as the transparent contact layer. After the thermal annealing of the ITO layer, the connecting metal bridges were deposited by magnetic sputtering. In this experiment, the HV-LED fabricated contained four cells in series.

*Project supported by the National Natural Science Foundation of China (Grant No. 11002013201102) and the National Key Technology R & D Program of China (Grant No. 2011BAE01B14).

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We use the Shockley equation to describe the I–V characteristics of LEDs, i.e.,

$$I = I_{\rm s} \exp(qv/n_{\rm ideal}KT), \tag{1}$$

where $I_{\rm s}$ is the reverse saturation current, q is the elementary charge, K is the Bolzmann constant, and $n_{\rm ideal}$ is the ideality factor.[5] A real diode has unwanted parasitic resistances, and the Shockley equation needs to be modified in order to take into account parasitic resistances. The I–V characteristics of a real diode are given by

$$I - \frac{(V - IR_{\rm s})}{R_{\rm p}} = I_{\rm s}\, {\rm e}^{e(V-IR_{\rm s})/(n_{\rm ideal}KT)}, \tag{2}$$

where $R_{\rm p}$ is the parallel resistance, and $R_{\rm s}$ is the series resistance. On the assumption that these resistors were large, Shah *et al.*[6] proposed that the GaN p–n junction diode can be modeled by a series of diodes, the actual p–n junction diode, unipolar heterojunction diodes, and a Schottky diode at the metal/p-type GaN junction. The I–V characteristics of the structure are given by

$$\ln I = \frac{(q/KT)}{\sum_i n_i} V + \frac{\sum_i n_i \ln I_{si}}{\sum_i n_i}. \tag{3}$$

Figure 1(a) is a theoretical curve obtained from Eq. (2).[7] The forward hump is caused by the parallel resistance, and it has the same level as the reverse saturation current. The second hump is caused by the series resistance. The electrical characteristics of the HV-LED measured at room temperature by Keithley 4200 are shown in Fig. 1(b). $R_{\rm s}$ has a relatively high value and leads to the hump at high voltage in $\ln I$–V curve, and the same conclusion can be drawn from the I–V curve. What is more, the inset in Fig. 1(b) shows the HV-LED tested by the prober.

If we only consider the linear region of the $\ln I$–V curve, the second term on the right-hand side of Eq. (3) will be a constant. Then equation (3) can be written as

$$\ln I = a + bV, \tag{4}$$

where $a = \sum_i n_i \ln I_{si} / \sum_i n_i$, and $b = (q/KT)/\sum_i n_i$. Therefore, the ideality factor can be estimated by the slope of the $\ln I$–V curve, namely $n = \sum_i n_i = (q/KT)/b$. Figure 2 shows how to extract the ideality factor from Fig. 1(b). In order to avoid the influence of parasitic resistance, the region near the origin is chosen. As shown, while the $\ln I$–V curve obeys the linear law, the I–V curve conforms to the exponential law. After the linear fitting, the slope of Fig. 3 is 6.003, and apparently the ideality factor of this HV-LED is 6.4.

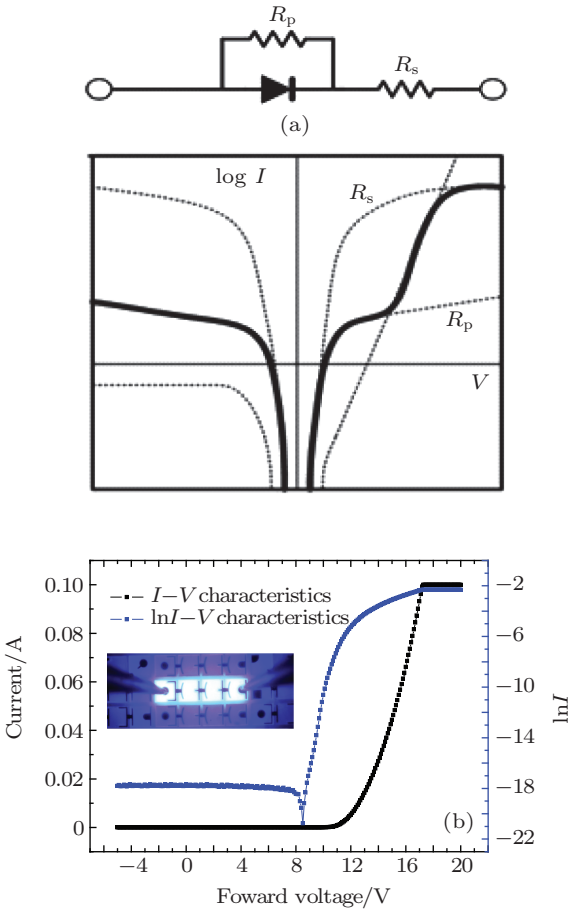


Fig. 1. (colour online) (a) I–V curve of parasitic resistance model, and (b) I–V and $\ln I$–V curve of HV LED.

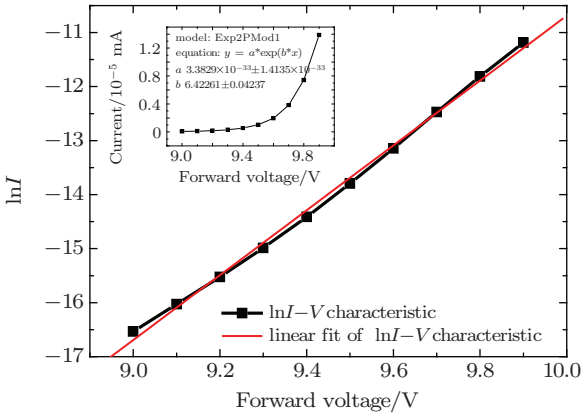


Fig. 2. (colour online) Linear fitting of the $\ln I$–V curve, and the inset shows the I–V relation in the same region.

Figure 3 shows the I–V characteristics of different cells. After the fitting process, the ideality factors are 1.6, 3.1, and 4.7 respectively. It means that the ideality factors increase linearly with the increase of the cells in series. According to the theory of Sah–Noyce–Shockley,[8] the ideality factors between 1 and

2 are caused by the recombination of carriers in the space charge region, mediated by recombination centres located near the intrinsic Fermi level.

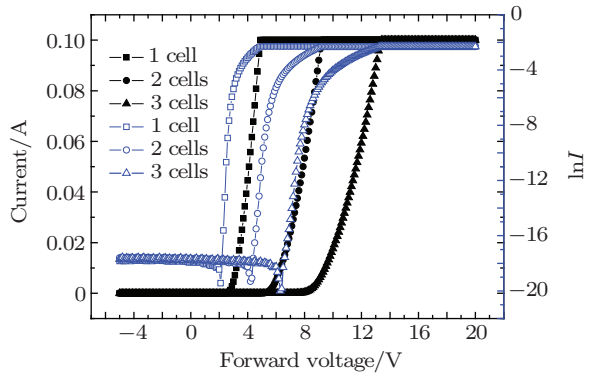
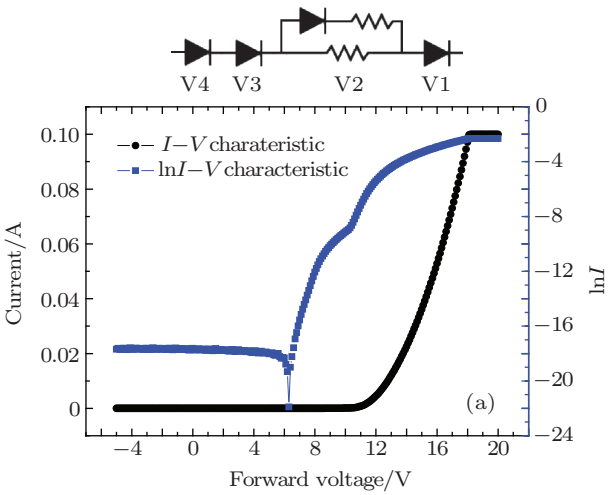


Fig. 3. (colour online) I–V characteristics of different cells of the HV-LED.



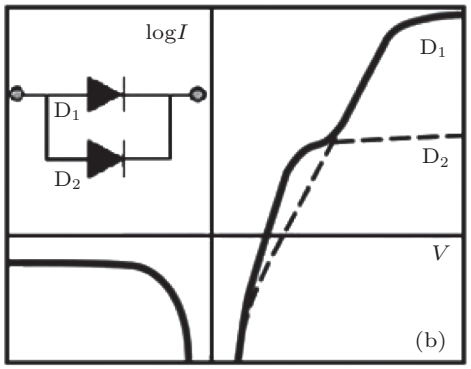


Fig. 4. (colour online) Electrical characteristics of (a) HV-LED with failure cells and (b) ideal LED with parallel diode.

As shown in Fig. 4(a), the electrical characteristics of some HV-LEDs are abnormal. In fact, the HV-LED performs like this because it had one cell delayed to turn on. Figure 4(b) illustrates the I–V characteristics of an ideal LED with a parasitic diode.[5] Obviously, the failure cell has a parallel resistance, which leads to a leakage pathway in the LED structure. The circuit in Fig. 4(a) shows the equivalent circuit of the abnormal HV-LED. Only when the value of V_2 increases to a threshold, will the failure cell be turned on.

In order to prove this theory, the I–V characteristics of the failure cell are tested in Fig. 5. Under a reverse biasing of 5 V, the leakage current is 7.6 mA while that of the normal cell is 18 nA. According to Li *et al.*,[9] the lattice damage could be caused by ICP etching process. During the fabrication of HV-LED, deep isolation trenches are etched, which surely causes dangling bonds on the side walls of the LED. These dangling bonds could absorb impurities and turn into defect states. Finally, the leakage pathways are formed. The deposition of the SiO_2 can alleviate the leakage, but there are pinholes or defects in the SiO_2 layer. To solve this problem, the deposition parameters should be optimized and a passivation layer can be used to improve the electrical characteristics of the LED.

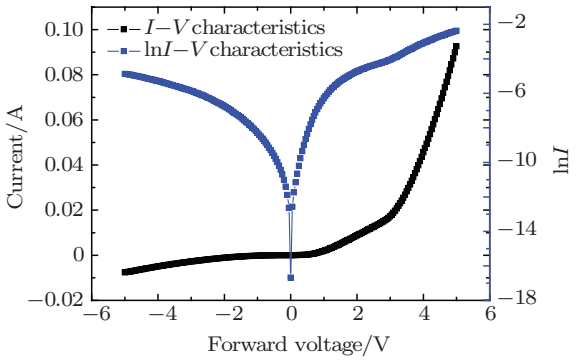


Fig. 5. (colour online) Electrical characteristics of the failure cell of the abnormal HV-LED.

In Fig. 5, it can be clearly concluded that the failure cell has a series resistance, which induces the high turn-on voltage. In order to analyse the high turn-on voltage, figure 6 shows the plots of the relation between $I(\mathrm{d}V/\mathrm{d}I)$ and I. Series resistance is one of the factors describing how the Ohmic contact affects the forward electrical characteristics of LEDs.[10] The series resistance can be obtained using an equation derived from Eq. (2), as

$$I\left(\frac{\mathrm{d}V}{\mathrm{d}I}\right) = IR_{\mathrm{s}} + \frac{n_{\mathrm{ideal}}KT}{q}. \tag{5}$$

We can obtain R_{s} from the slope of the curve in Fig. 6. After the fitting process, the R_{s} (slope) of the normal cell is obtained to be 21.3 Ω, while that of the failure cell is 76.8 Ω. The high series resistance cell is examined by scanning electron microscope (SEM), and figure 7 shows the structure of

the trench. The different metal layers do not contact closely, and even the outer metal layer does not contact the others. In addition, the metal on the side wall is thinner than in other places. This phenomenon may originate from the growth process of the metal layers. In fact, the isolation trenches are so deep that it is hard to deposit metal materials in the corners. The bad contact affects the electrical characteristics and the reliability of the HV-LED. For the industrialization of HV-LEDs, a new structure of the epitaxial layer or a new metal growing method should be developed to meet the requirements of the fabrication process. Moreover, the annealing of the ITO layer can reduce the series resistance of the HV-LED.[11]

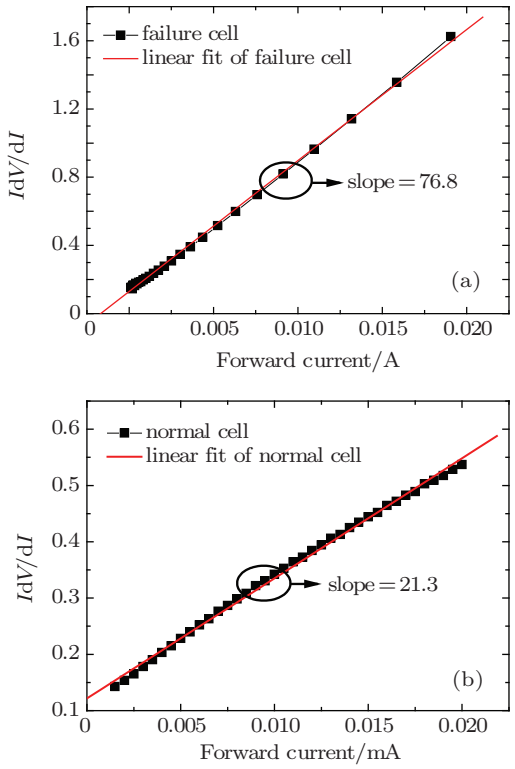


Fig. 6. (colour online) linear fittings of (a) failure cell and (b) normal cell.

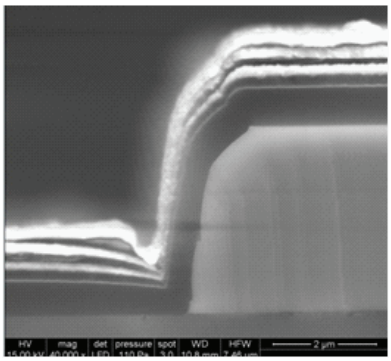


Fig. 7. SEM image of the metal layers in the trench.

3. Conclusion

In this work, we fabricated the HV-LEDs, and studied their electrical characteristics. The ideality factors are extracted from the ln I–V curves, and the ideality factors increase linearly with the number of cells. Moreover, we investigated the electrical characteristics of a HV-LED with a failure cell. The failure cell has a higher turn-on voltage and leakage current under reverse bias. Under a reverse biasing of 5 V, the leakage current is 7.6 mA while that of the normal cell is 18 nA. After analysis, the ICP etching process can induce the leakage current, and the failure cell has a larger series resistance than the normal cell. The large series resistance of the failure cell could be reduced through optimizing the parameters of the metal deposition process and the ITO annealing. The analysis of electrical characteristics is helpful for improving the fabrication maturity and the performance of HV-LEDs.

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