Wet thermal annealing effect on $TaN/HfO_2/Ge$ metal–oxide–semiconductor capacitors with and without a GeO_2 passivation layer*

Liu Guan-Zhou(刘冠洲), Li Cheng(李 成)†, Lu Chang-Bao(路长宝), Tang Rui-Fan(唐锐钒), Tang Meng-Rao(汤梦饶), Wu Zheng(吴 政), Yang Xu(杨 旭), Huang Wei(黄 巍), Lai Hong-Kai(赖虹凯), and Chen Song-Yan(陈松岩)

Department of Physics, Semiconductor Photonics Research Center, Xiamen University, Xiamen 361005, *China*

(Received 11 May 2012; revised manuscript received 13 July 2012)

Wet thermal annealing effects on the properties of $TaN/HfO_2/Ge$ metal–oxide–semiconductor (MOS) structures with and without a GeO_2 passivation layer are investigated. The physical and the electrical properties are characterized by X-ray photoemission spectroscopy, high-resolution transmission electron microscopy, capacitance–voltage (C–V) and current–voltage characteristics. It is demonstrated that wet thermal annealing at relatively higher temperature such as 550 °C can lead to Ge incorporation in HfO_2 and the partial crystallization of HfO_2, which should be responsible for the serious degradation of the electrical characteristics of the $TaN/HfO_2/Ge$ MOS capacitors. However, wet thermal annealing at 400 °C can decrease the GeO_x interlayer thickness at the HfO_2/Ge interface, resulting in a significant reduction of the interface states and a smaller effective oxide thickness, along with the introduction of a positive charge in the dielectrics due to the hydrolyzable property of GeO_x in the wet ambient. The pre-growth of a thin GeO_2 passivation layer can effectively suppress the interface states and improve the C–V characteristics for the as-prepared HfO_2 gated Ge MOS capacitors, but it also dissembles the benefits of wet thermal annealing to a certain extent.

Keywords: HfO_2 dielectric on germanium, X-ray photoemission spectroscopy, wet thermal annealing, metal–oxide–semiconductor capacitor

PACS: 77.55.dj, 79.60.Bm, 73.40.Qv **DOI:** 10.1088/1674-1056/21/11/117701

1. Introduction

Germanium (Ge) has attracted much attention as one of the promising channel materials for the scaling metal–oxide–semiconductor field effect transistor (MOSFET) because of its higher electron and hole mobilities than those of silicon.[1] The great progress made on the alternative high-k materials paves the way to overcome the vulnerability of germanium without stable natural oxides. Among the high-k dielectrics, HfO_2 on germanium is widely investigated using different deposition methods, such as atomic layer deposition (ALD), metal organic chemical vapor deposition (MOCVD), and magnetron sputtering.[2–4] However, the instability of the high-k/Ge interface is found to be one of the main obstacles to realize the high performance germanium MOSFET. Many efforts have been made to reduce the interface states, such as nitrification, passivation by Si or S, and building a stack structure with rare earth oxides.[5–9] First-principle simulations predicted that Ge–O and Hf–O–Ge bonds present at/near Ge/GeO_2 or Ge/HfO_2 interface did not produce any defect levels in the Ge band gap, but the formation of Ge–Hf bonds at the interface, likely present if Hf was located in the incompletely oxidized GeO_x transition layer, was predicted to result in the formation of a defect level in the upper part of the Ge energy band gap.[10] Thermal annealing in wet ambient was proposed to be able to greatly suppress the growth of unstable low-k GeO_x ($x < 2$) at the dielectric/Ge interface, thus resulting in a smaller effective oxide thickness, as well as fewer interface states and less of a dielectric charge.[11–13] On the other hand, the passivation of Ge surface for high-k dielectrics using GeO_2 was under extensive investi-

*Project supported by the National Natural Science Foundation of China (Grant Nos. 61176092, 61036003, and 60837001), the National Basic Research Program of China (Grant No. 2012CB933503), the Ph.D. Program Foundation of Ministry of Education of China (Grant No. 20110121110025), and the Fundamental Research Funds for the Central Universities, China (Grant No. 2010121056).

†Corresponding author. E-mail: lich@xmu.edu.cn

© 2012 Chinese Physical Society and IOP Publishing Ltd

gation recently.[14−16] With a GeO_2 passivation layer grown by high-pressure oxidation, high performance Ge n-MOSFET has been achieved with a peak electron mobility of 1500 $cm^2/V{\cdot}s$.[17] These results issue an interesting question that whether the two methods could be combined to achieve a lower interface state density for Ge MOS structures. Furthermore, the thermal stability of the GeO_2 passivation layer and the influence of the Ge incorporation in the HfO_2 dielectric during wet thermal annealing on the electrical characteristics of the Ge MOS structures also need to be further clarified.[18]

In this work, the physical and electrical properties of TaN/HfO_2/Ge MOS structures with and without a GeO_2 passivation layer annealed in water vapor are investigated. The Ge incorporation in the HfO_2 dielectric and the modification of the HfO_2/Ge interface are characterized by X-ray photoemission spectroscopy (XPS), high-resolution transmission electron microscopy (HRTEM), capacitance–voltage (C–V) and current–voltage (I–V) characteristics. Possible reasons for the modification of the interface and its influence on the electrical characteristics are discussed.

2. Experimental procedures

The key steps used in the fabrication of TaN/HfO_2/Ge MOS structures with and without a GeO_2 passivation layer, are shown in Fig. 1. The MOS capacitors were made on Sb-doped n-type Ge (100) wafers with resistivity of 0.02 $\Omega{\cdot}$cm. N-type Ge substrates were circularly degreased in an ultrasonic bath of acetone and ethanol, immersed in a hydrochloric acid solution (HCl:H_2O=1:1) and a hydrofluoric acid solution (HF:H_2O=1:50) to remove the native oxide, rinsed with deionized water, and blown dry with nitrogen. Some of the samples were then oxidized at 400 °C for 9 min in dry oxygen to form a 4 nm GeO_2 layer. Parts of the samples with the GeO_2 layer were annealed in wet N_2 ambient at 400 °C for 4 min (sample series A). The wet N_2 atmosphere was obtained by bubbling pure N_2 through de-ionized water at 95 °C with a flow rate of 1 L/min. The other samples with the GeO_2 layer were labelled as sample series B. The samples without the GeO_2 layer were labelled as sample series C. All of the samples were then transferred to the chamber of an electron beam evaporation system with a base pressure of 3.6×10^{-6} Torr for the deposition of HfO_2 thin films. The substrate temperature was kept at 200 °C during the deposition, and the depositing rate of HfO_2 was about 1.5 Å/s. The thickness of HfO_2 of the samples was about 20 nm. After that, sample series B and C were annealed in wet N_2 ambient for various durations at 400–550 °C respectively. The chemical compositions and the states of elements were analyzed by XPS with a 1486.6 eV Al $K\alpha$ source. The XPS analysis was performed with all peaks referring to the C 1s peak at the binding energy of 284.8 eV. Sputtering and patterning of 20 nm TaN/300 nm Au on HfO_2 were performed to fabricate MOS structures for the electrical characteristics measurements. The backside Ohmic contacts were formed by Au sputtering. Capacitance–voltage characteristics were measured in the parallel mode with a Keithley 4200 semiconductor characterization system and a Keithley 590 C–V analyzer to characterize the electrical properties and the interface qualities of the MOS capacitors.

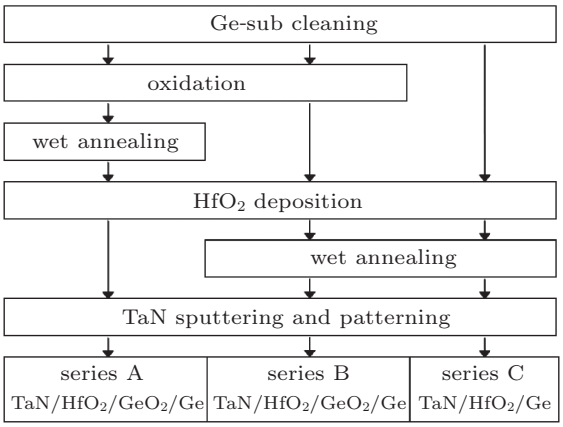


Fig. 1. Key steps used in the fabrication of TaN/HfO_2/Ge MOS structures with and without a GeO_2 passivation layer.

3. Results and discussion

Figure 2 shows the XPS depth profile of 6 nm HfO_2 dielectric on a Ge substrate, the sputter etching depth is 1.6 nm for each level. The sample only presents two peaks at 17.1 eV and 18.6 eV before the sputter etching, corresponding to Hf $4f_{7/2}$ and Hf $4f_{5/2}$ peaks from HfO_2. When the sputter etching depth reaches 3.2 nm, the Ge 2p3 region shows the presence of the Ge–Ge peak from the Ge substrate, suggesting that the XPS information from the interface of HfO_2/Ge is detected. In the meantime, another Hf $4f_{7/2}$ peak appears at 14.1 eV, which is thought to be from the Hf–Ge bonds at the HfO_2/Ge interface. The existence of a GeO_x interlayer between HfO_2 and

Ge leads to the formation of a Hf germanide (Hf–Ge) layer, which introduces a large number of interface states because the defect level of the Hf–Ge bonds lies in the Ge energy band gap.[10]

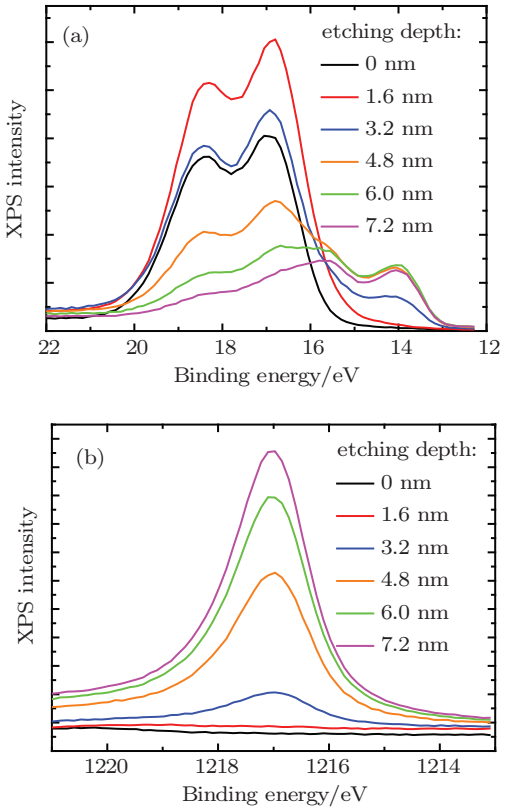


Fig. 2. (colour online) (a) Hf 4f and (b) Ge 2p3 XPS depth profiles of 6 nm HfO_2 dielectric on Ge substrate, the sputter etching depth is 1.6 nm for each level.

The physical properties of the HfO_2 thin films directly grown on the Ge substrates before and after wet thermal annealing were characterized by XPS. Figure 3 shows the Hf 4f, Ge $2p_{3/2}$, O 1s XPS spectra of the HfO_2 dielectric on the Ge substrate before and after wet thermal annealing at 550 °C for 2–10 min. In Figs. 3(a) and 3(c), the Hf $4f_{7/2}$ peak at 17.1 eV and the O 1s peak at 530.2 eV from the as-deposited sample respectively shift to 17.3 eV and 530.5 eV after thermal annealing, suggesting the formation of germanate of hafnium ($HfGeO_x$) during the wet thermal annealing process.[18] In Figs. 3(b) and 3(c), we can see that the Ge $2p_{3/2}$ and the O 1s peaks from GeO_x are detected and the peak intensities increase with the increasing annealing time, showing that considerable Ge is incorporated in the HfO_2 thin film. These results demonstrate that wet thermal annealing of HfO_2/Ge can lead to the formation of $HfGeO_x$ and the Ge diffusion into HfO_2. The chemical state of Ge in HfO_2 tends to transform from GeO_x to GeO_2 with the increase of the annealing time. In addition, the intensity of Hf 4f peak decreases with the increasing annealing time, which even disappears for the sample annealed for 10 min. It can be explained by the GeO_x coverage on HfO_2 due to the evaporation and redeposition of the uncovered back-side of Ge during wet thermal annealing, as reported in our previous work.[18] Figure 4 shows a typical high resolution transmission electron microscopy image of the HfO_2/Ge structure after wet thermal annealing at 550 °C. A very thin GeO_x interlayer between HfO_2 and Ge and the partial crystallization of HfO_2 thin films are observed, which are usually thought to introduce interface states and increase the leakage current of the MOS capacitor.

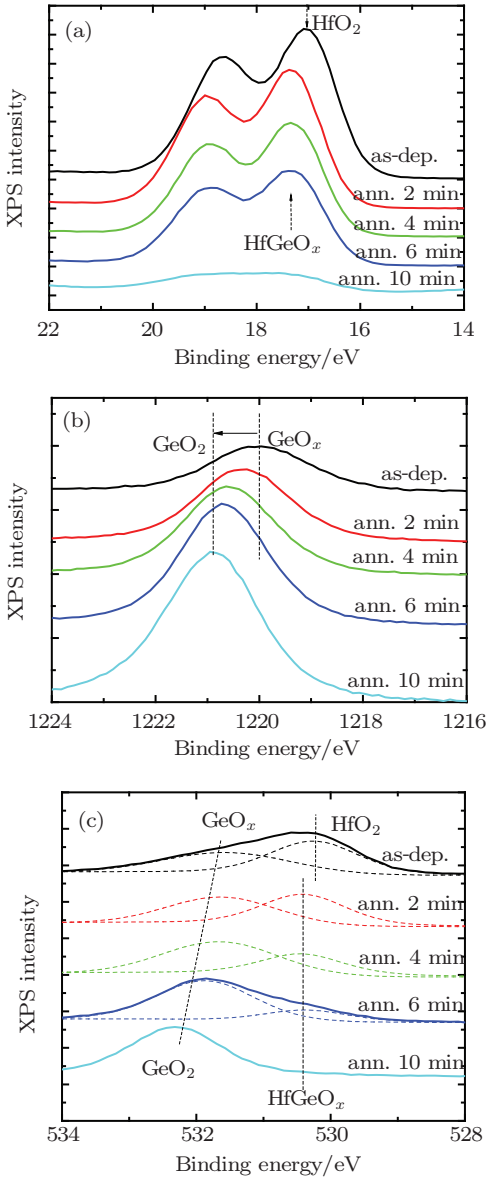


Fig. 3. (colour online) (a) Hf 4f, (b) Ge $2p_{3/2}$, and (c) O 1s XPS spectra of HfO_2 dielectric on Ge substrate before and after wet thermal annealing for various durations.

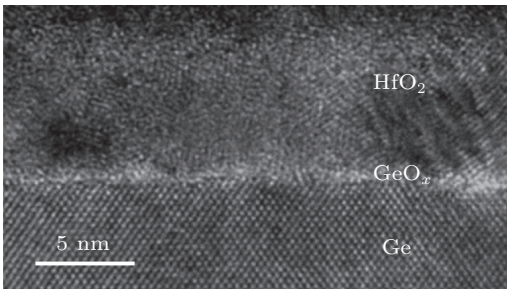


Fig. 4. A typical HRTEM image of the HfO_2/Ge structure after wet thermal annealing at 550 °C for 2 min.

The C–V characteristics of the TaN/HfO_2/Ge structures measured at 1 MHz before and after wet thermal annealing at 550 °C for various durations are shown in Fig. 5. The accumulation capacitance of the sample after thermal annealing for 2 min becomes slightly larger than that of the as-deposited one, while those of the samples after thermal annealing for 4 min and 6 min decrease with the increasing annealing time. Obvious stretch-outs are observed in the C–V curves for the samples thermal annealed for 4 min and 6 min. This result implies that the effective oxide thickness (EOT) becomes smaller for the sample annealed for 2 min due to the reduction of the GeO_x interlayer, as reported in Refs. [12] and [19]. However, the EOT increases when the wet thermal annealing precedes over 2 min. It is reasonable to suppose that another mechanism, rather than the reductioon of the interlayer, may dominate the process, which is believed to be the Ge incorporation including the subsequent reaction with HfO_2 according to the XPS results. With an increasing wet thermal annealing time, more Ge incorporation reduces the oxide permittivity and degrades the C–V characteristics seriously.

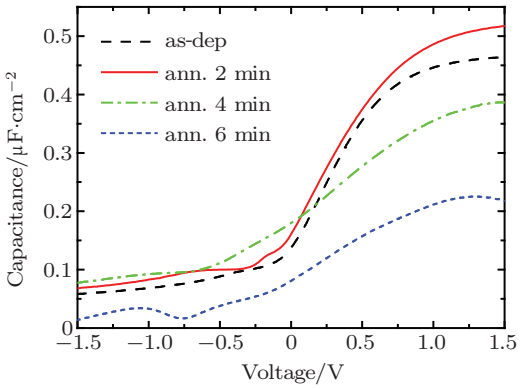


Fig. 5. (colour online) Capacitance-voltage characteristics of TaN/HfO_2/Ge structures before and after wet thermal annealing at 550 °C for various durations.

To investigate the temperature dependence of the Ge incorporation in wet thermal annealing, Hf 4f and Ge $2p_{3/2}$ XPS spectra of the HfO_2/Ge samples after wet thermal annealing at 400 °C, 450 °C, 500 °C, and 550 °C for 5 min are plotted in Fig. 6. The Ge $2p_{3/2}$ peak of the sample annealed at 550 °C shifts to a high binding energy compared to those of the samples annealed at 400–500 °C, indicating the presence of more Ge^{4+} chemical states (GeO_2). The Ge $2p_{3/2}$ peak intensity of the sample annealed at 550 °C is much higher, and the Hf 4f peak intensity becomes lower than those of the samples annealed at 400–500 °C. These results indicate that wet thermal annealing at 550 °C causes much more Ge incorporation in HfO_2, which can be attributed to the formation and desorption of Ge monoxide from the backside of the Ge wafer at a relatively higher temperature.[20] Therefore, the appropriate temperature of wet thermal annealing should be below 500 °C.

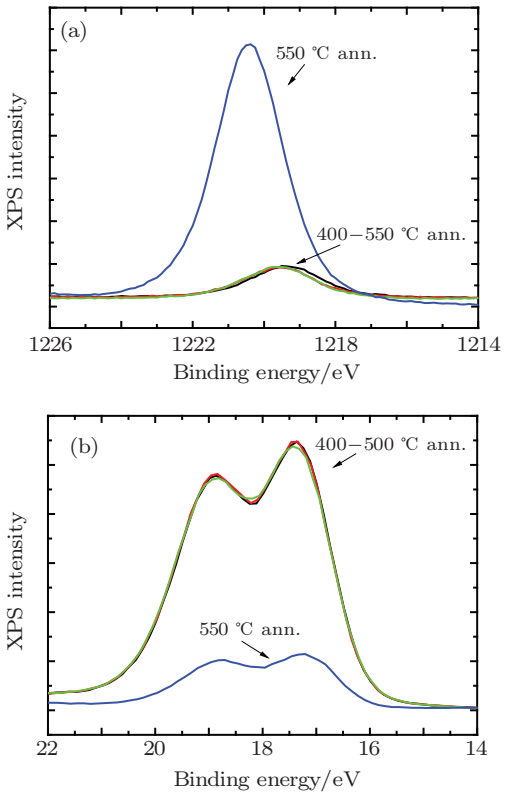


Fig. 6. (colour online) (a) Ge $2p_{3/2}$ and (b) Hf 4f XPS spectra of HfO_2 dielectrics on Ge substrates after wet thermal annealing for 5min at 400 °C, 450 °C, 500 °C, and 550 °C.

Wet thermal annealing at 400 °C was carried out to investigate its effect on TaN/HfO_2/Ge MOS structures with and without a GeO_2 passivation layer to alleviate or avoid the effect of Ge incorporation in HfO_2. XPS was applied for the GeO_2/Ge structures before and after wet thermal annealing at 400 °C for 4 min. The Ge 3d spectra of the samples are shown

in Fig. 7(a). The Ge 3d XPS peak related to GeO_x lies at 32.8 eV (a value which is close to 33.2 eV for Ge 3d from GeO_2) regardless of the sample annealing, suggesting that the process has a slight influence on the GeO_x oxidation degree. The integrated intensity ratio of the Ge 3d peak from GeO_x to Ge substrate significantly decreases after wet thermal annealing, suggesting that the GeO_x thickness decreases during the process. The C–V characteristics of the samples from series A corresponding to the XPS data are shown in Fig. 7(b). The accumulation capacitance of the sample after wet thermal annealing becomes larger than that of the as-deposited sample, and the C–V curve becomes sharp, implying a lower interface state density. The mid-gap interface state density of the TaN/HfO_2/GeO_2/Ge capacitor is calculated with the Terman method[21] from the measured C–V curve at 1 MHz and a theoretical C–V curve obtained by a C–V simulator.[22] The mid-gap interface state density decreases from 3.3×10^{12} $cm^{-2}\cdot V^{-1}$ to 8.7×10^{11} $cm^{-2}\cdot V^{-1}$ for the sample after wet thermal annealing, confirming that the wet thermal annealing process is able to suppress the interface states by reducing the thickness of the GeO_x interlayer.

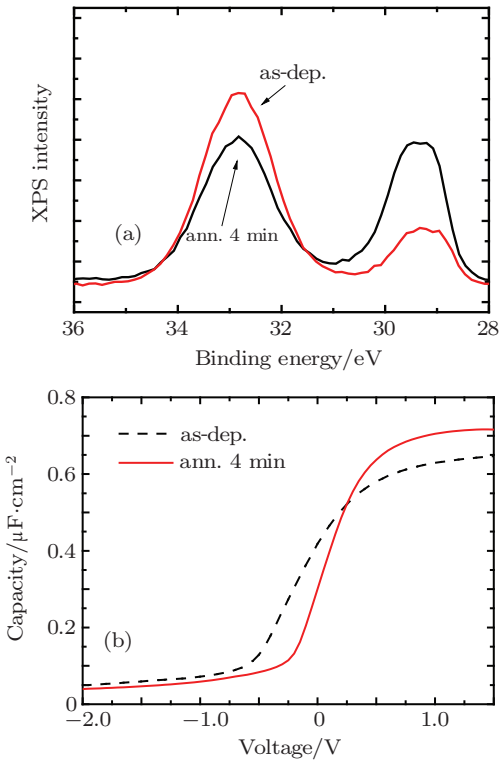


Fig. 7. (colour online) (a) Ge 3d XPS spectra of GeO_2/Ge structure before and after wet thermal annealing. (b) Capacitance–voltage characteristics of sample series A.

The C–V characteristics of the samples from series B and C before and after wet thermal annealing at 400 °C for 4–10 min are shown in Fig. 8. The accumulation capacitance increases with the increasing wet thermal annealing time due to the reduction of the GeO_x interlayer thickness. The flat band voltage shifts in the negative voltage direction after wet thermal annealing. We notice that the flat band voltage has no obvious change for the samples of HfO_2/GeO_2/Ge MOS capacitors with wet thermal annealing being carried out for GeO_2/Ge before the deposition of HfO_2, as shown in Fig. 7(b). The results demonstrate that the Ge diffusion into HfO_2 during wet thermal annealing can introduce a positive charge in the dielectrics.

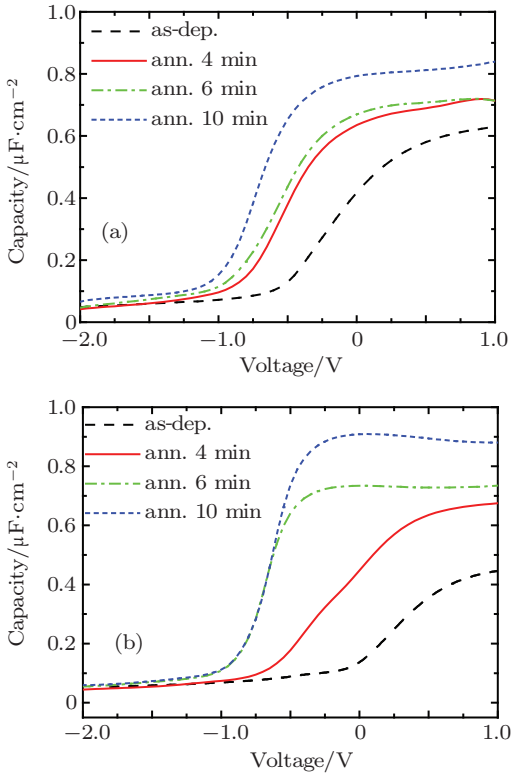


Fig. 8. (colour online) Capacitance–voltage characteristics of sample series (a) B and (b) C before and after wet thermal annealing for various durations.

As shown in Fig. 9, the mid-gap interface state densities are significantly suppressed for all of the samples after wet thermal annealing at 400 °C, which keep decreasing with the increasing wet thermal annealing time. The as-deposited sample with the GeO_2 passivation layer has a lower mid-gap interface state density than that without the GeO_2 passivation layer, because the quality of the pre-grown GeO_2 passivation layer is thought to be better than the GeO_x interlayer formed during the HfO_2 deposition process. However, the lowest interface state density of 4.6×10^{11} $cm^{-2}\cdot V^{-1}$ is achieved for the TaN/HfO_2/Ge sample after wet

thermal annealing for 10 min without the GeO_2 passivation layer. It is shown that the interface states of the samples without the GeO_2 passivation layer are greatly suppressed by wet thermal annealing. In comparison, the improvement of the sample with the GeO_2 passivation layer is not obvious.

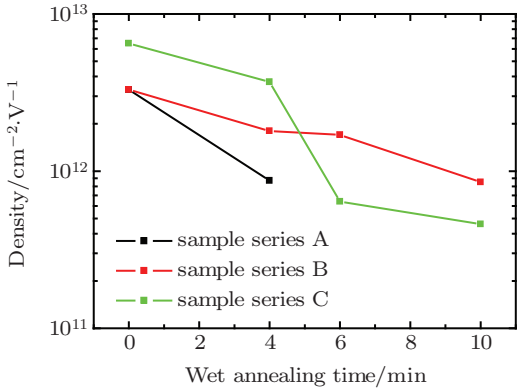


Fig. 9. (colour online) Dependences of mid-gap interface state densities of sample series A, B, and C on the wet thermal annealing time.

Figure 10 shows the current–voltage characteristics of TaN/HfO_2/Ge and TaN/HfO_2/GeO_2/Ge capacitors before and after wet annealing at 400 °C for 4 min. The leakage current density has similar trends with the interface state density dependence on the wet annealing time. The pre-growth of the GeO_2 passivation layer can reduce the leakage current density effectively for the as-deposited samples. However, after wet thermal annealing, the reduction of the leakage current density of the samples without the GeO_2 passivation layer is more obvious. The lowest leakage current density of 4.9×10^{-6} A/cm^2 at -1 V is achieved for the TaN/HfO_2/Ge sample without the GeO_2 passivation layer after wet thermal annealing.

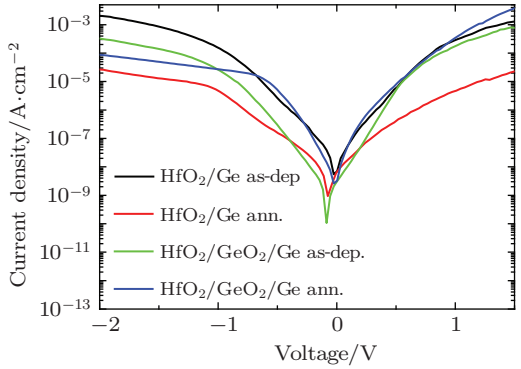


Fig. 10. (colour online) Current–voltage characteristics of TaN/HfO_2/Ge and TaN/HfO_2/GeO_2/Ge capacitors before and after wet annealing at 400 °C for 4 min.

The electrical characteristics of the TaN/HfO_2/Ge capacitors strongly depend on the physical properties of the HfO_2/Ge interface. The formation of an incompletely oxidized GeO_x interlayer can introduce interface states between HfO_2 and Ge. When the sample is annealed at 400 °C in wet ambient, the GeO_x interlayer is greatly reduced, which should be responsible for the lower interface state density and the larger accumulation capacitance of the wet annealed sample. However, for the sample annealed at 550 °C, the interface state density increases and the accumulation capacitance decreases with the increasing annealing time. The degradation of the electrical characteristics of the TaN/HfO_2/Ge MOS structures after wet thermal annealing at 550 °C can be attributed to the Ge incorporation in HfO_2 due to Ge diffusion, Ge monoxide desorption from the uncovered back-side of the Ge wafer, and the redeposition during the thermal annealing processes. The pre-growth of a thin GeO_2 passivation layer before the deposition of the HfO_2 dielectric can reduce the interface states and improve the C–V characteristics of the MOS capacitors without thermal treatments, but after wet thermal annealing, the C–V characteristics for the samples without the GeO_2 passivation layer become even better with lower interface state densities. We infer that the different changes of the C–V characteristics of series B and C derive from that the passivation method with a GeO_2 passivation layer suppresses the interface states by increasing the oxidation degree of the GeO_x interlayer, while wet thermal annealing takes effect by reducing the GeO_x interlayer thickness but not increasing the oxidation degree of GeO_x. Both methods achieve improved results compared to the as-deposited sample, but there is an inherent contradiction when combining them.

4. Summary

We have investigated the effects of wet thermal treatments on the physical and electrical properties of TaN/HfO_2/Ge MOS structures with and without a GeO_2 passivation layer. Wet thermal annealing at 550 °C gives rise to the Ge incorporation in HfO_2, which stretches out the C–V curves and degrades the electrical properties of the capacitors. However, the wet thermal annealing process at optimized 400 °C would lead to a smaller effective oxide thickness and a lower interface state density by reducing the unstable GeO_x interlayer thickness at the HfO_2/Ge interface. A positive charge can be introduced in the dielectrics

during the thermal treatments. The wet thermal annealing process can effectively suppress the interface states of $TaN/HfO_2/Ge$ MOS structures, but the pregrowth of a GeO_2 passivation layer dissembles its benefits to a certain extent.

References

[1] Claeys C and Simoen E 2007 *Germanium Based Technologies*: em From Materials to Devices (New York: Elsevier)

[2] Spiga S, Wiemer C, Tallarida G, Scarel G, Ferrari S, Seguini G and Fanciulli M 2005 *Appl. Phys. Lett.* **87** 112904

[3] Wu N, Zhang Q C, Chan D S H, Balasubramanian N and Zhu C X 2006 *IEEE Transact. Electron. Dev. Lett.* **27** 479

[4] He G, Fang Q, Li G H, Zhang J P and Zhang L D 2007 *Appl. Surf. Sci.* **253** 8483

[5] Wu N, Zhang Q C, Zhu C X, Yeo C C, Whang S J, Chan D S H, Li M F, Cho B J, Chin A, Kwong D L, Du A Y, Tung C H and Balasubramanian N 2004 *Appl. Phys. Lett.* **84** 3741

[6] Xu J P, Chen W B, Lai P T, Li Y P and Chan C L 2007 *Chin. Phys.* **16** 529

[7] Xie R L, Phung T H, Yu M B and Zhu C X 2010 *IEEE Transact. Electron. Dev.* **57** 1399

[8] Xie R L and Zhu C X 2007 *IEEE Transact. Electron. Dev. Lett.* **28** 976

[9] Ahmet P, Nakagawa K, Kakushima K, Nohira H, Tsutsui K, Sugii N, Hattori T and Iwai H 2008 *Microelectron. Reliab.* **48** 1769

[10] Houssa M, Pourtois G, Caymax M, Meuris M and Heyns M 2008 *Surf. Rev. Lett.* **602** L25

[11] Xu J P, Lai P T, Li C X, Zou X and Chan C L 2006 *IEEE Transact. Electron. Dev. Lett.* **27** 439

[12] Zou X, Xu J P, Li C X and Lai P T 2007 *Appl. Phys. Lett.* **90** 163502

[13] Park I, Choi Y, Nichols W T and Ahn J 2011 *Appl. Phys. Lett.* **98** 102905

[14] Delabie A, Bellenger F, Houssa M, Conard T, Elshocht S V, Caymax M, Heyns M and Meuris M 2007 *Appl. Phys. Lett.* **91** 082904

[15] Afanas'ev V V, Stesmans A, Delabie A, Bellenger F, Houssa M and Meuris M 2008 *Appl. Phys. Lett.* **92** 022109

[16] Oniki Y, Koumo H, Iwazaki Y and Ueno T 2010 *J. Appl. Phys.* **107** 124113

[17] Nishimura T, Lee C H, Wang S K, Tabata T, Kita K, Nagashio K and Toriumi A 2010 *VLSI Symp. Tech. Dig.* 209

[18] Liu G Z, Li C, Lai H and Chen S Y 2010 *J. Electrochem. Soc.* **157** H603

[19] Kim H, McIntyre P C, Chui C O, Saraswat K C and Cho M H 2004 *Appl. Phys. Lett.* **85** 2902

[20] Zhang Q C, Wu N, Lai D M Y, Nikolai Y, Bera L K and Zhu C X 2006 *J. Electrochem. Soc.* **153** G207

[21] Terman L M 1962 *Solid-State Electron.* **5** 285

[22] Berkeley Device Group Available: www-device.eecs.berkeley.edu/qmcv/qmcv.htm