Three-dimensional Monte Carlo simulation of bulk fin field effect transistor*

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In this paper, we investigate the performance of the bulk fin field effect transistor (FinFET) through a three-dimensional (3D) full band Monte Carlo simulator with quantum correction. Several scattering mechanisms, such as the acoustic and optical phonon scattering, the ionized impurity scattering, the impact ionization scattering and the surface roughness scattering are considered in our simulator. The effects of the substrate bias and the surface roughness scattering near the Si/SiO_2 interface on the performance of bulk FinFET are mainly discussed in our work. Our results show that the on-current of bulk FinFET is sensitive to the surface roughness and that we can reduce the substrate leakage current by modulating the substrate bias voltage.

Keywords: bulk fin field effect transistor (FinFET), three-dimensional (3D) Monte Carlo simulation, surface roughness scattering, substrate bias effect

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1. Introduction

As complementary metal oxide semiconductor CMOS scales down to the 22 nm technology node and beyond, the semiconductor industry is facing many challenges, such as short channel effects and some leakage issues. However, these problems can be solved by either introducing new materials or by developing new device structures. The fin field effect transistor (FinFET) has been regarded as a most promising device structure for the scaling down trend of the technology roadmap.[1−4] Intel already announced the three-dimensional (3D) Tri-Gate transistors in its 22 nm microprocessor in 2011.[5] FinFET has shown better down-scaling characteristics and higher performance than the conventional planar metal–oxide–semiconductor field-effect transistor (MOSFET),[6,7] due to better gate controllability of the channel. Compared with Bulk FinFET, silicon-on-insulator (SOI) FinFET has some disadvantages, such as high wafer cost and high defect density.[8] With little heat transfer problems and its ability to be integrated with standard bulk CMOS technology, bulk FinFET is now gaining more and more attention in recent research.[9−13]

However, the substrate leakage issues and the ON state performance of bulk FinFET were not discussed in Refs. [9]–[13]. Since bulk FinFET has the disadvantage in sub channel leakage due to short channel lengths,[11] we need to consider the substrate leakage issues, which are important for reducing the power consumption and improving the device performance. The decreasing of the substrate leakage current can be achieved by modulating the substrate bias voltage. As MOSFETs scale down to the nano-scale, the electronic properties of two-dimensional (2D) electrons in the Si inversion layer are significantly affected by the oxide-semiconductor interface.[14,15] The effects are modelled by the surface roughness scattering rate near the Si/SiO_2 surface, which is first studied in the simulation of bulk FinFET. So we mainly discuss the effects of the substrate bias and the surface roughness scattering near the Si/SiO2 interface on the performance of bulk FinFET in this work.

2. Simulation method and device structure

A 3D parallel Monte Carlo simulator is used in our work. The Monte Carlo method and the physical

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model are well verified and calibrated in Refs. [16]–[20]. The band structure of Si and some models of scattering such as acoustic and optical phonon scattering, ionized impurity scattering, and impact ionization scattering are described in Refs. [19] and [20]. The surface roughness scattering is modelled based on the scattering matrix in the Gaussian model,[21] and given as

$$S_{\rm sr}(E_{\rm eff}) = \frac{\pi m^* e^2}{\hbar^3} L^2 \Delta^2 E_{\rm eff}^2. \quad (1)$$

The model parameters of correlation length L and roughness amplitude Δ have been carefully calibrated as $L = 2.0$ nm and $\Delta = 0.113$ nm for the electron to reproduce the universal experimental mobility curves,[22] and $E_{\rm eff}$ is the effective transverse electric field, which is evaluated with the method used in Ref. [23].

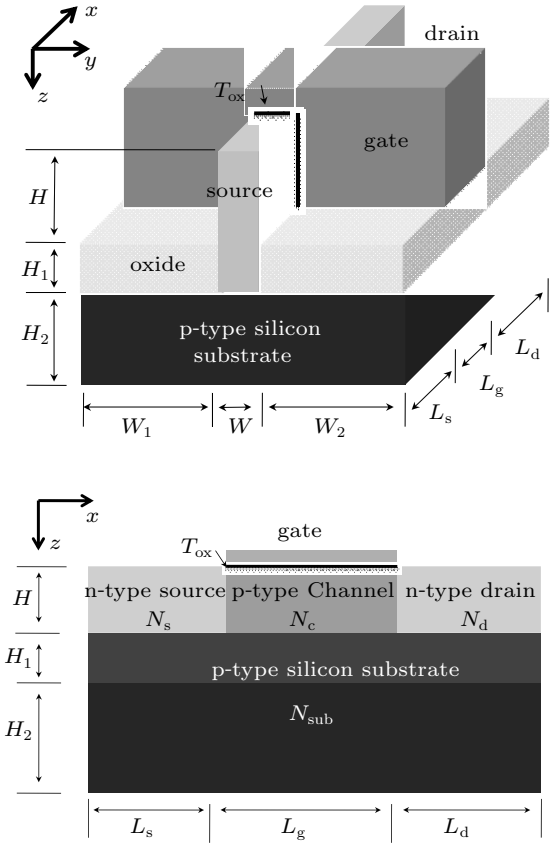


Fig. 1. Schematic view of bulk FinFET.

In this work, the Monte Carlo simulator is used to study the effects of the substrate bias and the surface roughness scattering near the Si/SiO_2 interface on the performance of bulk FinFET. Figure 1 shows the schematic view of the device, whose default parameters are given in Table 1.

Table 1. Default parameters used in this work.

Parameters	Description	Value
L_g	gate length	20 nm
L_s/L_d	source/drain length	20 nm
W	fin width	10 nm
W_1/W_2	substrate width	30 nm/30 nm
T_{ox}	gate oxide thickness	1 nm
H	fin height	40 nm
H_1/H_2	substrate height	20 nm/100 nm
N_s/N_d	n-doping source or drain density	10^{20} cm^{-3}
N_c	p-doping channel density	10^{18} cm^{-3}
N_{sub}	p-doping substrate density	2×10^{16} cm^{-3}
Φ_{ms}	the work function difference between metal and silicon	−0.5 eV

3. Results and discussion

The effects of the substrate bias and the surface roughness scattering near the Si/SiO2 interface on the performance of bulk FinFET are mainly discussed in our work. Figure 2 shows the I_{ds}-V_{gs} characteristics of bulk FinFET at $V_{ds} = 0.1$ V, 1.0 V, and Fig. 3 displays I_{ds}-V_{ds} characteristics of bulk FinFET at $V_{gs} = 0.6$ V, 0.8 V, 1.0 V. By calibrating the parameters, the characteristics of bulk FinFET in the simulation can be well consistent with the experimental data in Ref. [11].

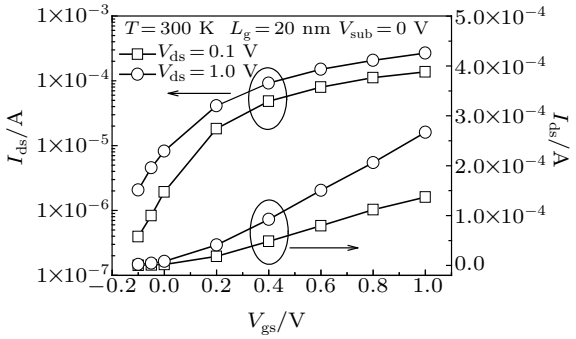


Fig. 2. I_{ds}-V_{gs} characteristics of bulk FinFET at V_{ds} = 0.1 V, 1.0 V.

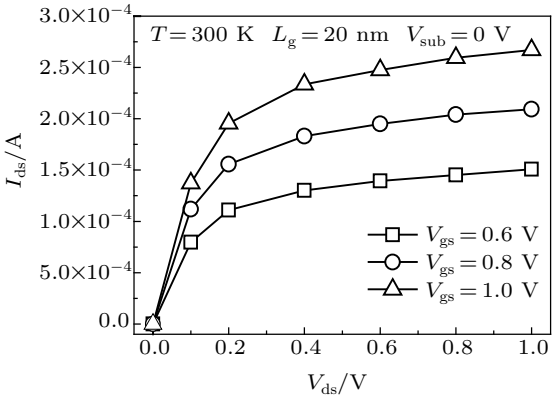


Fig. 3. I_{ds}-V_{ds} characteristics of bulk FinFET at V_{gs} = 0.6 V, 0.8 V, 1.0 V.

3.1. Surface roughness scattering

As MOSFET scales down to the nano-scale, the electronic properties of two-dimensional electrons in the Si inversion layer are significantly affected by the oxide–semiconductor interface. Inversion charge density and the electron average velocity distributions along the channel with and without surface roughness in a 20 nm gate-length bulk FinFET are plotted in Figs. 4 and 5 respectively.

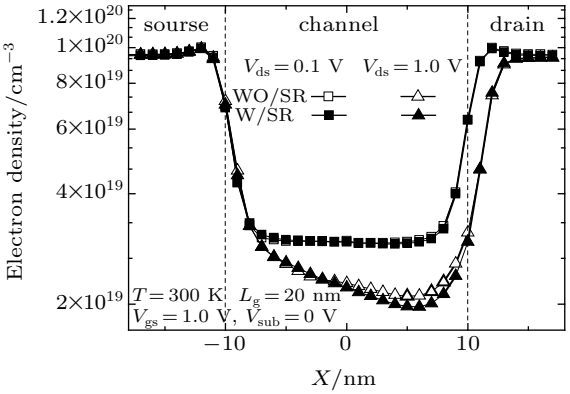


Fig. 4. Electron density distributions along the channel with and without surface roughness in a 20 nm gate-length bulk FinFET at V_{ds} = 0.1 V, 1.0 V.

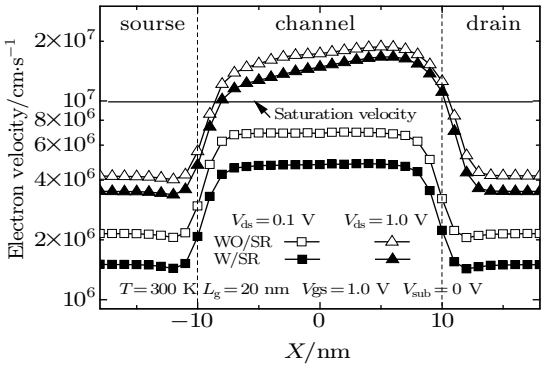


Fig. 5. Electron average velocity distributions along the channel with and without surface roughness in a 20 nm gate-length bulk FinFET at V_{ds} = 0.1 V, 1.0 V.

As shown in Fig. 4, the surface roughness affects the electron density distribution in the channel, especially in the channel near the drain side, since the self-consistent simulation is used. However, the inversion charge density at the source side is almost changeless. Figure 5 shows the curves of the saturation velocities in bulk Si. It is obvious that there exists non-local transport almost in the whole channel for Si even with surface roughness at V_{ds} = 1.0 V. Different from the case of inversion charge density, the velocity is affected by the surface roughness in the whole channel. The simulation results in Figs. 5 and 6 indicate that surface roughness more seriously affects the source-side velocity of an electron than the drain-side velocity. Thus, it can be concluded that the on-current is greatly sensitive to the surface roughness results from the stronger relationship between source-side velocity and surface roughness scattering. Figure 6 also shows that surface roughness has more influence at the low drain bias voltage or at low electric field along the channel.

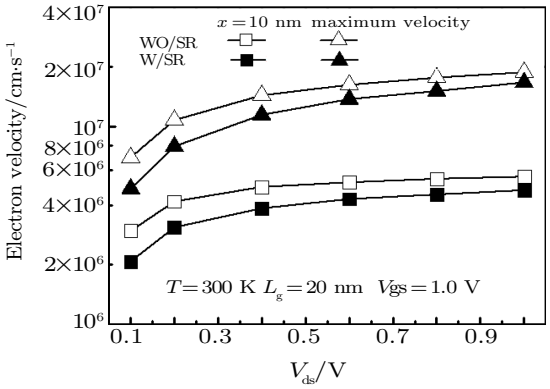


Fig. 6. Electron average velocity at $X = -10$ nm and electron maximum velocity along the channel with and without surface roughness in a 20 nm gate-length bulk FinFET with V_{ds} varying from 0.1 V to 1.0 V.

The effects of the surface roughness scattering near the Si/SiO_2 interface on the performance of bulk FinFETs with the gate length varying from 12 nm to 24 nm are also investigated. Figure 7 shows the source-drain currents of bulk FinFETs under different conditions. In the figure, I_{BL} is the source-drain ballistic current without phonon scattering and ionized impurity scattering, I_{ph+imp} is the source-drain current with phonon scattering and ionized impurity scattering in bulk FinFET, and $I_{ph+imp+SR}$ is the source-drain current with the surface roughness scattering besides the phonon scattering and ionized impurity scattering in bulk FinFET. The difference between the simulation results of the source-drain current with and without phonon scattering and ionized impurity scattering describes the influence of phonon scattering together with ionized impurity scattering, while the difference between the simulation results of the source-drain current with and without surface roughness describes the influence of surface roughness scattering.

The source-drain currents I_{BL}, I_{ph+imp} and $I_{ph+imp+SR}$ all decrease with gate length varying from 12 nm to 24 nm, and surface roughness has more influence in bulk FinFET at the low drain bias voltage or at the low electric field along the channel. To better investigate the effects of the surface roughness scattering near the Si/SiO_2 interface on the performance

of bulk FinFETs with different gate lengths, we define a factor $K_{\rm SR}$ to characterize the effect of the surface roughness scattering on current decrease, the same as $K_{\rm Ph+Imp}$ which reflects the effect of the phonon scattering together with ionized impurity scattering. They are given as

$$K_{\rm SR} = \frac{I_{\rm ph+imp} - I_{\rm ph+imp+SR}}{I_{\rm BL}}, \tag{2}$$

$$K_{\rm ph+imp} = \frac{I_{\rm BL} - I_{\rm ph+imp}}{I_{\rm BL}}. \tag{3}$$

Figure 8 shows that the surface roughness has a greater influence at the low drain bias voltage while the phonon scattering together with ionized impurity scattering has a greater influence at the high drain bias voltage. Considering the surface roughness scattering alone, the decrease is about 10%–15% at high drain bias voltage and rises up to 20%–30% at low drain bias voltage, which is consistent with the trends in Figs. 4–6; surface roughness has a greater influence in the long channel in our nano-scale FinFETs work.

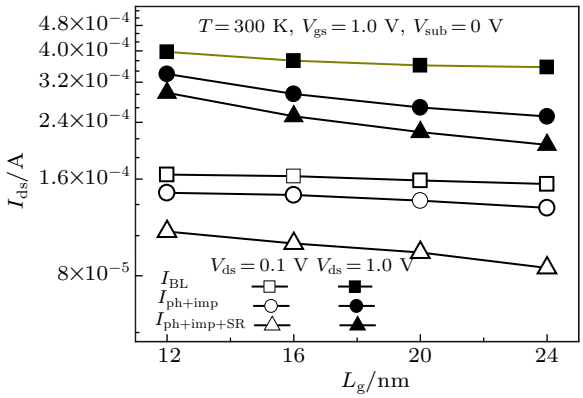


Fig. 7. Variations of source-drain currents $I_{\rm BL}$ $I_{\rm ph+imp}$ and $I_{\rm ph+imp+SR}$ of bulk FinFET with the gate length changing from 12 nm to 24nm at $V_{\rm ds}$=0.1 V, 1.0 V.

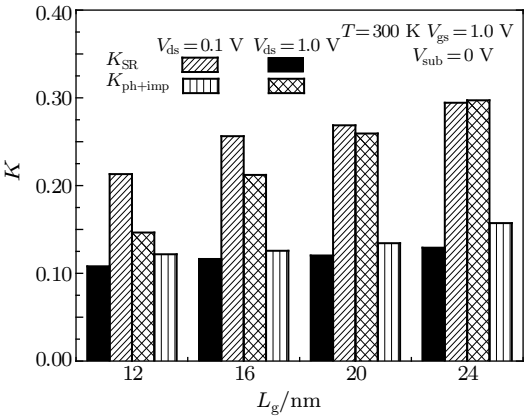


Fig. 8. Comparison between the influence of phonon scattering together with ionized impurity scattering and the influence of surface roughness in bulk FinFET for gate length varying from 12 nm to 24 nm at $V_{\rm ds}$ = 0.1 V, 1.0 V.

3.2. Substrate bias effect

With devices scaling down to the nano-scale, we need to consider the substrate leakage issues, which is important for reducing the power consumption and improving the device performance. The substrate leakage current can be reduced by modulating the substrate bias voltage.

Figures 9 and 10 illustrate that the electron density and the average velocity along the channel in a 20 nm gate-length bulk FinFET with the substrate bias voltage varying from 0.7 V to 1.0 V are almost changeless at $V_{\rm ds}$ = 0.1 V, 1.0 V. Thus, we can conclude that the substrate bias voltage has little influence on the electron density and the average velocity distributions along the channel in bulk FinFETs, resulting in little change in the source-drain current as shown in Fig. 12.

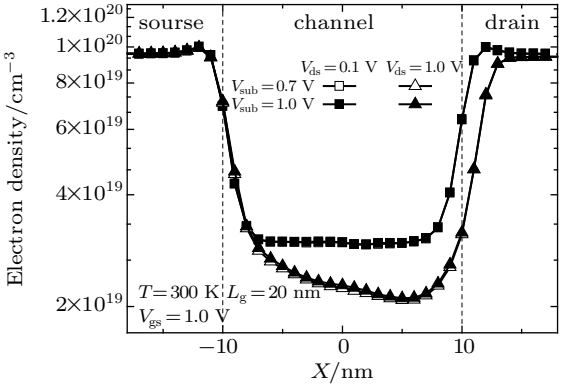


Fig. 9. Electron density distributions along the channel in a 20 nm gate-length bulk FinFET with the substrate bias voltage varying from 0.7 V to 1.0 V at $V_{\rm ds}$ = 0.1 V, 1.0V.

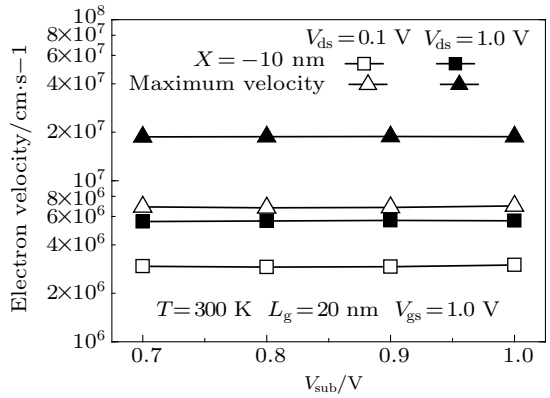


Fig. 10. The electron average velocity at $X = -10$ nm and the electron maximum velocity along the channel in a 20 nm gate-length bulk FinFET with substrate bias voltage varying from 0.7 V to 1.0 V at $V_{\rm ds}$ = 0.1 V, 1.0 V.

The hole density distributions along the channel in a 20 nm gate-length bulk FinFET with the substrate bias voltage varying from 0.7 V to 1.0 V, are

plotted in Fig. 11. Both the hole density along the channel and the substrate leakage current increase due to substrate bias modulation, and the substrate leakage current is higher at low drain bias voltage, as shown in Fig. 12.

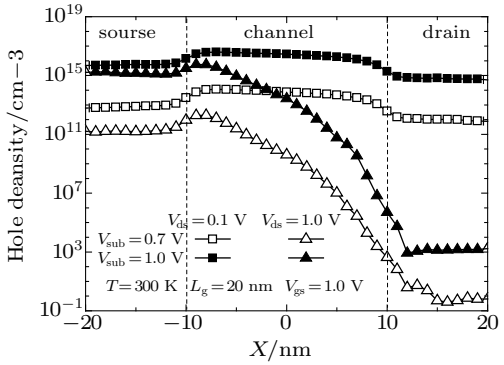


Fig. 11. Hole density distributions along the channel in a 20 nm gate-length bulk FinFET with the substrate bias voltage varying from 0.7 V to 1.0 V at V_{ds} = 0.1 V, 1.0 V.

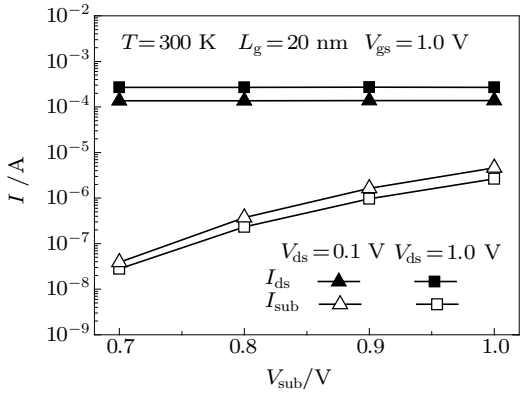


Fig. 12. Source-drain current and substrate current of bulk FinFET with substrate bias voltage varying from 0.7 V to 1.0 V at V_{ds} = 0.1 V, 1.0 V.

4. Conclusions

In this paper, the performance of a bulk FinFET is investigated through a 3D full band Monte Carlo simulator with quantum correction. Several scattering mechanisms are taken into consideration in our simulator, such as acoustic and optical phonon scattering, ionized impurity scattering, impact ionization scattering and surface roughness scattering. Simulation results show that the surface roughness and the substrate bias play an important role in nano-scale bulk FinFETs. The on-current greatly sensitive to the surface roughness results from the stronger relationship between the source-side velocity and surface roughness scattering. The surface roughness has a greater influence at the low drain bias voltage while the phonon scattering together with ionized impurity scattering has greater influence at the high drain bias voltage. The substrate bias voltage has little influence on the source-drain current of nano-scale bulk FinFETs. We can reduce the hole density along the channel and the substrate leakage current by modulating the substrate bias voltage.

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