Nano-scale gap filling and mechanism of deposit–etch–deposit process for phase-change material*

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(Received 29 February 2012; revised manuscript received 11 June 2012)

$Ge_2Sb_2Te_5$ gap filling is one of the key processes for phase-change random access memory manufacture. Physical vapor deposition is the mainstream method of $Ge_2Sb_2Te_5$ film deposition due to its advantages of film quality, purity, and accurate composition control. However,the conventional physical vapor deposition process cannot meet the gap-filling requirement with the critical device dimension scaling down to 90 nm or below. In this study, we find that the deposit–etch–deposit process shows better gap-filling capability and scalability than the single-step deposition process, especially at the nano-scale critical dimension. The gap-filling mechanism of the deposit–etch–deposit process was briefly discussed. We also find that re-deposition of phase-change material from via the sidewall to via the bottom by argon ion bombardment during the etch step was a key ingredient for the final good gap filling. We achieve void-free gap filling of phase-change material on the 45-nm via the two-cycle deposit–etch–deposit process. We gain a rather comprehensive insight into the mechanism of deposit-etch-deposit process and propose a potential gap-filling solution for over 45-nm technology nodes for phase-change random access memory.

Keywords: deposit–etch–deposit process, single step deposit, gap filling, re-deposition

PACS: 52.50.Qt, 81.65.Cf, 68.60.−p, 81.16.−c **DOI:** 10.1088/1674-1056/21/11/115203

1. Introduction

Phase-change random access memory (PCRAM) has been regarded as one of the most promising candidates of the next generation nonvolatile memory because of its high speed, low power, good endurance, good scalability, and fabrication compatibility with standard complementary metal-oxide-semiconductor (CMOS) process.[1−6] It is believed that the advantages of the PCRAM will become more remarkable at the 45-nm or below technology node.[4,5] The PCRAM is based on chalcogenide materials, such as $Ge_2Sb_2Te_5$ (GST), SiSbTe (SST), and AgInTeSb,[7−9] and uses the Joule heat to change the phase of such materials. This reversible phase transition between amorphous (high resistivity) and crystalline (low resistivity) states enables the data storage. The PCRAM has a wide application in high density and capacity of embedded CMOS chips.

To achieve higher density and lower power device performance, there are mainly two schemes to fabricate nano-size PCRAM cells: to confine a GST pattern on blanket wafer using the dry etch process; to fill up a small via hole with GST film followed by a GST chemical mechanical polishing process. In the gap-filling case, the GST film is usually filled in by atomic layer deposition (ALD), metalorganic chemical vapor deposition (MOCVD), and physical vapor deposition (PVD). The ALD and CVD can achieve void-free GST gap filling on trench wafers for the 45-nm critical dimension (CD) with an aspect ratio (AR) of 7.5 and 7.5-nm CD with an AR of 4, respectively. The PVD is widely used for blanket film deposition instead of the fill-in process on structure wafers with an AR greater than 1.[10−12] However, the dry etch process suffers sidewall damage and a scalability limit.[11] For ALD and MOCVD processes, their

*Project supported by the National Basic Research Program of China (Grant Nos. 2010CB934300, 2011CBA00607, and 2011CB932800), the National Integrate Circuit Research Program of China (Grant No. 2009ZX02023-003), the National Natural Science Foundation of China (Grant Nos. 60906004, 60906003, 61006087, and 61076121), and the Science and Technology Council of Shanghai, China (Grant No. 1052nm07000).

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disadvantages of impurity and composition control restrict their applications in the PCRAM despite the good gap-filling capability.[13−15] Currently, the PVD is the mainstream method of phase-change material film deposition due to its merits of film quality, purity, and accurate composition control. However, the conventional PVD process cannot meet the gap-filling requirements when the CD of device scales down to 45 nm and beyond.

In this work, a novel PVD process, deposit–etch–deposit (DED) process, is developed for GST deposition. Its applications in filling vias of different sizes are compared. The mechanism of gap-filling improvement by the DED process is also investigated.

2. Experimental details

GST film was deposited and etched using a magnetron sputtering system at room temperature. A radio-frequency generator (13.56 MHz) was used to initiate plasma with argon gas. The background pressure of the sputtering system was 3.4×10^{-6} Pa. There was no vacuum breaking between the deposition and etch process switching. During the DED sputtering process, the etch amount (about 20 nm) was about 50% of the deposition thickness based on blanket wafer results. Via patterns with the aspect ratio ranging from 0.4:1 to 2:1 (45-nm to 300-nm CD) were used for the gap-filling evaluation. Samples were prepared with single-step deposition, one-cycle and two-cycle DED process for comparison. The GST gap filling was characterized by scanning electron microscope (SEM) and transmission electron microscope (TEM). Ge, Sb, and Te atomic composition-depth profiles were tested by glow discharge optical emission spectroscopy (GD-OES).

3. Results and discussion

Single-step sputtering process partially filled the big via (300-nm CD) with the AR of 0.4:1 (see Fig. 1(a)). However, it failed to fill the small via (45-nm CD) with the AR of 2:1 (see Fig. 1(b)) because the GST atoms sputtered from the alloy target could not be deposited into the via bottom through the slot formed by the serious overhang at the via's top entrance.The

DED sputtering process could improve the GST gap filling. One-cycle DED process partially filled the small via (45-nm CD) with the AR of 2:1 (see Fig. 2(a)). The GST thickness in the via bottom was greatly improved by about 100% (from 30 nm to 60 nm) compared with the single-step sputtering process. With the two-cycle DED process, void-free GST gap filling was achieved on the via, as shown in Fig. 2(b).

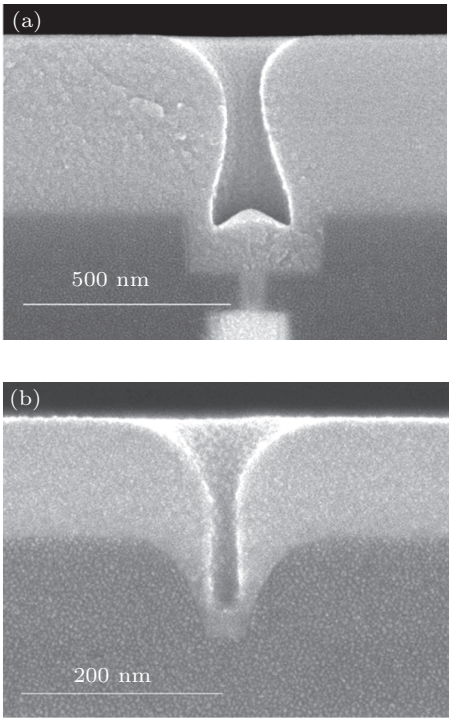


Fig. 1. GST gap filling through the single-step sputtering process on (a) 300-nm CD with the AR of 0.4:1, and (b) 45-nm CD with the AR of 2:1.

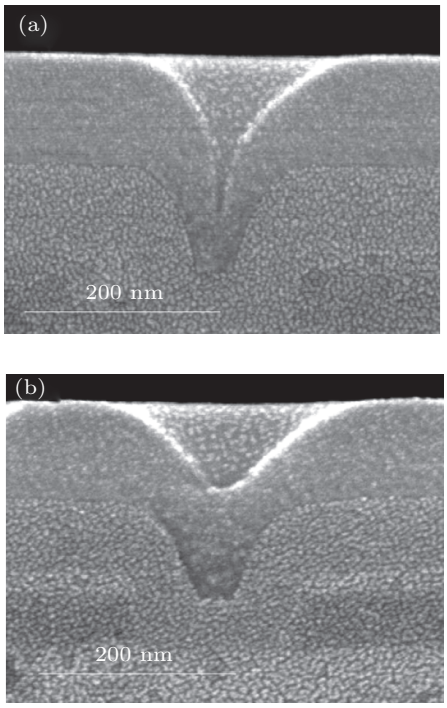


Fig. 2. GST gap filling for a small via (45-nm CD with the AR of 2:1) by (a) one-cycle DED process, and (b) two-cycle DED process.

Re-deposition was proved to be the key ingredient of good gap filling of the DED sputtering process on a small-size via. After the first 40-nm GST deposition (see Fig. 3(a)), about 16-nm GST filled the via bottom, but the overhang at the via's top entrance increased accordingly. In this case, the GST gap filling could not be obviously improved even with increasing the GST deposition thickness. With the first etching process, overhang was almost completely removed with a loss of only about 19% of the GST bottom thickness (see Fig. 3(b)). About 20-nm GST film in the via bottom was achieved, and a sharp slot was formed by overhang after the second 40-nm GST deposition (see Fig. 3(c)). The most distinct change during the second etch process (see Fig. 3(d)) is that the GST film in the via bottom increased over 100% and no obvious overhang was observed at the via's top entrance. Based on the SEM cross section results, we believe that some GST atoms on the sharp slot sidewall were re-sputtered into the via bottom. At the same time, the GST overhang on the via's top entrance was efficiently removed. The profile became easier for the final deposition step to fully fill in the vias.

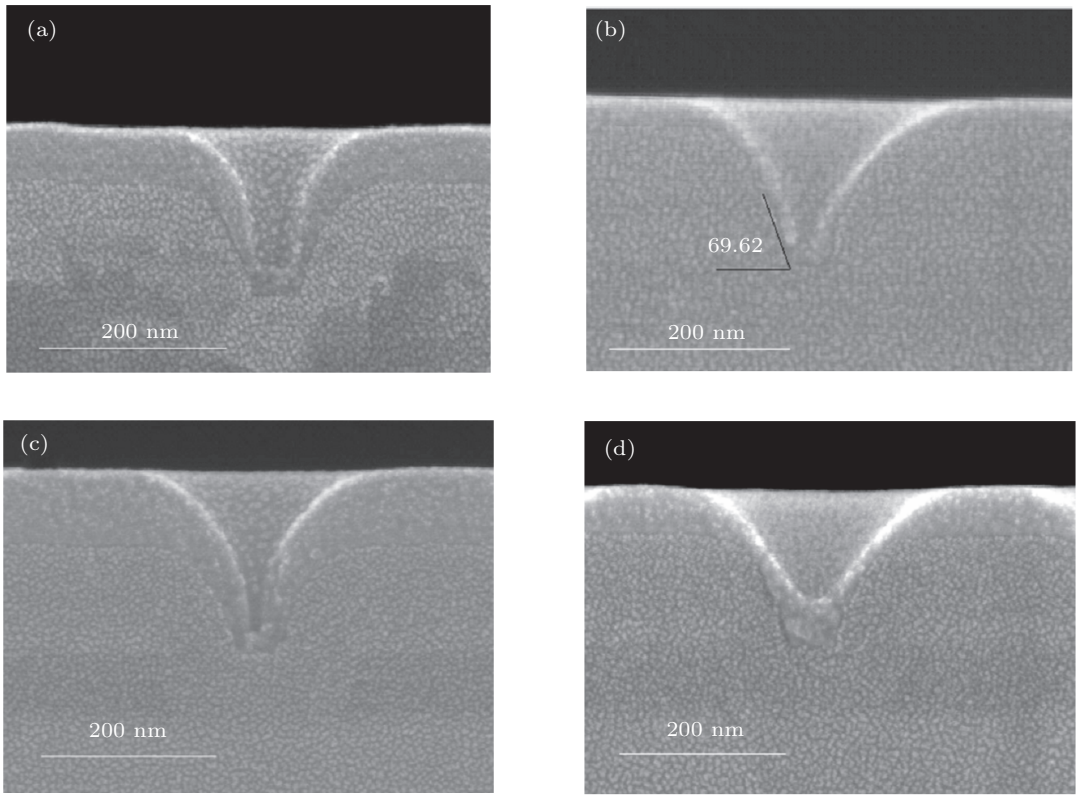


Fig. 3. Re-deposition mechanism of the DED sputtering process for a small via (45-nm CD with the AR of 2:1) by (a) the first GST deposition, (b) the first GST etching, (c) the second GST deposition, and (d) the second GST etching.

Comparing with the small-size via, we find a completely different re-sputtering mechanism and gap-filling capability improvement for the big-size via during the etch sputtering process (see Figs. 4(a) and 4(b)). The GST thickness on the via bottom decreased by about 58%, while the sidewall increased by about 15%. As showen in the SEM cross section images (see Figs. 5(a) and 5(b)), due to the bigger via open size, many argon ions easily reached the via bottom and bombarded the GST film. Then some GST atoms on the via bottom were partially re-deposited onto the via sidewall. After the final deposition, no obvious improvement of GST gap filling was found on the big-size via (see Fig. 5(c)).

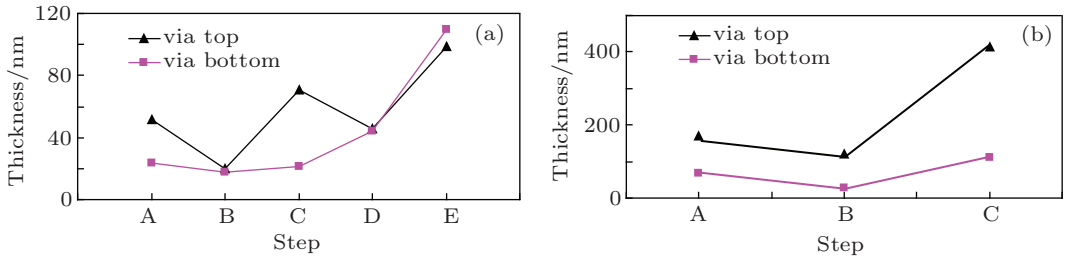


Fig. 4. (colour online) Comparison between DED sputtering processes with (a) small size and (b) big size. A: first depositon, B: first etching, C: second etching, D: second etching, E: final deposition.

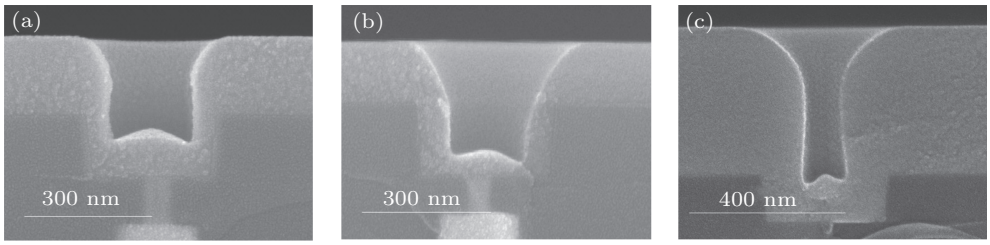


Fig. 5. Re-deposition mechanism of the DED sputtering process for a big via (300-nm CD with the AR of 0.4:1) by (a) the first GST deposition process, (b) the first GST etching process, and (c) the final deposition process.

Figure 6(a) shows the TEM image of a layered structure after the two-cycle DED process, which was generated by different sputter yields of Ge, Sb, and Te during the etching step. Figure 6(b) shows the GST composition depth profile by the GD-OES. Comparing with the composition of the GST film prepared by one-step deposition in DED GST film, the atomic percentage of Te was found to be about 3.54% or less, while that for Ge and Sb was about 1.04% and 2.60% higher, respectively.

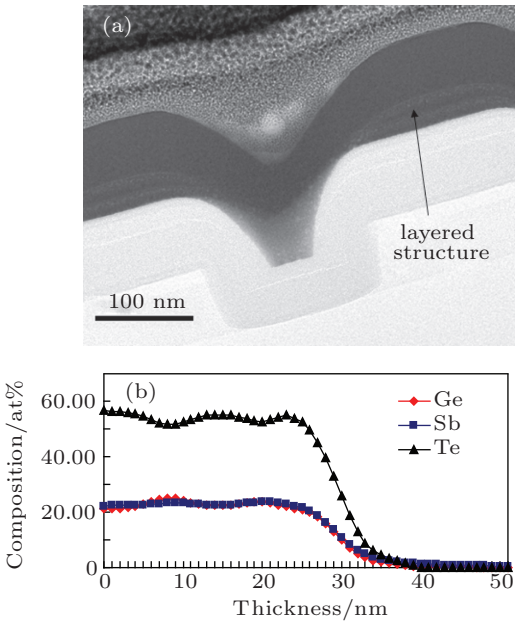


Fig. 6. (colour online) (a) TEM cross section of two-cycle DED and (b) GST atomic composition depth profile obtained by the GD-OES.

4. Conclusions

We achieved void-free GST gap filling on a small via (45-nm CD with the AR of 2:1) with the DED sputtering process, provided a rather comprehensive insight into the mechanism of DED process by the SEM cross section, and clarified that re-sputtering of the GST material from via sidewall to via bottom by argon ion bombardment during the etching step was the key ingredient of the final good gap filling. In addition, we compared and studied different re-sputtering mechanisms for vias of different sizes.

This DED process has been qualified on the PCRAM device by electrical performance testing. It is a good potential gap-filling solution for 45-nm (or lower) technology nodes for phase-change random access memory.

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